LAUTERBACH
DEVELOPMENT TOOLS

Stimuli Generator User's Guide

MANUAL

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Version 06-Jun-2024

Stimuli-Generator

Basics

The stimuli-generator is a bidirectional input/output device for automatic test applications.. The generator is connected to the PODBUS of the TRACE32 system. The features of the stimuli generator are:

- 64 input/output channels
- input/output can be defined in 8-bit groups
- latched input
- output ports can be read back for short-circuit-test
- any channel can be switched to the frequency-counter
- 4 analog outputs
- 8 analog inputs, differential or single ended
- connection tester for measurement in running systems
- logic level tester
- pulse generator
- pattern generator (only on Version 2)
- channel-names can be configured
- automated test sequences with PRACTICE

The stimuli generator must be connected to the system on power up. Otherwise the STG driver software is not linked. The default device-name is '**S:**'.

Input

Every input port may be readed directly

Latched Input

Input data are latched in the input register by a selected trigger signal.

Output

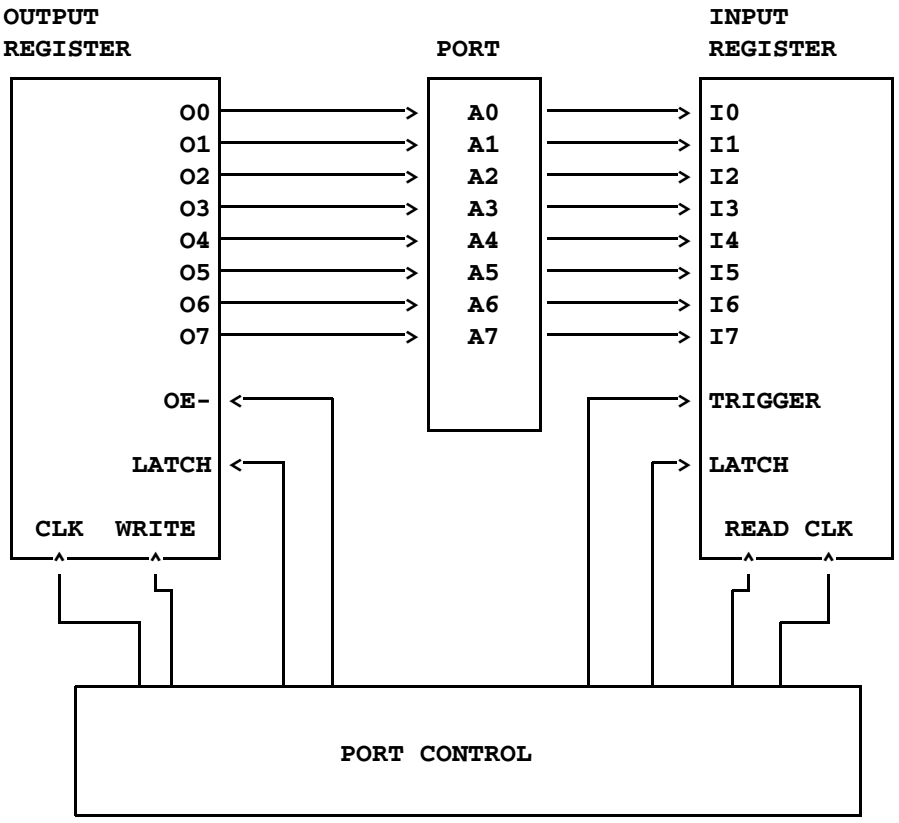
Output data are set directly to the output register.

Output with Enable

Every output block may be set to tristate by setting the corresponding OE line to high.

Important !!!

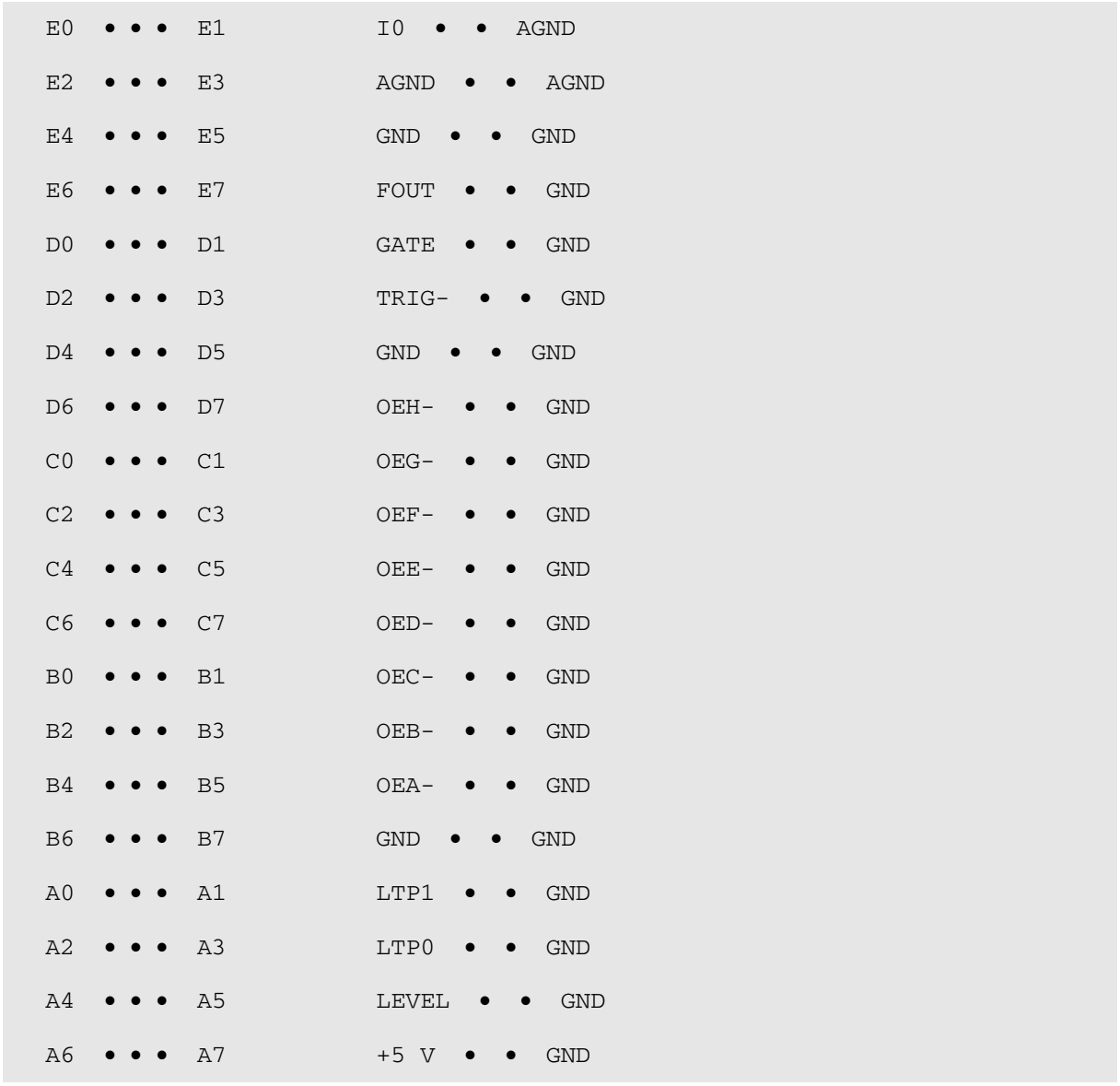
All output ports are driven by PushPull CMOS drivers. The outputs are short-circuit-protected within a voltage range from 0 … 5 V. The short-circuit current is about 10 mA.



Schematic I/O-Port

The simuli generator has 8 similar I/O ports, named A-H.

H0	• • •	H1	O3	• •	AGND
H2	• • •	H3	O2	• •	AGND
H4	• • •	H5	O1	• •	AGND
H6	• • •	H7	O0	• •	AGND
G0	• • •	G1	AGND	• •	AGND
G2	• • •	G3	I7	• •	AGND
G4	• • •	G5	I6	• •	AGND
G6	• • •	G7	I5	• •	AGND
F0	• • •	F1	I4	• •	AGND
F2	• • •	F3	I3	• •	AGND
F4	• • •	F5	I2	• •	AGND
F6	• • •	F7	I1	• •	AGND


E0 E1
E2 E3
E4 E5
E6 E7
D0 D1
D2 D3
D4 D5
D6 D7
C0 C1
C2 C3
C4 C5
C6 C7
B0 B1
B2 B3
B4 B5
B6 B7
A0 A1
A2 A3
A4 A5
A6 A7
I0 AGND
AGND AGND
GND GND
FOUT GND
GATE GND
TRIG- GND
GND GND
OEH- GND
OEG- GND
OEF- GND
OEE- GND
OED- GND
OEC- GND
OEB- GND
OEA- GND
GND GND
LTP1 GND
LTP0 GND
LEVEL GND
+5 V GND


POWER
SELECT
HIGH
LOW

Digital Commands

Get	Reads the digital ports
ISet	Sets the digital ports
IPULSE	Defines the pulse generator
Mode	Defines the modes of the ports
STOre	Stores the setup
RESet	Resets the stimuli generator

Analogous Port Functions

The stimuli generator support 4 output ports and 8 input ports. The input ports can measure relative to AGND or to AIN7 (differential mode).

Analogous Commands

IN	Reads the analog input ports
IOUT	Sets the analogous output ports

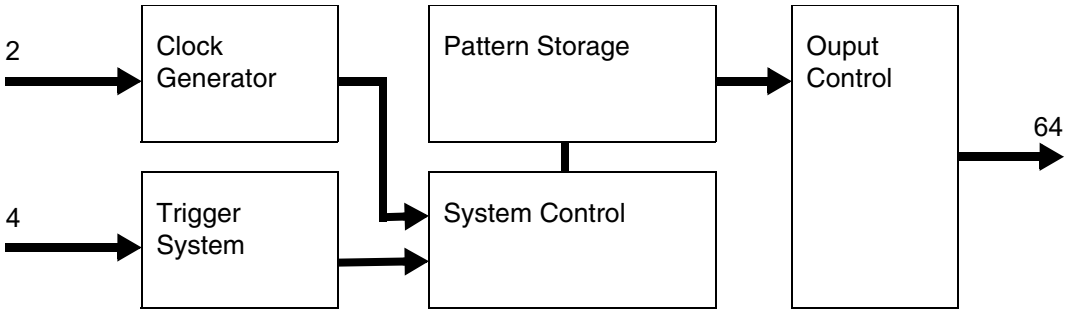
State line

The state line displays the level of every input signal, the state of the logic probe and the connection tester.

```
76...210 ........ ........ ........ ........ ........ ........ .......
CON LOW

  ch A     ch B     ch C     ch D     ch E     ch F     ch G     ch H
```

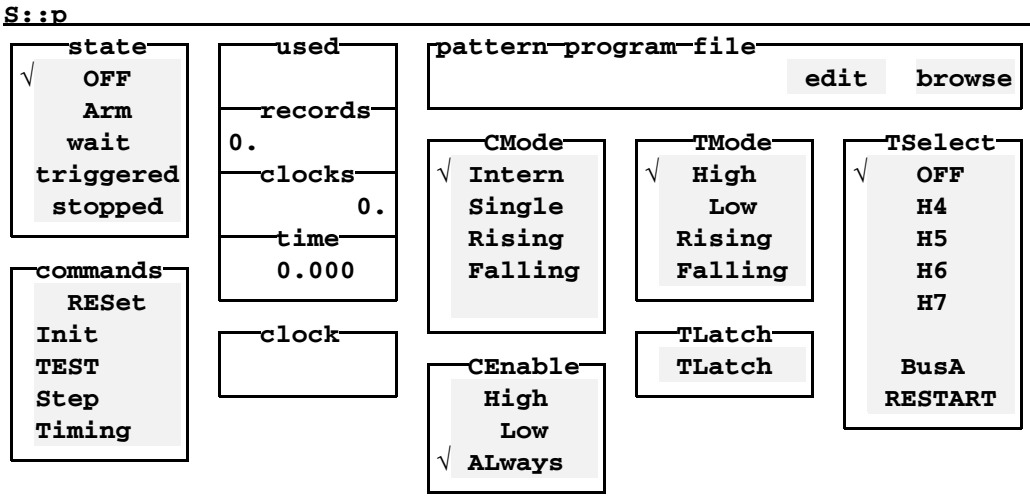
Function



Pattern Generator

The pattern generator storage memory is 256 frames in depth and 64 bit width. Every frame can store a pattern or a repetition time. 64 pattern bits are send to the probe and one to the internal trigger bus. Every pattern can be repeated up to 4000 Mio. times. The max. external clock speed is 50 MHz, the delay between clock and output approx. 20 ns.

The pin for the pattern generator must be set to Output or OutputEnable. A true (logical 1) pattern signal inverts the default setting for the output (High pulse if output set to low or low pulse if output set to high).



After programming the pattern generator, the pattern sequence can be started by the command **Pattern.Arm**. On every clock edge the next data pattern is activated on the output probes. The pattern generator can be stopped by the command **Pattern.OFF**. The pattern sequence is restarted by the **Pattern.Init** command.

Pattern.state	Display control window of pattern generator
Pattern.Arm	Starts pattern generator
Pattern.OFF	Stops pattern generator
Pattern.Init	Stops pattern generator and sets pattern counter to start position
Pattern.TEST	Init and Arm pattern generator
Pattern.Step	Single-step
Pattern.RESet	Reset pattern generator to power-on state

Clock Generator

The pattern generator can run with internal or external clock and in single-step mode. The internal clock is fixed to 50 MHz. The external clock edge may be selected. An additional clock enable inputs qualifies the internal or external clock signal. The external clock signal is on input x.24 , the clock-enable signal on input x.25. Additional the clock generated by the synchronous clock qualifier can be used.

Pattern.CMode	Selects internal or external clock and clock edge
Pattern.CEnable	Controls clock qualifier
Pattern.Step	Single-Step function

Trigger System

The trigger input is either edge or level sensitive. The trigger signal can be supported external (input H4 to H7) or internal by the bus or the serial line tester. Usually the trigger signal is only sensed, if the pattern generator is in WAIT state. Previous trigger events are ingnored. By the function **TLatch** previous trigger events are stored until the next WAIT instruction occurs in the pattern sequence. Trigger overruns are ignored. The external trigger inputs are on H.4 to H7.

Pattern.TSelect	Selects the trigger input
Pattern.TMode	Selects the trigger mode
Pattern.TLatch	Selects trigger latch mode

```
S::w.p.p
standby A:0
repeat 3
(
   set A0:1
   set A0:0
)
delay 0.3us
set A1:1
delay 0.3us
set A1:0
wait
restart
```

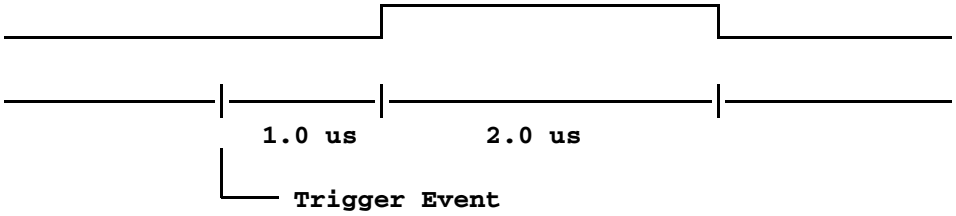
The pattern memory is programmed by an ASCII file. Every line in the text defines a new pattern setup. A delay function repeats the previous state n times. 16 pattern lines plus 4 bus trigger lines can be controlled by the pattern generator. The pattern file commands are:

Set	Defines the state of the pattern generator output lines and the bus trigger lines. A string is interpreted as multiple patterns. A mask is used to change only some bits in the sequence. All bit positions with don't care bits don't change the previous bits.
DEFAULT	Defines the default setup for Delay, Wait, BUS or NONE
STANDBY	Defines the pattern at the reset state of the pattern generator
WAIT	Wait for trigger event
DELAY	Repeat previous state
RESTART	The pattern sequence starts again with the first line
STOP	The pattern sequence stops here. It can be started by the commands **INIT** and **ARM** (or **TEST**) only.
RePeaT	Repeat function. The next line or the next block will be repeated n times. Repeat functions may be nested.
( )	The block brackets are used to mark blocks for the repeat function.
BUSA	A signal will be send over the corresponding bus trigger line BUSA.
Trigger	Trigger Analyzer

Pattern.Program	Defines the pattern sequence
Pattern.ReProgram	Load an already defined pattern sequence

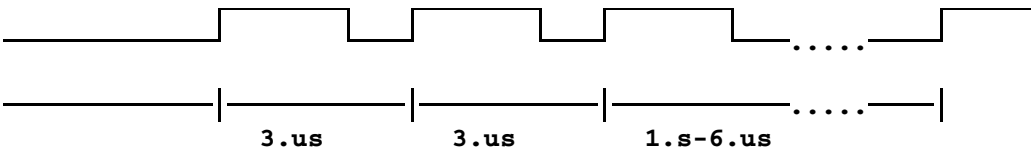
Monoflop function with delay

```
standby A0:0                    ; set channel A0 to zero
wait                            ; wait for trigger event
delay   0.98 us                 ; delay 0.98 us
set     A0:1                    ; set channel A0 to high
delay   1.98 us                 ; delay for 1.98 µs again
set     A0:0                    ; set channel A0 to low
restart                         ; restart pattern sequence
```



Triple pulse every second

```
standby A0:0                   ; set channel 0
RePeaT  3.
(
set     A0:1                   ; set A0 to high
delay   1.98us                 ; delay for 1.9 µs again
set     A0:0                   ; set A0 to low
delay   0.98us                 ; pulse low time 0.9 µs
)
delay   1.s-6.us-0.02us
restart                        ; restart pattern sequence
```



Cascading pulses

```
standby A0:0  p.1:0             ; set all aux lines to zero
set     A0:1                    ; set A0 to high
delay   1.98us                  ; delay for 1.9 µs
set     A1:1                    ; set A1 to high
delay   1.98us
set     A2:1                    ; set A2 to high
stop
```