

# Simulator for V850

MANUAL

# Simulator for V850

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# Simulator for V850

Version 06-Jun-2024

The screenshot shows the TRACE32 PowerView v850 debugger interface. The top menu bar includes File, Edit, View, Var, Break, Run, CPU, Misc, Trace, Probe, Perf, Cov, Window, and Help. The toolbar below has icons for Step, Over, Diverge, Return, Up, Go, Break, Mode, Find, and a file path. The main window has tabs for B::List.auto, B::Register, and B::Var.Local. The B::List.auto tab displays assembly code for a sieve function, with labels like 680, 690, and 6A4, and various instructions like shl, add, mov, and br. The B::Register tab shows the state of registers R0-R7 and special registers EIP, EIPSW, FEP, and CTP. The B::Var.Local tab shows local variables i, primz, and anzahl with their current values. The bottom status bar shows the current file path P:000010B4 \\larv850\\larv850\\sieve+0x48 and the status stopped.

TRACE32 PowerView v850

File Edit View Var Break Run CPU Misc Trace Probe Perf Cov Window Help

Step Over Diverge Return Up Go Break Mode Find: larv850.c

B::List.auto

addr/line	code	label	mnemonic	comment
P:000010B0	3A11		shl	#0x1,r7
P:000010B2	3A43		add	#0x3,r7
680			k = i + primz;	
P:000010B4	3005		mov	r5,r6 ; i,r6
P:000010B6	EDB5		br	0x108C
		}		
		}		
690	007F		jmp	[r31]
P:000010B8	0000		nop	
P:000010B9	1A5C	exit:	add	#-0x4,r3
P:000010BE	FF630001		st.w	r31,0x0[r3]
P:000010C2	FF230001		ld.w	0x0[r3],r31
P:000010C6	1A44		add	#0x4,r3
P:000010C8	07BFEFA8		jr	0x70 ; __exit
P:000010CC	0000		nop	
P:000010CE	0000		nop	

B::Register

	R8	6012	R16	0	R24	0	S	Stack
R0	0		10	0	R25	0		
R1	8	R9		0				
R2	0	R10	0	R18	0	R26	FFFE028	
R3	FFFFE13C	R11		0	R19	0	R27	0
R4	6000	R12	0	R20	0	R28	1	
R5	0D	R13	0	R21	0	R29	2	
R6	600D	R14	0	R22	0	R30	FFFE150	
R7	1D	R15	0	R23	0	R31	105C	

EIP: 0 EIPSW: 0 ECR: 0 PC: 1084  
FEP: 0 FEP SW: 0 PSW: 20 — I -----  
CTPC: 0 CTP SW: 0 CTBP: 0

B::Var.Local

	i	primz	anzahl
register int	13	29	8
register int	0x0D	0x1D	0x8
register int	NNNC	NNNN	NNNN
register int	UUUR	UUUS	UUUS

B::

components trace Data Var List PERF SYSTEM Step Go Break symbol other previous

P:000010B4 \\larv850\\larv850\\sieve+0x48

stopped

MIX UP

# Introduction

---

This document describes the processor-specific settings and features for the TRACE32 Instruction Set Simulator for V850/RH850.

All general commands are described in the “[PowerView Command Reference](#)” (ide\_ref.pdf) and “[General Commands Reference](#)”.

## TRACE32 Simulator License

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[build 68859 - DVD 02/2016]

The extensive use of the TRACE32 Instruction Set Simulator requires a *TRACE32 Simulator License*.

For more information, see [www.lauterbach.com/sim\\_license.html](http://www.lauterbach.com/sim_license.html).

## Brief Overview of Documents for New Users

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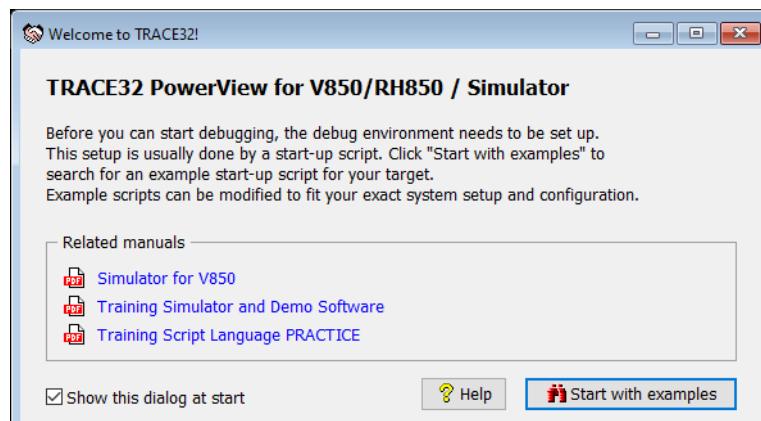
### Architecture-independent information:

- “[Training Basic Debugging](#)” (training\_debugger.pdf): Get familiar with the basic features of a TRACE32 debugger.
- “[T32Start](#)” (app\_t32start.pdf): T32Start assists you in starting TRACE32 PowerView instances for different configurations of the debugger. T32Start is only available for Windows.
- “[General Commands](#)” (general\_ref\_<x>.pdf): Alphabetic list of debug commands.

### Architecture-specific information:

- “[Processor Architecture Manuals](#)”: These manuals describe commands that are specific for the processor architecture supported by your debug cable. To access the manual for your processor architecture, proceed as follows:
  - Choose **Help** menu > **Processor Architecture Manual**.
- “[OS Awareness Manuals](#)” (rtos\_<os>.pdf): TRACE32 PowerView can be extended for operating system-aware debugging. The appropriate OS Awareness manual informs you how to enable the OS-aware debugging.

To get started with the most important manuals, use the **Welcome to TRACE32!** dialog ([WELCOME.view](#)):



## Demo and Start-up Scripts

---

**To search for PRACTICE scripts, do one of the following in TRACE32 PowerView:**

- Type at the command line: [WELCOME.SCRIPTS](#)
- or choose **File** menu > **Search for Script**.

You can now search the demo folder and its subdirectories for PRACTICE start-up scripts (\*.cmm) and other demo software.

You can also manually navigate in the `~/demo/v850/` and `~/demo/rh850/` subfolders of the system directory of TRACE32.

# Quick Start of the Simulator

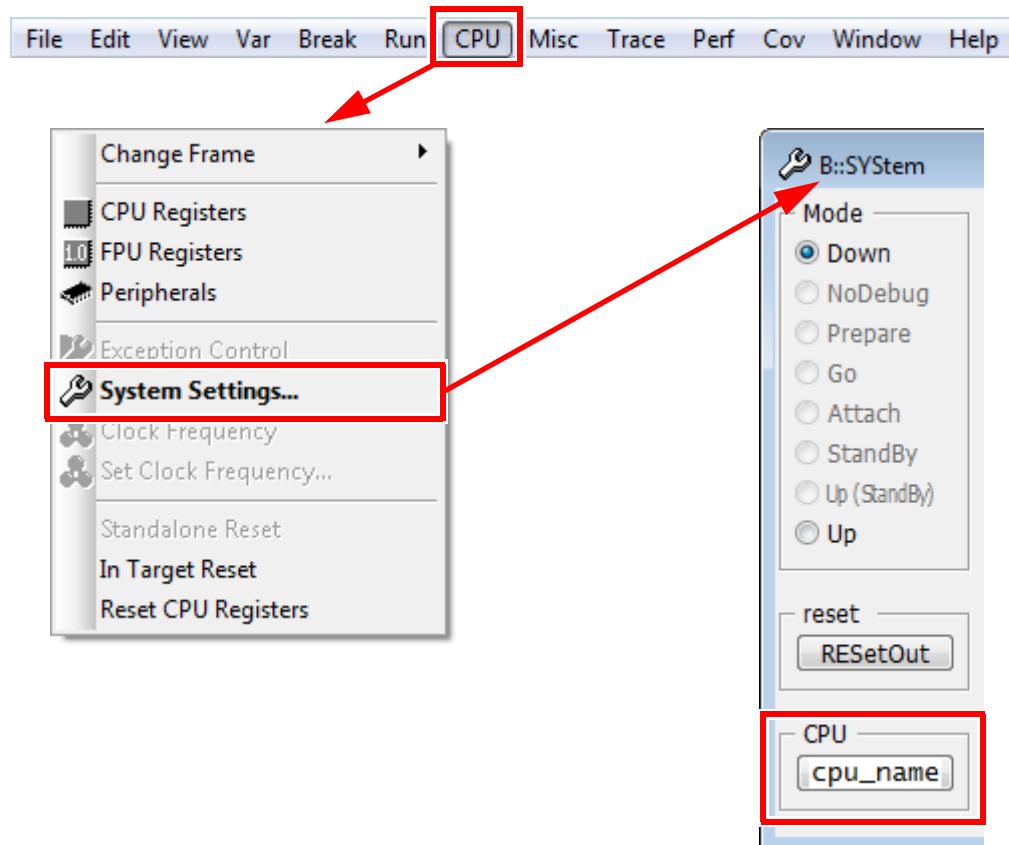
## To start the simulator, proceed as follows:

1. Select the device prompt for the Simulator and reset the system.

```
B:::  
RESet
```

The device prompt B:: is normally already selected in the [TRACE32 command line](#). If this is not the case, enter B:: to set the correct device prompt. The [RESet](#) command is only necessary if you do not start directly after booting TRACE32.

2. Specify the CPU specific settings.



```
SYStem.CPU <cpu_name>
```

The default values of all other options are set in such a way that it should be possible to work without modification. Please consider that this is probably not the best configuration for your target.

3. Enter debug mode.

```
SYStem.Up
```

This command resets the CPU and enters debug mode. After this command is executed it is possible to access memory and registers.

4. Load the program.

```
Data.LOAD.<file_format> <file> ; load program and symbols
```

See the **Data.LOAD** command reference for a list of supported file formats. If uncertain about the required format, try **Data.LOAD.auto**.

A detailed description of the **Data.LOAD** command and all available options is given in the reference guide.

5. Start-up example

A typical start sequence is shown below. This sequence can be written to a PRACTICE script file (\*.cmm, ASCII format) and executed with the command **DO <file>**.

```
B::: ; Select the ICD device prompt

WinCLEAR ; Clear all windows

SYStem.CPU <cpu_name> ; Select CPU type

SYStem.Up ; Reset the target and enter
           ; debug mode

Data.LOAD.<file_format> <file> ; Load the application

Register.Set pc main ; Set the PC to function main

PER.view ; Show clearly arranged
          ; peripherals in window *) */

List.Mix ; Open source code window *) */

Register.view /SpotLight ; Open register window *) */

Frame.view /Locals /Caller ; Open the stack frame with
                            ; local variables *) */

Var.Watch %Spotlight flags ast ; Open watch window for
                                ; variables *) */
```

\*) These commands open windows on the screen. The window position can be specified with the **WinPOS** command.

# Peripheral Simulation

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For more information, see “[API for TRACE32 Instruction Set Simulator](#)” (simulator\_api.pdf).

# Troubleshooting

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No information available.

# FAQ

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Please refer to <https://support.lauterbach.com/kb>.

# CPU specific SYStem Commands

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## SYStem.CPU

---

CPU type selection

Format: **SYStem.CPU <cpu>**

Selects the CPU type.

## SYStem.LOCK

---

Lock and tristate the debug port

Format: **SYStem.LOCK [ON | OFF]**

The command has no effect for the simulator.

## SYStem.MemAccess

---

Select run-time memory access method

Format: **SYStem.MemAccess Enable | StopAndGo | Denied**  
**SYStem.ACCESS (deprecated)**

**Enable** Memory access during program execution to target is enabled.

**Denied** Memory access during program execution to target is disabled.

**StopAndGo** Temporarily halts the core(s) to perform the memory access. Each stop takes some time depending on the speed of the JTAG port, the number of the assigned cores, and the operations that should be performed.

Format:	<b>SYStem.Mode &lt;mode&gt;</b>
	<b>SYStem.Down</b> (alias for SYStem.Mode Down) <b>SYStem.Up</b> (alias for SYStem.Mode Up)
<mode>:	<b>Down</b> <b>NoDebug</b> <b>Go</b> <b>Up</b>

Default: Down.

Selects the target operating mode.

<b>Down</b>	The CPU is in reset. Debug mode is not active. Default state and state after fatal errors.
<b>NoDebug</b>	The CPU is running. Debug mode is not active. Debug port is tristate. In this mode the target should behave as if the debugger is not connected.
<b>Go</b>	The CPU is running. Debug mode is active. After this command the CPU can be stopped with the break command or if any break condition occurs.
<b>Up</b>	The CPU is not in reset but halted. Debug mode is active. In this mode the CPU can be started and stopped. This is the most typical way to activate debugging.

If the mode **Go** is selected, this mode will be entered, but the control button in the **SYStem.state** window jumps to the mode **Up**.

<i>&lt;parameter&gt;</i> :	<b>DRPRE</b> <bits>
(JTAG):	<b>DRPOST</b> <bits>
	<b>IRPRE</b> <bits>
	<b>IRPOST</b> <bits>
	<b>TAPState</b> <state>
	<b>TCKLevel</b> <level>
	<b>TriState</b> [ON   OFF]
	<b>Slave</b> [ON   OFF]

The **SYStem.CONFIG** commands have no effect in Simulator. These commands describe the physical configuration at the JTAG port and the trace port of a multi-core hardware target. Since the simulator normally just simulates the instruction set, these commands will be ignored. Refer to the relevant [Processor Architecture Manual](#) in case you want to know the effect of these commands on a debugger.

## SYStem.Option.IMASKASM

Mask interrupts during assembler step

Format:	<b>SYStem.Option.IMASKASM</b> [ON   OFF]
---------	--

If enabled, the interrupt mask bits of the cpu will be set during assembler single-step operations. The interrupt routine is not executed during single-step operations. After single step the interrupt mask bits are restored to the value before the step.

## SYStem.Option.IMASKHLL

Mask interrupts during HLL step

Format:	<b>SYStem.Option.IMASKHLL</b> [ON   OFF]
---------	--

If enabled, the interrupt mask bits of the cpu will be set during HLL single-step operations. The interrupt routine is not executed during single-step operations. After single step the interrupt mask bits are restored to the value before the step.

The command asserts nRESET on the JTAG connector in the TRACE32 In-Circuit Debugger (ICD) but is ignored by the TRACE32 Instruction Set Simulator. However, the command is allowed in the simulator so that you can run scripts which have actually been made for the debugger. For more information about the effect in the debugger, refer to your [Processor Architecture Manual](#) (debugger\_<arch>.pdf).

# TrOnchip Commands

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## TrOnchip.state

Display on-chip trigger window

Format:	<b>TrOnchip.state</b>
---------	-----------------------

Opens the **TrOnchip.state** window.

## TrOnchip.RESet

Set on-chip trigger to default state

Format:	<b>TrOnchip.RESet</b>
---------	-----------------------

Sets the TrOnchip settings and trigger module to the default settings.

# Memory Classes

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## Overview

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Access Class	Description
C	CPU (Program and Data)
D	Data
P	Program
ED	Dualport Data
EP	Dualport Program

## **C:, E:, D:, P:, ED:, EP:**

---

### **C:, P: and D:**

This storage classes operate on the same physical memory. They are only used to be compatible with other emulation probes.

### **E:, EP: and ED:**

The E: prefix is used for accesses via dualport. The on-chip I/O-registers and the on-chip RAM area can be accessed via a special dualport mode (see MAP.SOnchip).

## Keywords for the Display

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<b>INT</b>	Occurrence of Interrupt
<b>psw_EP</b>	Processor Status Word: EP bit set
<b>psw_ID</b>	Processor Status Word: ID bit set
<b>psw_NP</b>	Processor Status Word: NP bit set
<b>psw_SAT</b>	Processor Status Word: SAT bit set
<b>praddress</b>	Instruction address
<b>prdata</b>	Instruction data
<b>prcycle</b>	Instruction cycle type