LAUTERBACH
DEVELOPMENT TOOLS

PowerIntegrator User's Guide

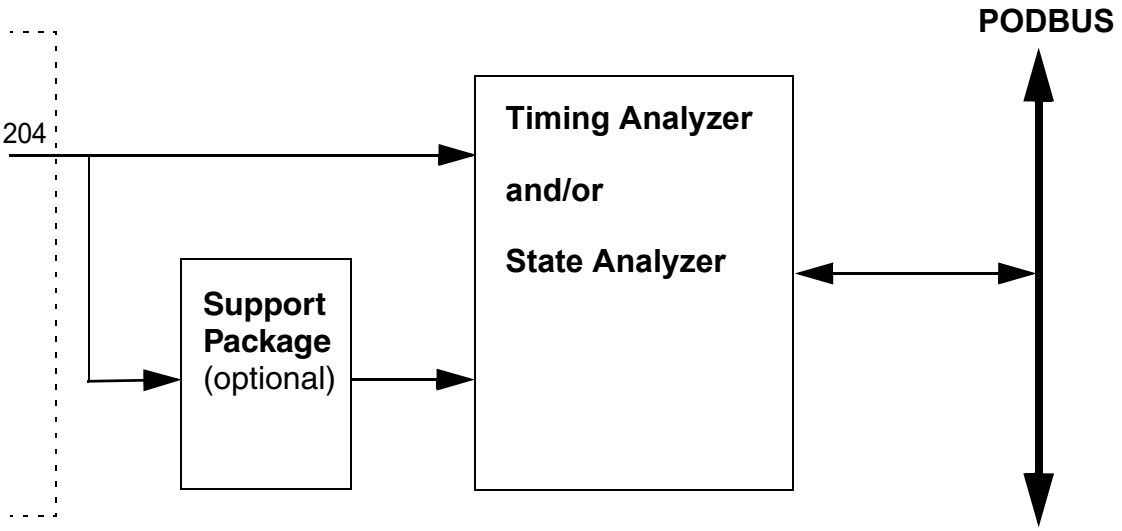
MANUAL

PowerIntegrator User’s Guide

Version 06-Jun-2024

Functional Units

The power integrator module consists of 2 parts: The timing/state analyzer and the optional support package.



The features of the Timing/State ANALYZER are:

Trace

In timing mode the analyzer can trace
- up to 102 channels with 500 MHz sampling rate
- up to 204 channels with 250 MHz sampling rate

In state mode the analyzer can trace
- up to 204 channels with 200 MHz sample rate
- up to 102 channels with 200 MHz sample rate, double data rate

The trace depth is 512 K records.
For 500 MHz mode and Double Data Mode it is 1024 K records.

Transient Recording

The sampling of the input lines is stored to the trace buffer by changes of the input level only. The total recording time depends on the occurrence of changes of the input signals. If the traced signals only changes once per ms, the total sampling time will be 512 s. The minimum trace time is 2 ms, which may appear if high-speed clock signals are recorded.

Mixed Trace

The input channels are split into two groups of 102 channels each. Each group can be used for timing or state mode recording.
Timing mode: Fixed sample rate of 250/500 MHz.
State mode: For each group a 1of2 qualifier selects the sampling clock out of the dedicated clock inputs (CLKA/B, CLKJ/K).
The sampled data are synchronized to the asynchronous trace information.

Simple Triggering

The simple trigger unit uses one trigger mask, which can include level or edge detection, a trigger filter and a trigger counter for generating a trigger event. Trigger programming can be done in the data window as easy as setting trigger conditions on a scope.

Support Package

This optional function gives the advantage of hardware based target-specific add-ons like:

- Channel reordering
- Address reconstruction based on FlowTrace information
- Address demultiplexing (DRAM, SDRAM busses …)
- Protocol analysis (JTAG, Serial, CAN, USB …)
- …

This allows recording and triggering on a higher level like protocol level.

Input/Output Lines

The PowerIntegrator offers 12 connectors with 16-data + 1-data/clock channels.

For using a 16+1channel probe (standard probe) only one of this connectors is used. For using a 32+2channel probe (MICTOR/SAMTEC probe) two of this connectors are used.

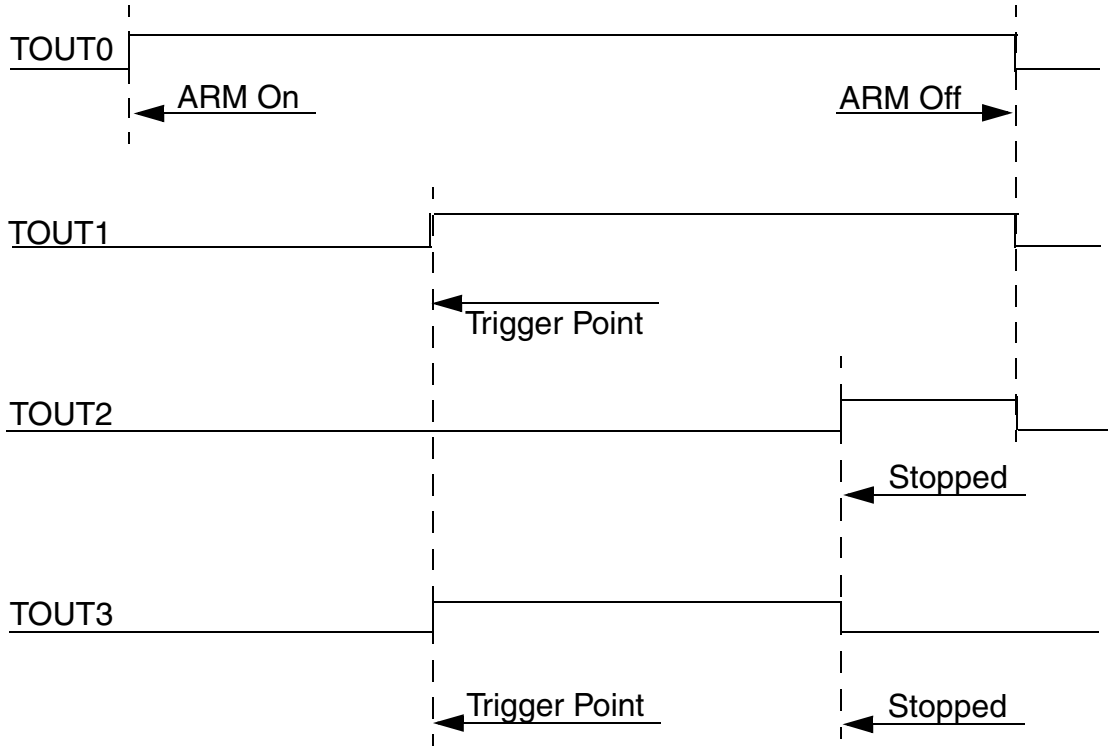
D.00..D.15	12 times 16-data channels
CLKA/B, **CLKJ/K**	4 times 1-data/clock channel • timing mode: used as data channel • state mode: used as data or clock channel
CLKC /D /E /F, **CLKL /M /N /O**	8 times 1-data channel
TOUT0..TOUT3 **OUTA..OUTD**	Trigger Output

ITRIGGER OUT Connector

Signal	Pin	Pin	Signal
TOUT0	1	2	GND
TOUT1	3	4	GND
TOUT2	5	6	GND
TOUT3	7	8	GND
OUTA	9	10	GND
OUTB	11	12	GND
OUTC	13	14	GND
OUTD	15	16	GND

Counting starts beside the power connector, bottom row at GND.

OUTA, OUTB, OUTC OUTD trigger outputs can be forced by the complex trigger unit



Probe Connector Assignments

Mictor Probe

Signal	Pin	Pin	Signal
N/C	1	2	N/C
GND	3	4	N/C
CLK0	5	6	CLK1
D15	7	8	D31
D14	9	10	D30
D13	11	12	D29
D12	13	14	D28
D11	15	16	D27
D10	17	18	D26
D9	19	20	D25
D8	21	22	D24
D7	23	24	D23
D6	25	26	D22
D5	27	28	D21
D4	29	30	D20
D3	31	32	D19
D2	33	34	D18
D1	35	36	D17
D0	37	38	D16

Mictor Difference Probe

Signal	Pin	Pin	Signal
N/C	1	2	N/C
GND	3	4	N/C
CLK+	5	6	CLK-
D15+	7	8	D15-
D14+	9	10	D14-
D13+	11	12	D13-
D12+	13	14	D12-
D11+	15	16	D11-
D10+	17	18	D10-
D9+	19	20	D9-
D8+	21	22	D8-
D7+	23	24	D7-
D6+	25	26	D6-
D5+	27	28	D5-
D4+	29	30	D4-
D3+	31	32	D3-
D2+	33	34	D2-
D1+	35	36	D1-
D0+	37	38	D0-

Standard Probe

Signal	Pin	Pin	Signal
N/C	1	2	N/C
CLK	3	4	D15
D14	5	6	D13
D12	7	8	D11
D10	9	10	D9
D8	11	12	D7
D6	13	14	D5
D4	15	16	D3
D2	17	18	D1
D0	19	20	GND

Signal	Pin	Pin	Signal
GND	1	2	GND
N/C	3	4	N/C
GND	5	6	GND
D16	7	8	D0
GND	9	10	GND
D17	11	12	D1
GND	13	14	GND
D18	15	16	D2
GND	17	18	GND
D19	19	20	D3
GND	21	22	GND
D20	23	24	D4
GND	25	26	GND
D21	27	28	D5
GND	29	30	GND
D22	31	32	D6
GND	33	34	GND
D23	35	36	D7
GND	37	38	GND
D24	39	40	D8
GND	41	42	GND
D25	43	44	D9
GND	45	46	GND
D26	47	48	D10
GND	49	50	GND
D27	51	52	D11
GND	53	54	GND
D28	55	56	D12
GND	57	58	GND
D29	59	60	D13
GND	61	62	GND
D30	63	64	D14
GND	65	66	GND
D31	67	68	D15
GND	69	70	GND
N/C	71	72	N/C
GND	73	74	GND
N/C	75	76	N/C
GND	77	78	GND
CLK1	79	80	CLK0
GND	81	82	GND
N/C	83	84	N/C
GND	85	86	GND
N/C	87	88	N/C
GND	89	90	GND
N/C	91	92	N/C
GND	93	94	GND
GND	95	96	GND
N/C	97	98	N/C
N/C	99	100	N/C

Initialization

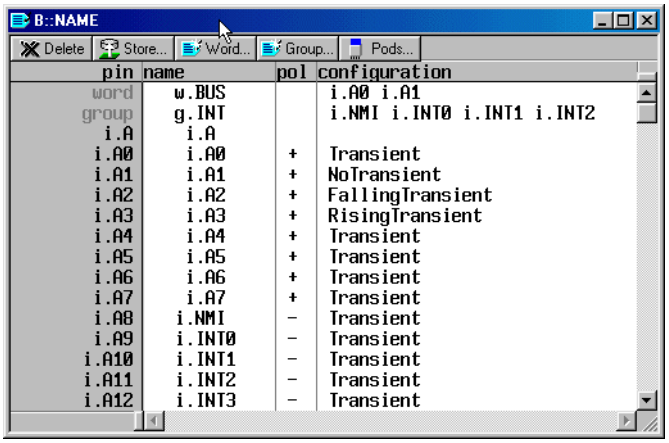
RESet	Initialize integrator
STOre	Save setup

Signal Names

The **NAME** function generates logical names for input lines and additionally the polarity of the signal. In the trigger program of the integrator, logical definitions can be used instead of physical pin names.

The **NAME** function also configures the transient detection type. It can be set to **NoTransient**, **Transient**, **FallingTransient** or **RisingTransient**.

NAME.list	Display logical names
NAME.RESet	Erase logical names for input pins
NAME.Set	Define logical names for input pins
NAME.Group	Define logical names for input groups
NAME.Word	Define logical names for busses
NAME.Delete	Erase logical groups or words for input pins

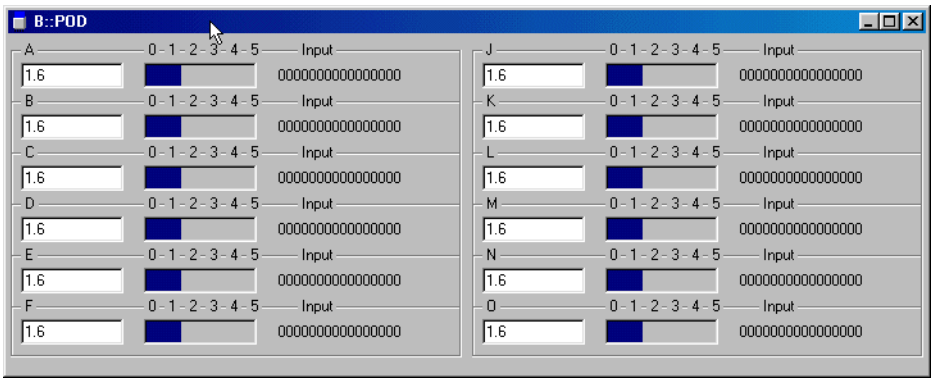


POD Threshold Levels and Signal Display

The **POD** function defines the threshold level for the input lines. Each probe (16 data+1 Clock) can be configured for different threshold levels in a range of 0 to 5 V.

The POD window also displays the selected threshold levels, the current probe signal levels and the clock frequency of the selected target state clock (StatePLL modes only).

POD.state	Display threshold level
POD.Level	Select threshold level
POD.RESet	Set to default



Sampling Modes

The PowerIntegrator supports four kinds of sampling modes:

1. Timing Mode

   Probe signals are sampled with a fixed frequency of 250 MHz (204 channels) or 500 MHz (102 channels).

2. State ModePLL

   Probe signals are sampled on the **rising or falling** edge of a target clock signal (CLKA, CLKB, CLKJ, CLKK). The selected target clock feeds an PowerIntegrator internal PLL which gives the option to vary the sampling time in a range of -3 … +6 ns in steps of 250 ps. To make the PLL circuit work the target clock has to be active always and it has to run on a fixed frequency in the range of 6 … 200 MHz.

3. State Mode Double Data Rate

   like State ModePLL, but data is sampled on the **rising and falling** clock edge. Channel count is reduced to 102.

4. State Mode

   A kind of State Mode for pulsed clock signals. Probe signals are sampled on the **rising or falling** edge of a target clock signal (CLKA, CLKB, CLKJ, CLKK). The selected clock is sampled with 500 MHz (2 ns resolution) to detect the clock edges. Probe signals are sampled with 250 MHz if a clock edge was detected. This method works in the range of 0 … 133 MHz.

Sampling Mode Configurations

The 204 input channels are split into two groups of 102 channels each. To give the maximum flexibility this groups can be combined and configured in different modes.

Group ABCDEF	Group JKLMNO	Mode	Probes	Channels Number
500MHz		Timing Mode 500 MHz	ABCDEF	102
Fixed500MHz		Fixed sampling with 500 MHz	ABCDEF	102 with 500 Mhz
250MHz	250MHz	Timing Mode 250 MHz	all	204
250MHz	State	Timing Mode 250 MHz State Mode	ABCDEF JKLMNO	102 102
State	250MHz	State Mode Timing Mode 250 MHz	ABCDEF JKLMNO	102 102
State	State	State Mode State Mode	ABCDEF JKLMNO	102 102
StatePLL	250MHz	State Mode PLL Timing Mode 250 MHz	ABCDEF JKLMNO	102 102 **
StatePLL	State	State Mode PLL State Mode	ABCDEF JKLMNO	102 102 **
StatePLL	StatePLL	State Mode PLL State Mode PLL	ABCDEF JKLMNO	102 102
StatePLL, DDR		State Mode PLL	ABCDEF	102, DDR
StatePLLBoth		State Mode PLL	all	204

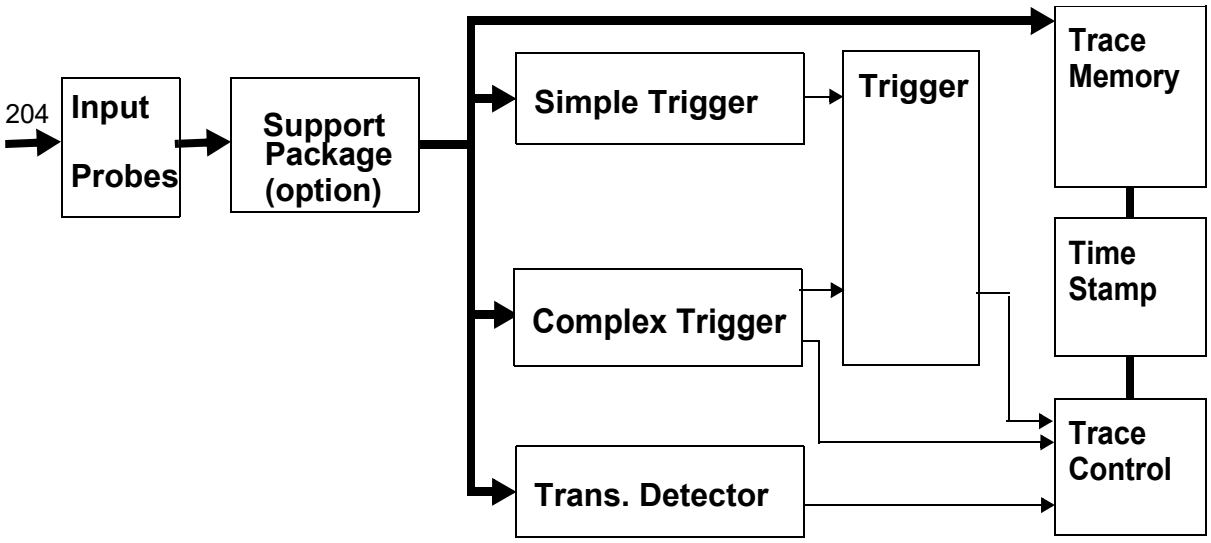
Integrator.ABCDEF 500MHZ	Timing Mode 500 MHz, group ABCDEF only
Integrator.ABCDEF Fixed500MHZ	Timing Mode, fixed sampling with 50 0MHz, group ABCDEF only
Integrator.ABCDEF 250MHZ	Timing Mode 250 MHz
Integrator.ABCDEF State	State Mode
Integrator.ABCDEF StatePLL	State Mode PLL
Integrator.ABCDEF StatePLLBoth	State Mode PLL, group ABCDEF **and** JKLMNO sampled with CLKA or CLKB
Integrator.JKLMNO 250MHZ	Timing Mode 250MHz
Integrator.JKLMNO State	State Mode
Integrator.JKLMNO StatePLL	State Mode PLL

Sampling Clock Configuration

For State-Mode and State-PLL-Mode various clock settings are supported.

1. Clock Selection: For each group (ABCDEF, JKLMNO) a 1 of 2 qualifier selects the sampling clock out of the dedicated clock inputs (CLKA/B, CLKJ/K).
2. Edge Selection: For each clock (CLKA/B, CLKJ/K) the rising or falling edge can be selected. Additional both edges can be selected for clock CLKA/B to support Double Data Rate sampling on the rising and falling clock edge.
3. State Mode PLL setting: For each clock (CLKA/B, CLKJ/K) the sampling clock delay can be defined in a range of **-3 … +6 ns** in steps of **250 ps**.

Integrator.ABCDEF CLKA	clock A select
Integrator.ABCDEF CLKB	clock B select
Integrator.ABCDEF Falling	sample on falling clock edge
Integrator.ABCDEF Rising	sample on rising clock edge
Integrator.ABCDEF DDR	sample on rising and falling clock edge
Integrator.ABCDEF SAMPLE	sampling delay of selected clock
Integrator.JKLMNO CLKJ	clock J select
Integrator.JKLMNO CLKK	clock K select
Integrator.JKLMNO Falling	sample on falling clock edge
Integrator.JKLMNO Rising	sample on rising clock edge
Integrator.JKLMNO SAMPLE	sampling delay of selected clock (-3 … +6 ns in steps of 250 ps)



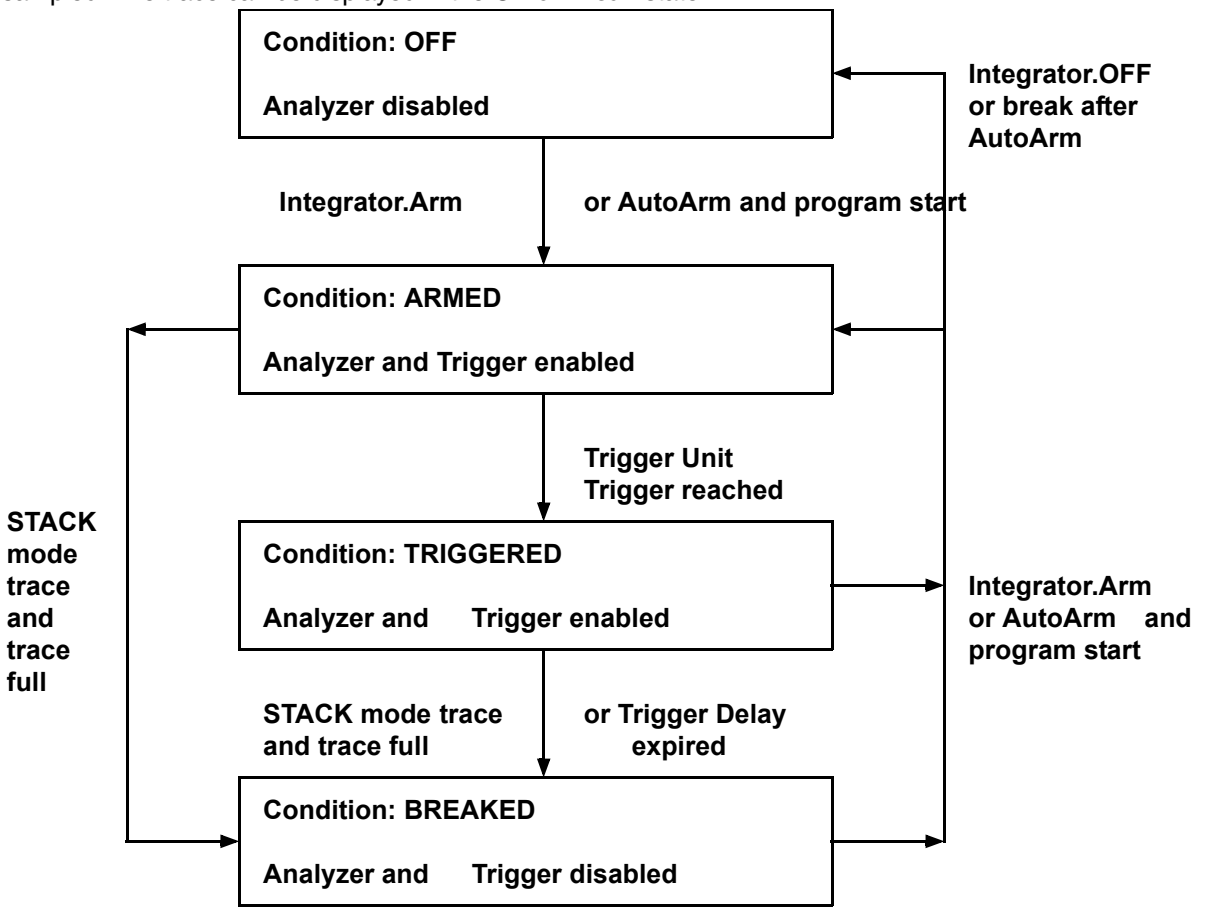
Timing Analyzer Schematics

Input Control

Support Package	Target-specific adaption (FlowTrace address reconstruction, SDRAM address demultiplexing …)
Trace Memory	The trace memory stores all data from the input line.
Timestamp	As the trace memory samples only differences to the previous state, a timestamp memory is needed to sample the time information.
Transient Detection	The circuit detects all state changes of input lines.
Trace Control	The trace control unit generates the control signals for the trace and the timestamp memory, depending on the output of transient detection circuit and complex trigger.
Simple Trigger	The simple trigger system has one trigger pattern detection for 204 signals, a trigger filter and a trigger counter.
Complex Trigger	Sequencer controlled trigger system, used for complex trigger conditions and selective tracing.

Basic Trace Control

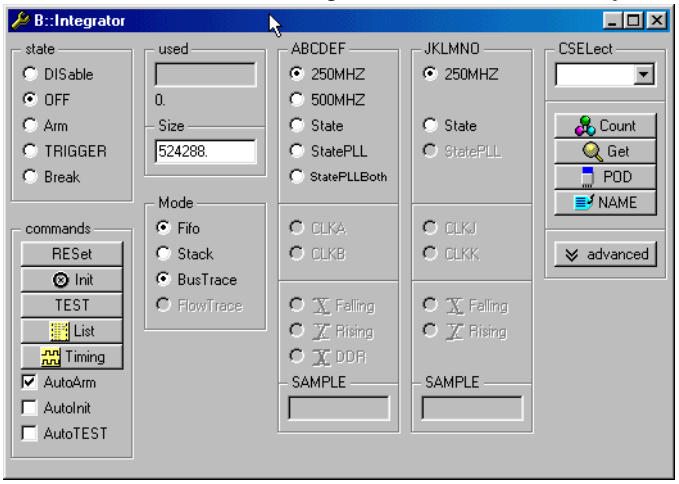
The trace buffer can either sample information or display the results. In the **Arm** state the input lines are sampled. The trace can be displayed in the **Off** or **Break** state.



Analyzer Operation States

Integrator.state	Show the integrator state window
Integrator.OFF	Turn off the integrator
Integrator.Arm	Arm the integrator
Integrator.TRIGGER	Trigger the integrator
Integrator.Init	Clear the trace buffer and restart the trigger unit and the counters.
Integrator.SnapShot	Combination of **Init** and **Arm**
Integrator.RESet	Restore all setting to the default values

All basic functions of the integrator can be controlled by the integrator state window.



The window displays information about the actual state, the mode and the number of records in the trace buffer. It also shows information about the trigger unit, like logical trigger level, counters and flags.

triggered	The integrator is waiting for the expiration of the trigger delay.
break	The trigger unit has stopped the recording
records	Displays the used records in the trace buffer

Operation Modes

The behavior characteristics of the integrator can be changed by the **Integrator.Mode** command. The basic operation mode for the trace storage can be FIFO or STACK.

Integrator.Mode Fifo	FIFO operation mode, integrator records the last cycles before stop recording
Integrator.Mode Stack	STACK operation mode, the integrator stops recording, when the trace buffer is full

Automatic Trace Control

To simplify the controlling of the integrator, different automatic control options are available. As a default the **AutoArm** option is active. This means that the integrator will be armed automatically when the user program is started, and switches to off, after stopping the real-time emulation.

Integrator.AutoArm	Arm the integrator before starting the user program, switch off after stopping
Integrator.AutoInit	Init the integrator before starting the user program
Integrator.SelfArm	Automatically arm the integrator after all windows have been updated

The combination of **AutoTEST** and **Stack** operation mode can be used for making random samples and displaying the results continuously:

```
B:Integrator.Mode AutoTest ON

B:Integrator.Mode Stack

B:Integrator.List

B:Go
```

The result will be a continuously updated trace list window, which shows the last sampled signals.

Display Commands

The trace buffer can be displayed in tabular form or in graphical form.

Integrator.List	Displays trace in table format
Integrator.Timing	Displays channels as waveform graphics
Integrator.Get	Displays the input signal level and activity
Integrator.View	Displays one line
Integrator.Chart	Displays values graphically
Integrator.PROTOcol.'*'	Displays protocols like CAN, I2C, etc.
Integrator.STATistic	Displays trace statistics
COVerage	Displays code coverage

The integrator GET command displays the actual input state and activity.

high Signal stays high

low Signal stay low

hilo Signal is toggling

B::Integrator.get

record	i.a0	i.a1	i.a2	i.a3	i.a4	i.a5	i.a6	i.a7	i.a8	i.a9	i.a10	i.a11	i.a12
direct	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW

i.a13	i.a14	i.a15	i.b0	i.b1	i.b2	i.b3	i.b4	i.b5	i.b6	i.b7	i.b8	i.b9	i.b10
LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW

i.b11	i.b12	i.b13	i.b14	i.b15	i.c0	i.c1	i.c2	i.c3	i.c4	i.c5	i.c6	i.c7	i.c8
LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW

i.c9	i.c10	i.c11	i.c12	i.c13	i.c14	i.c15	i.d0	i.d1	i.d2	i.d3	i.d4	i.d5	i.d6
LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW

i.d7	i.d8	i.d9	i.d10	i.d11	i.d12	i.d13	i.d14	i.d15	i.e0	i.e1	i.e2	i.e3	i.e4
LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW

i.e5	i.e6	i.e7	i.e8	i.e9	i.e10	i.e11	i.e12	i.e13	i.e14	i.e15	i.f0	i.f1	i.f2
LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW

i.f3	i.f4	i.f5	i.f6	i.f7	i.f8	i.f9	i.f10	i.f11	i.f12	i.f13	i.f14	i.f15	i.j0
LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW

i.j1	i.j2	i.j3	i.j4	i.j5	i.j6	i.j7	i.j8	i.j9	i.j10	i.j11	i.j12	i.j13	i.j14
LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW

i.j15	i.k0	i.k1	i.k2	i.k3	i.k4	i.k5	i.k6	i.k7	i.k8	i.k9	i.k10	i.k11	i.k12
LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW

i.k13	i.k14	i.k15	i.l0	i.l1	i.l2	i.l3	i.l4	i.l5	i.l6	i.l7	i.l8	i.l9	i.l10
LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW

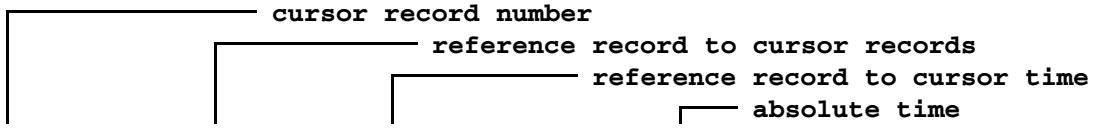
i.l11	i.l12	i.l13	i.l14	i.l15	i.m0	i.m1	i.m2	i.m3	i.m4	i.m5	i.m6	i.m7	i.m8
LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW

i.m9	i.m10	i.m11	i.m12	i.m13	i.m14	i.m15	i.n0	i.n1	i.n2	i.n3	i.n4	i.n5	i.n6
LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW

i.n7	i.n8	i.n9	i.n10	i.n11	i.n12	i.n13	i.n14	i.n15	i.o0	i.o1	i.o2	i.o3	i.o4
LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW

i.o5	i.o6	i.o7	i.o8	i.o9	i.o10	i.o11	i.o12	i.o13	i.o14	i.o15	i.clka	i.clkb

The integrator list window can display the contents of the trace memory in several formats. The displayed columns and information can be configured very flexible. The command **Integrator.List** without arguments creates a window with an assortment of usually interesting parts of the trace.




```
+00024  C-R: -00001    -0.220us       C-Z:  +3.534s
```

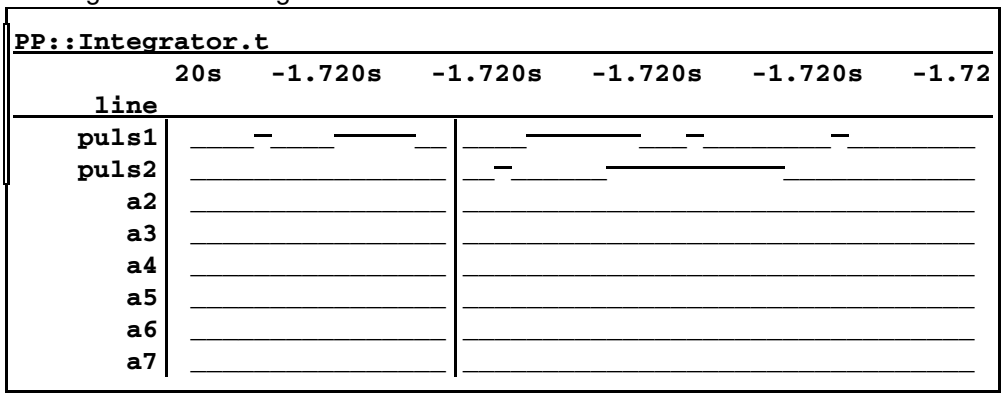
```
B::I.l i.a0 i.int0  w.test ti.ref
   record x.0  int0 st ti.ref
-00000029          00 -201.130us
-00000028          00 -200.900us
-00000027          00 -200.690us
-00000026          00 -200.460us
-00000025          00   -0.230us
-00000024          00    0.000
-00000023          00    0.220us
-00000022          00    0.440us
-00000021          00    0.660us
-00000020          00    0.880us
-00000019          00  201.120us
-00000018          00  201.340us
-00000017          00  201.560us
-00000016          00  201.780us
-00000015          00  202.000us
-00000014          00  202.220us
-00000013          00  402.450us
-00000012          00  402.680us
-00000011          00  402.890us
-00000010          00  403.120us
-00000009          00  403.330us
-00000008          00  403.560us
-00000007          00  603.790us
```

Each entry is classified by a record number. Usually the most recent entry is -1. If a trigger point is available, it is marked with a "T" and its record number is 0.

```
PP::I.l a0  a1 ti.ref ti.fore
 record a0 a1 ti.ref     ti.fore
+032754 |  |    -10.300us   20.000ns
+032755 |  |    -10.280us   40.000ns
+032756 |  |    -10.240us   20.000ns
+032757 |  |    -10.220us   40.000ns
+032758 |  |    -10.180us   20.000ns
+032759 |  |    -10.160us   40.000ns
+032760 |  |    -10.120us   20.000ns
+032761 |  |    -10.100us   40.000ns
+032762 |  |    -10.060us   20.000ns
+032763 |  |    -10.040us   10.020us
+032764 |  |    -20.000ns   20.000ns
R032765 |--|  -   0.000  -   1.695s
+032766 |  |     1.695s
```

The most used display command is the timing diagram. Timing displays can be zoomed.

The left mouse bottom set the cursor. By pressing the mouse, a new zoom window can be selected. Fast zooming and de-zooming can be done with the middle mouse buttom.



The Integrator.View shows only one frame of the trace storage.

```
PP::I.view w.bus g.int  /track
record  w.bus i.nmi  i.int0  i.int1
-078570 00
x.int2
```

```
PP::Integrator.t
                 ms      -39.285ms      -39.28
        line
      x.NMI-◄►
     x.INT0-◄►
     x.INT1-◄►
     x.INT2-◄►
       w.BUS◄►
        x.0#◄►
        x.1#◄►
```

```
PI::Integrator.Chart.Draw , %Signed w.test
                  -190.000ms  -180.000ms  -170.000ms  -160.000ms   -150.0
          range
       00000030
       00000020
       00000010
       00000000
      -00000010
      -00000020
      -00000030
```

Search and Compare

Several commands allow to search for specific events, or compare the trace against a reference:

Integrator.GOTO	Track the display window to a new record
Integrator.Find	Search for records matching the pattern
Integrator.ComPare	Compare two traces or the trace buffer against a file
Integrator.REF	Set reference record for timing measurements

The **Find** command allows to search for the occurrence of a data pattern:

```
Integrator.Find , data w.test:0x55      ; search for matching data on
                                        ; probe
                                        ; A is 55 h

Integrator.Find , Integrator.puls1      ; search for rising edge of
on at -1. Integrator.nmi off            ; the puls1 signal

Integrator.Find , w.dat 0x5--0x44 or    ; search for different data bytes
w.dat 0xff

Integrator.Find                         ; search for next occurrence
```

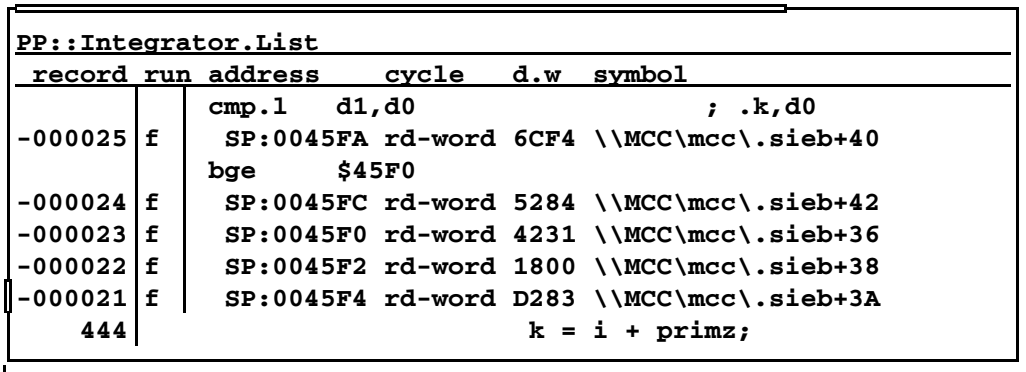
The **ComPare** command can compare the current trace against a reference trace saved on disk:

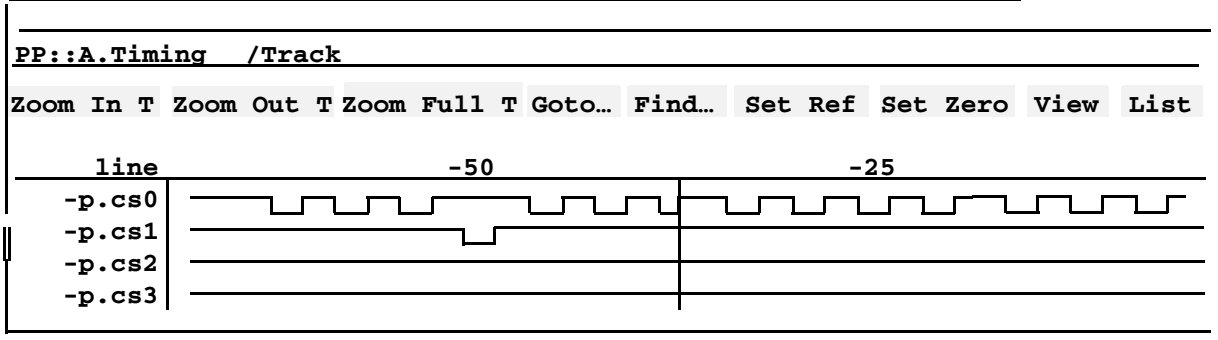
```
Integrator.LOAD x1

Integrator.List /track          ; display current trace

Integrator.List /track          ; display reference trace
/file

Integrator.ComPare , , i.a0     ; compare two lines against
i.a0 /file                      ; file (complete trace memory)

Integrator.ComPare              ; compare next entries
```

Tracking

The tracking option forces all port integrator windows, which are in tracking mode (option **/Track**), to pan to the same position like the reference window. The reference window can be any integrator display window from the state integrator, the timing integrator or the port integrator. The reference point is fixed to the absolute time. Every integrator system has an independent, but correlated, timestamp unit. The tracking function can be used also for displaying port integrator windows with different zoom rates. Tracking can also be done by drag-and-drop.

```
Integrator.Timing /Track       ; define tracking window for port
Integrator.List                ; integrator
```





Real-Time Displays

The information recorded by the integrator can be displayed, while the integrator is sampling information.

Integrator.SelfArm	Arm the integrator after all windows have been updated

The command **AutoTEST** can be used to make random samples and show the results continuously.

Saving Trace Buffers

The contents of the trace buffer can be saved on disk and recalled later. The recalled trace buffer can be accessed by all regular integrator commands by adding the option **/FILE**.

Integrator.SAVE	Save the contents of the trace buffer
Integrator.EXPORT	Exports trace data to VHDL file
Integrator.LOAD	Load a saved trace buffer as a reference

Saving a part of the trace buffer can be done by the following command:

```
Integrator.SAVE test (-1000.)--0x0
```

Exporting signals of the trace buffer to a VHDL Wait file can be done by the following command:

```
Integrator.EXPORT test i.a0 i.a1 i.a2 w.test
```

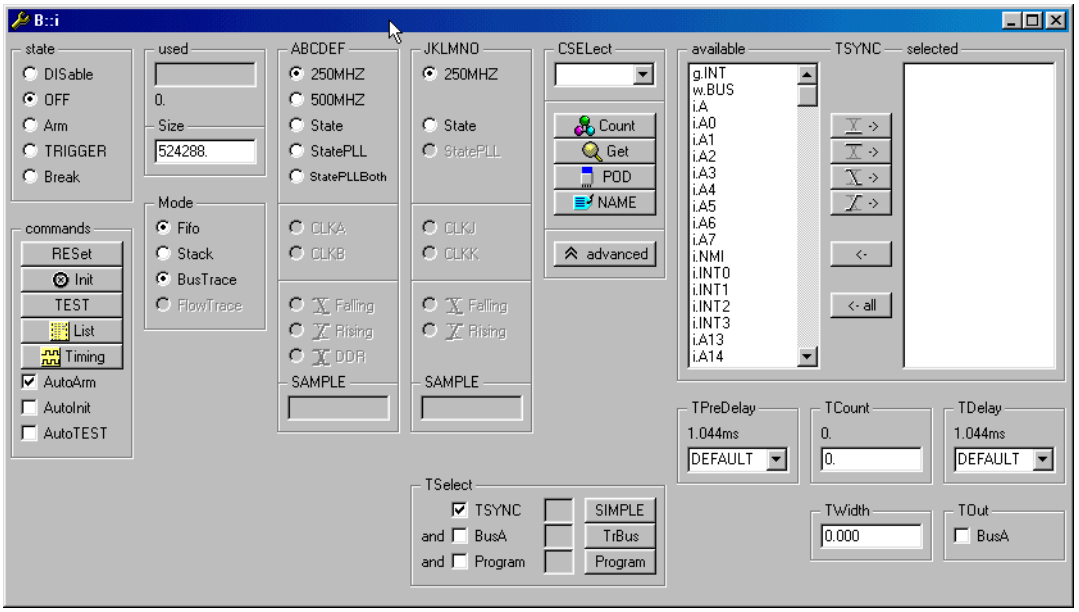
The trace can be recalled and viewed again by the **Load** command:

```
Integrator.LOAD test

w.Integrator.List /file
```

Comparing the file against a new record is possible with the **ComPare** command:

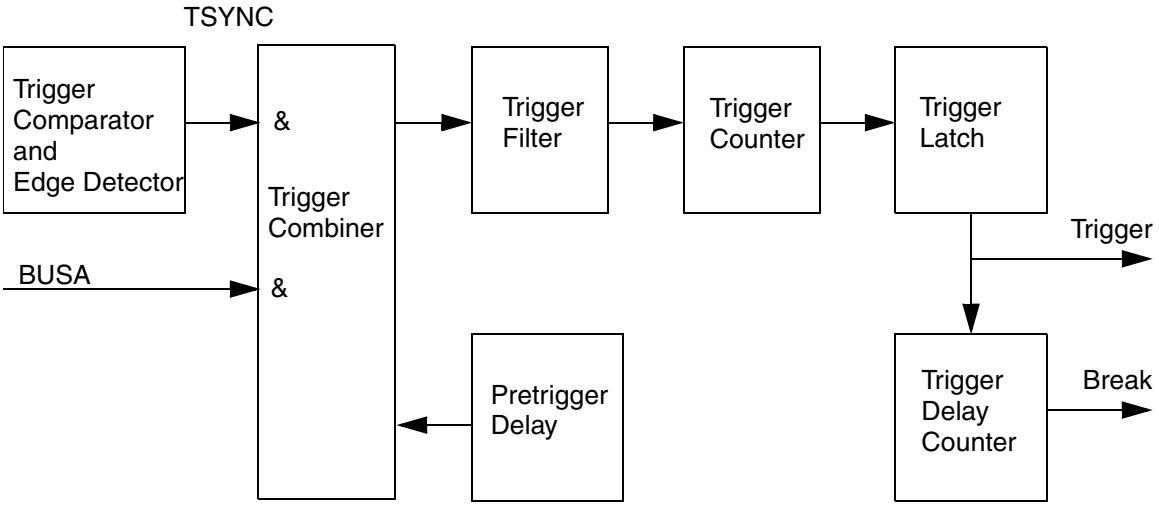
```
Integrator.LOAD test

Integrator.ComPare (-1000.)--0x0 -1000. C0 C1 /file
```

Simple Trigger



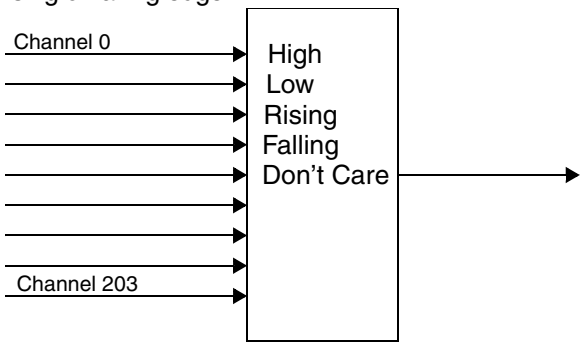
Function

The trigger concept allows fast programming of trigger events related to the application.

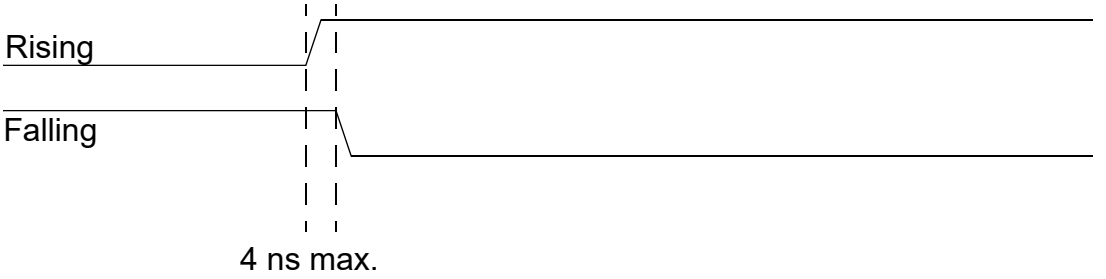


Trigger Word

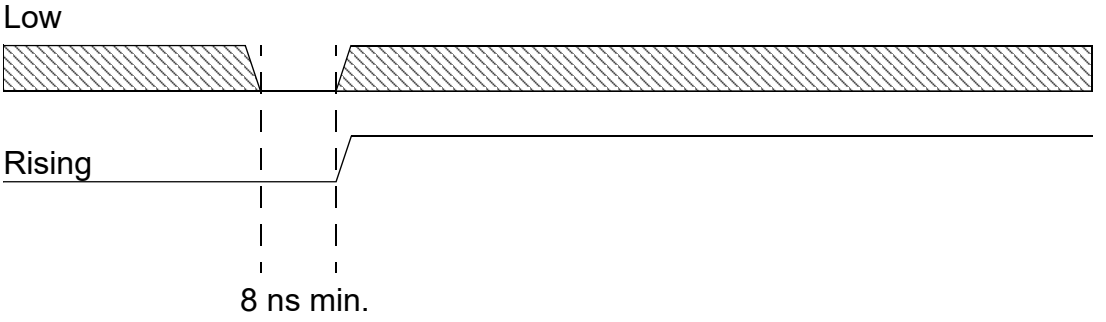
The trigger word can be generated out of the 204 port channels. Each signal can be qualified as high, low, rising or falling edge.



More than 1 edge can be combined to a trigger word. To detect a valid combination of edges, the edges must have a max. skew of 4 ns.



Edges and state signals can be combined. The state signal must be stable 4 ns before the edge. The sampling of the state signal is guaranteed before the edge is detected.



Trigger Combiner

The trigger signals from the trigger word selector and the bus trigger signals (BUSA) can be combined to form a valid trigger signals. The combining is made on a **and** basis. Therefore trigger conditions can be qualified by bus trigger signals generated by the state analyzer or other systems.

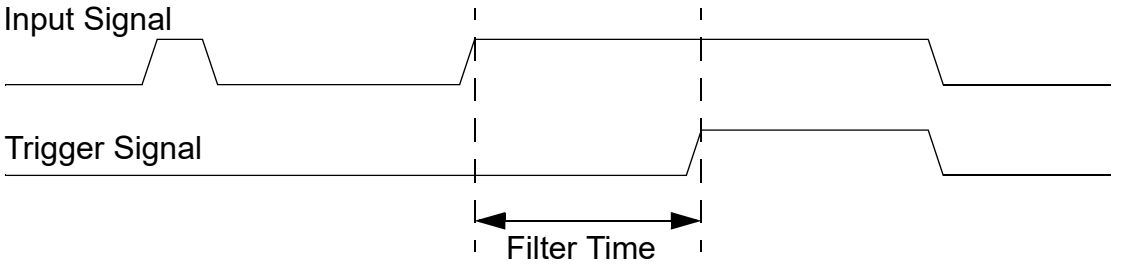
The trigger or break signals from the debugger can be used to stop the PowerIntegrator and vice versa.

Trigger PreDelay

To avoid nearly empty trace buffers, the trigger system can activated delayed, the trace buffer is filled partly then.

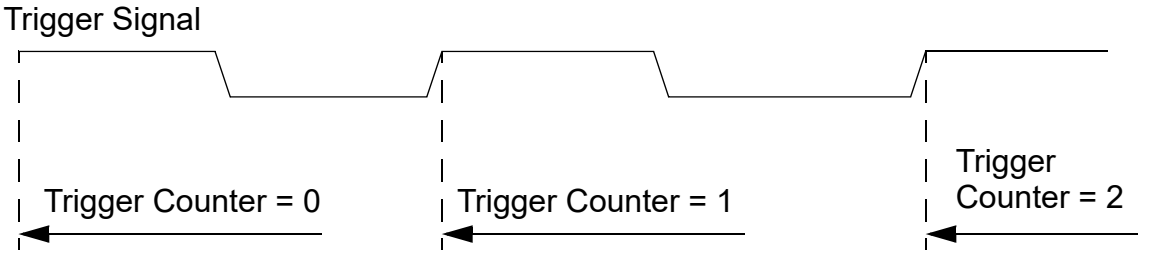
Trigger Filter

The trigger filter selects valid trigger signals from glitches or runts on the input lines. It can be used to trigger on a minimum pulse width. Trigger filtering should not be used, if edge triggering is selected in the trigger word qualifier.



Trigger Counter

The trigger counter delays the triggering on the n-th event of a valid trigger condition. The value zero means triggering immediately, one on the first occurrence of the trigger event.



Trigger Delay

After the trigger condition has been latched, a trigger delay is used before stopping the PowerIntegrator. The delay can be defined with an absolute time (1 ms to 10 s) or in percentage of the trace storage.

Trigger Outputs

When reaching the trigger state (trigger latch is true), other systems like oscilloscopes can be triggered by the PowerIntegrator. The trigger output signals are true as long as the PowerIntegrator is running and the trigger latch has been set.

The PowerIntegrator can trigger a debugger or PowerProbe directly by using the **Integrator.TOut** command.

See also: **Trigger Out Connector**

Trigger Setting

Integrator.TView	Trigger state window
Integrator.TSYNC	Selects trigger source and level/edge mode
Integrator.TPreDelay	Select pre trigger delay
Integrator.TWidth	Select minimum trigger width
Integrator.TCount	Sets trigger counter
Integrator.TDelay	Defines trigger delay
Integrator.TOut	Activate Trigger Output Signals

Using the Trigger Delay and Predelay

The trigger delay is used for the adjustment of the trigger point inside the whole sampling.

Integrator.TDelay	Define the trigger delay
Integrator.TPreDelay	Define the trigger predelay

The selected value is the percentage of trace memory records which will be sampled respectively overwritten after the occurrence of the **trigger event** released from the trigger unit.

The actual value could be less if the sampling is **switched to off manually** by the user before the maximum value is reached.

The default trigger delay is 0. In this case the trigger point is at the last sampled record in the trace memory.

e.g. 0 = the sampling stops immediately

50 = up to 256K records will be recorded

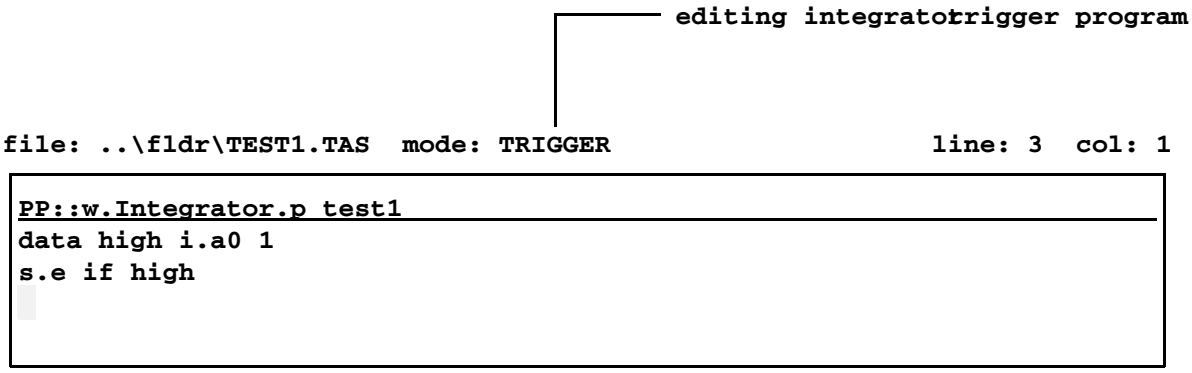
100 = up to all 512K records will be recorded

```
Integrator.TDelay 0%

0                                                    512K sampled records
└──────────────────────────────────────────────────────┘
                                                      T
                                                       trigger point

Integrator.TDelay 50%

0                                                    512K sampled records
└──────────────────────┘
                       T
                       trigger point

Integrator.TDelay 100%

0                                                    512K sampled records
T──────────────────────────────────────────────────────┘
trigger point
```

Complex Trigger

If the trigger unit is not programmed, the integrator samples all signals on the input probe. For selective recording or complex triggering, the trigger unit must be programmed. The command **Integrator.Program** opens a special editor window for entering an integrator trigger program. The input is guided by softkeys and the context selective help.

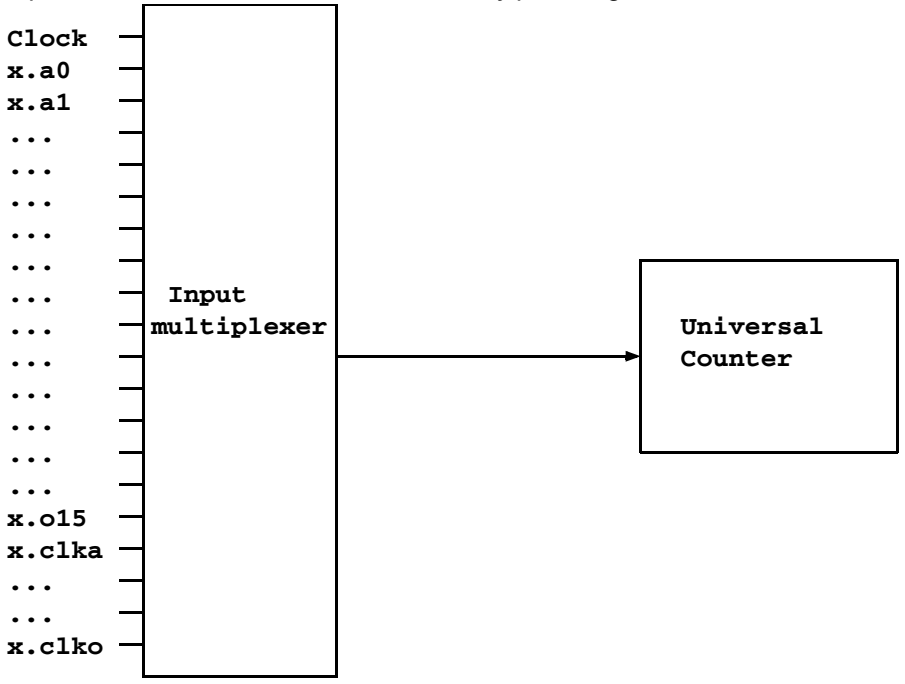
Integrator.Program	Write a program for the trigger unit interactive with softkey support
Integrator.ReProgram	Load a program into the trigger unit without interactive window
Integrator.state	Displays the name of the trigger program and the values of counters and flags



If the editing of the program is complete, a short click on the right mouse button (MS-DOS) or a double click on the left button (X-Windows/MS-WINDOWS) starts the trigger language compiler. When the compilation is error-free, the "DRAFT" message in the state line will disappear. The name of the program is shown in the integrator state window. The integrator is now ready to perform the programmed actions.

Function

The universal counter is the logic measurement system for sampling of pulses and frequencies. The input multiplexer enables the counter to measure any probe signal.



Principle of Universal Counter

The count ranges are:

frequency:	0 … 200 MHz	
Puls width:	100 ns … 300 days	
Period:	100 ns … 300 days	
Events:	2.8 * 10E+14	max. rate 10 MHz

The input signal is selected with the function **Count.Select**. The function **Count.Mode** is used to change the counter mode and the **Count.Gate** function defines the gate time. Frequency and event analyzing may be qualified by the foreground running signal.

If there is no event counting, it will be possible to activate more than one count window. Every window represents a separate counter. For example it is possible to check the clock frequency and the puls width on some probe inputs simultaneously.

Integrator.CSELelect	Select counter signal

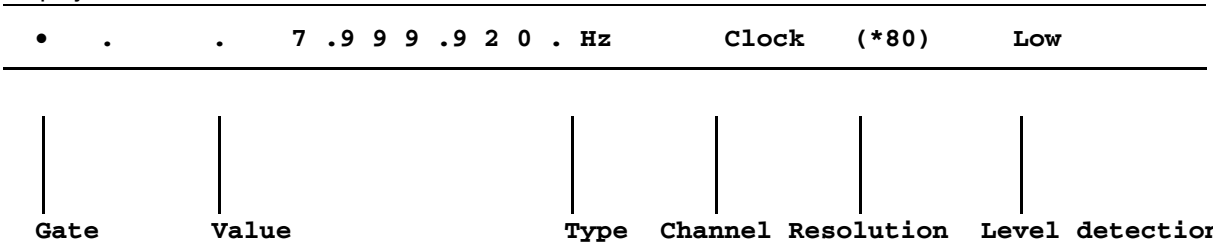
Example

```
Integrator.CSEL                ; selects signal a0
Integrator.a0

C.Select Integrator.a0         ; selects signal
```

Level Display

If there is no signal (frequency is zero), the level of the input signal will be displayed (high or low level).

Display Window



Count.state	Display value and setup
Count.RESet	Initialize counter setup
Count.Init	Initialize counter
Count.Mode	Select counter mode
Count.Select	Select input signal
Count.Gate	Select gate time
Count.Enable	Select run time
Count.PROfile	Display profile