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DEVELOPMENT TOOLS

PowerIntegrator State Trace Application Note

MANUAL

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State Recording

State Recording is the appropriate method to trace synchronous bus protocols. A typical application is a clocked SDRAM bus where valid data is driven on the bus relative to the SDRAM clock.

Of course State Recording also can be used for a standard RAM interface where address, data and strobe information is valid on each rising edge of a chip select.

State Recording means:

Only the change in state of a single reference signal enables the trace recording.

The setup for State Recording requires:

- selection of a **reference signal**
- selection of the **change in state type**
- definition of a **data sampling offset**

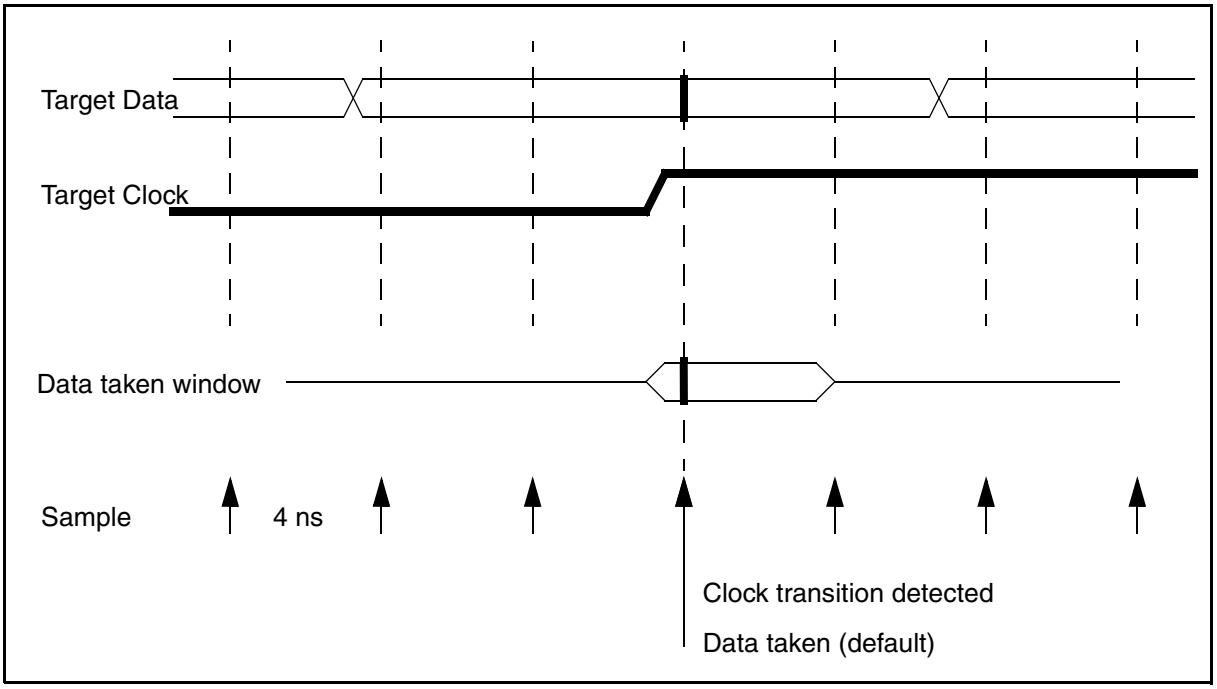
The PowerIntegrator offers different solutions for State Recording which are explained here.

Depending on the application under test it has to be decided which one fits best.

State recording by use of 250 MHz Mode

For slow signal toggling (up to 100 MHz) a simple transient detection gives good trace results.

The target clock (reference signal) and data is sampled on a fixed ratio of 4ns. The detection of a clock transition forces a new trace record.



A Target Clock edge is detected by comparing the current sampling against the sampling before. If there is a difference then a clock transition had occurred.

The Target Clock is asynchronous to the Sampling Clock. So the clock edge will be detected immediate, if the current Sampling Point is close to the clock edge, but it will be detected 4 ns later if the **last** Sampling Point was close to the clock edge.

This means, clock transition is detected in a 4 ns window **after** the Target Clock edge. During this period Target Data has to be stable (Data taken window).

PowerIntegrator Configuration:

- set **250 MHz** Mode
- set transient detection for reference signal to **Transient**, **RisingTransient** or **FallingTransient**.
- set transient detection for all other signals to **NoTransient**.

Advantages:

- any trace channel can be used as reference signal
- transition can be defined for Rising, Falling or Both edges

Restrictions:

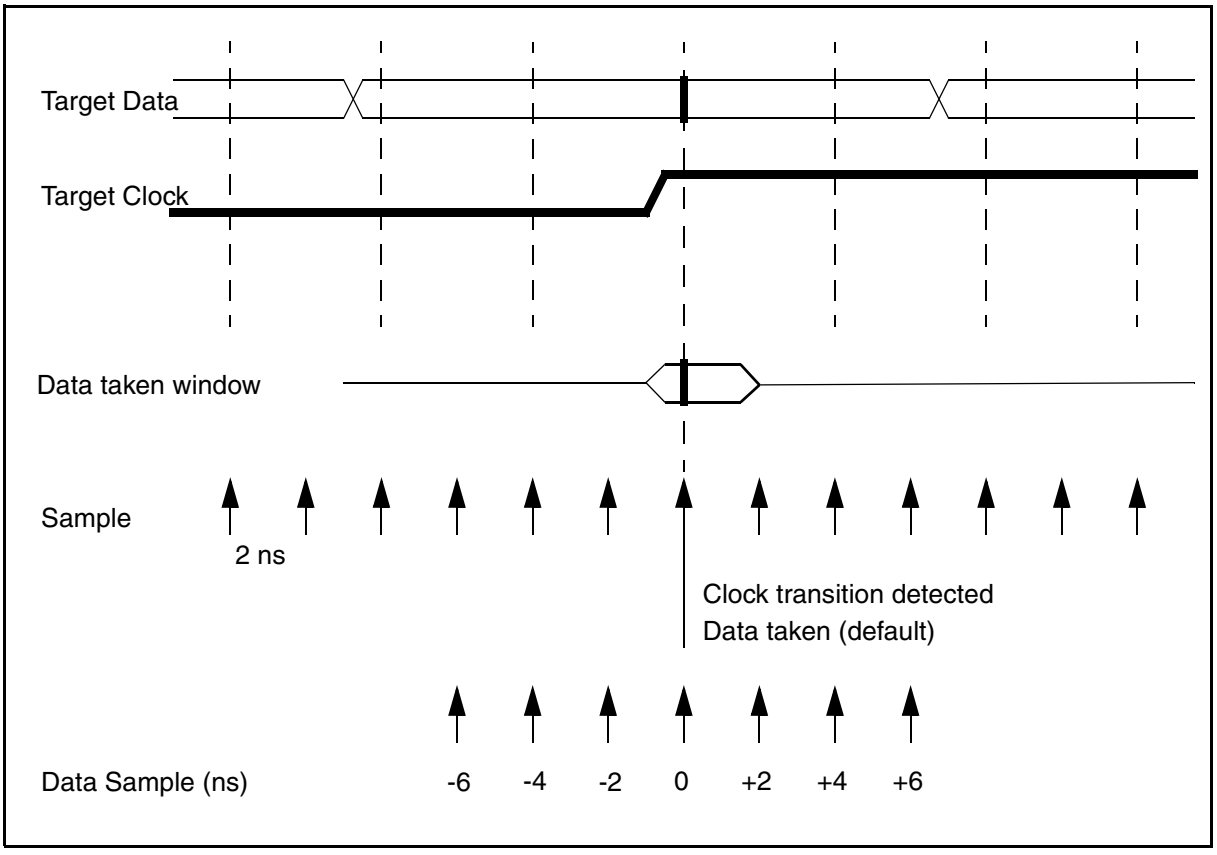
- The minimum clock high time is 4ns
- The minimum clock low time is 4ns
- The minimum data setup time is 0ns
- The minimum data hold time is 4ns

Depending on the target signal quality (transition times on data channels, reflections, …) the minimum setup and hold times will be longer.

State recording by use of STATE-MODE

This method is useful for signal toggling over 100 MHz and for very short clock strobes.

The target clock (reference signal) and data is sampled on a fixed ratio of 2 ns. The detection of a clock transition forces a new trace record.



A Target Clock edge is detected by comparing the current sampling against the sampling before. If there is a difference then a clock transition had occurred.

The Target Clock is asynchronous to the Sampling Clock. So the clock edge will be detected immediate if the current Sampling Point is close to the clock edge, but it will be detected 2 ns later if the **last** Sampling Point was close to the clock edge.

This means, clock transition is detected in a 2 ns window **after** the Target Clock edge. During this period Target Data has to be stable (Data taken window).

The Data taken window can be moved in steps of 2ns in the range of -6 ns to +6 ns around the Target Clock edge. This is useful for Target Data which changes at the same time as the Target Clock. So it is possible to trace data which is valid before or after the clock edge.

PowerIntegrator Configuration:

- select **STATE** Mode
- select clock source (**CLKA**, **CLKB**, **CLKJ**, **CLKK**)
- select clock edge (**Rising**, **Falling**).
- select sample offset (**SAMPLE -6 … +6 ns**)

Advantages:

- works for clock speeds up to 200 MHz
- detects any clock transition (very short strobes)
- transition can be defined for Rising or Falling edge
- variable offset for data sampling in the range of -6 … +6 ns around clock edge in steps of 2 ns

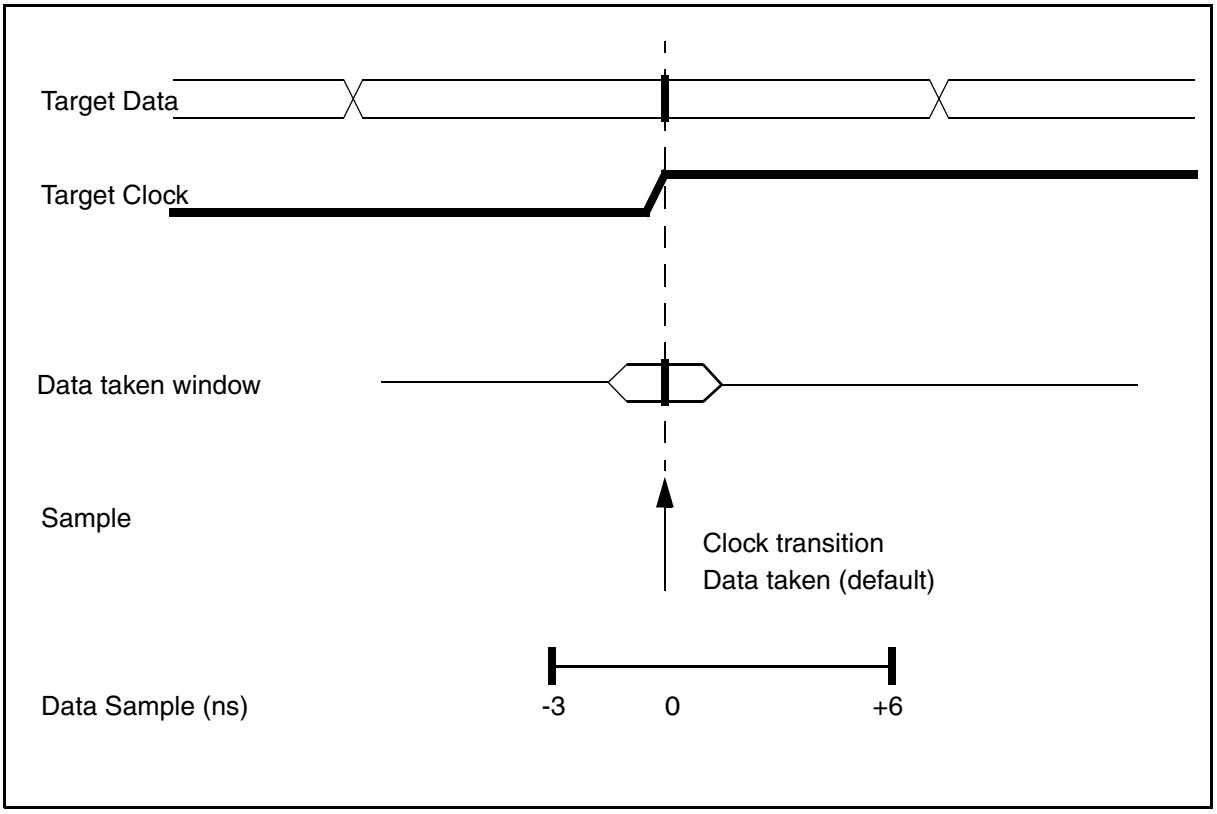
Restrictions:

- The clock signal has to be connected to predefined probe pins (CLKA or CLKB, CLKJ or CLKK)
- The minimum edge to edge time is 4 ns
- The minimum data setup time is 0 ns
- The minimum data hold time is 2 ns

Depending on the target signal quality (transition times on data channels, reflections, …) the minimum setup and hold times will be longer.

State recording by use of STATEPLL-MODE

With this method very short data setup and hold times can be handed. It is useful for high speed busses (up to 200 MHz) with continuous clocking and very short data valid windows.



The target clock itself defines the sampling point of the data channels. Data has to be stable for only 1 ns.

By use of the PowerIntegrator internal clocking unit the Sample Point can be moved in steps of 250ps in the range of -3 … 6 ns around the Target Clock edge. This way it is easy to set the Sample point to the center of the Data valid window.

PowerIntegrator Configuration:

- select **STATEPLL** Mode
- select clock source (**CLKA**, **CLKB**, **CLKJ**, **CLKK**)
- select clock edge (**Rising**, **Falling, DDR**).
- select sample offset (**SAMPLE -3 … +6 ns**)

Advantages:

- works for clock speeds up to 200 MHz
- supports Double Data Rate sampling up to 200 MHz
- transition can be defined for Rising, Falling or both edges (DDR sampling).
- variable offset for data sampling in the range of -3 … +6 ns around clock edge in steps of 250 ps.
- just 1ns data valid time needed

Restrictions:

- The clock signal has to be connected to predefined probe pins (CLKA or CLKB, CLKJ or CLKK).
- The clock signal has to be a continuous clock with fixed frequency with 50/50 duty cycle

Depending on the target signal quality (transition times on data channels, reflections, …) the minimum setup and hold times will be longer.