

Training Intel® Processor Tracing

MANUAL

Training Intel® Processor Tracing

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Training Intel® Processor Tracing

Version 06-Jun-2024

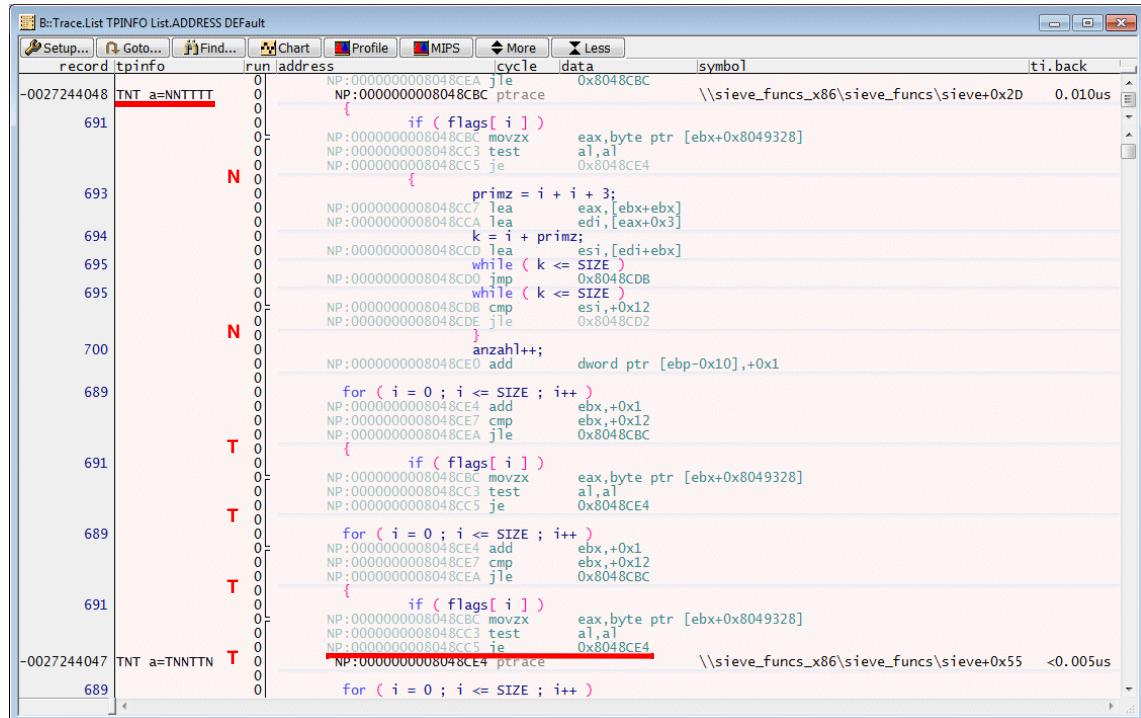
Protocol Description

Basic Trace Packets

To enable a trace tool to reconstruct the instruction execution sequence the following trace packets are generated:

TNT packets

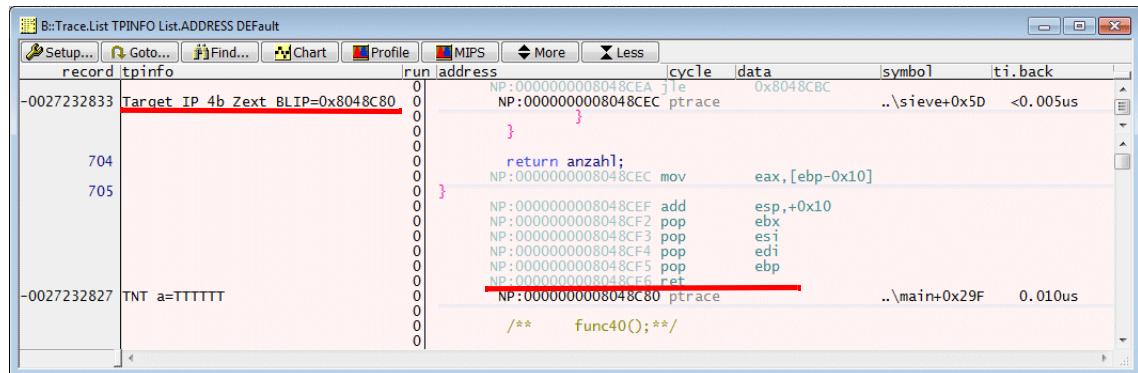
Taken Not Taken packets track the direction of up to 6 conditional branches. Since the address at which the program execution continues when the branch was taken is part of the source code TNT packets provide sufficient information to reconstruct the instruction execution sequence.



record	tpinfo	run	address	cycle	data	symbol	ti.back
-0027244048	TNT a=NNTTTT	691	NP:0000000008048CEA	jte	0x8048CBC	\\sieve_funcs_x86\sieve_funcs\sieve+0x2D	0.010us
			{				
			if (flags[i])				
			NP:0000000008048C8C movzx	eax,byte ptr	[ebx+0x8049328]		
			NP:0000000008048CC3 test	al,al			
			NP:0000000008048CC5 je	0x8048CE4			
		N	{				
			primz = i + i + 3;				
			NP:0000000008048CC7 lea	eax,[ebx+ebx]			
			NP:0000000008048CCA lea	edi,[eax+0x3]			
		694	k = i + primz;				
			NP:0000000008048CCD lea	esi,[edi+ebx]			
		695	while (k <= SIZE)				
			NP:0000000008048CDB jmp	0x8048CDB			
		695	while (k <= SIZE)				
			NP:0000000008048CDB cmp	esi,+0x12			
			NP:0000000008048CDE jle	0x804CD2			
		N	}				
		700	anzahl++;				
			NP:0000000008048CE0 add	dword ptr	[ebp-0x10],+0x1		
		689	for (i = 0 ; i <= SIZE ; i++)				
			NP:0000000008048CE4 add	ebx,+0x1			
			NP:0000000008048CE7 cmp	ebx,+0x12			
			NP:0000000008048CEA jle	0x8048CBC			
		T	{				
			if (flags[i])				
			NP:0000000008048CEC movzx	eax,byte ptr	[ebx+0x8049328]		
			NP:0000000008048CC3 test	al,al			
			NP:0000000008048CC5 je	0x8048CE4			
		T	{				
		689	for (i = 0 ; i <= SIZE ; i++)				
			NP:0000000008048CE4 add	ebx,+0x1			
			NP:0000000008048CE7 cmp	ebx,+0x12			
			NP:0000000008048CEA jle	0x8048CBC			
		T	{				
			if (flags[i])				
			NP:0000000008048CEC movzx	eax,byte ptr	[ebx+0x8049328]		
			NP:0000000008048CC3 test	al,al			
			NP:0000000008048CC5 je	0x8048CE4			
-0027244047	TNT a=TNNTTN	689	NP:0000000008048CE4	ptrace		\\sieve_funcs_x86\sieve_funcs\sieve+0x55	<0.005us
			for (i = 0 ; i <= SIZE ; i++)				

Target IP packets

Ret instructions, register indirect calls and similar instructions as well as exception and interrupts cause the generation of a Target IP packet. Since the address at which the program execution continues is only known at run-time, a Target IP packet contains this address fully or in a compressed format.



The screenshot shows the B::Trace.List TPINFO List.ADDRESS DEFault window. The table lists several trace entries. The first entry, record -0027232833, is highlighted with a red box and shows a 'Target IP' packet. The assembly code for this entry is:

```
NP:0000000008048CEA jle    0x8048CBC
NP:0000000008048CEC ptrace
...sieve+0x5D <0.005us
```

Below this, the assembly code for entry 704 is shown:

```
return anzahl;
NP:0000000008048CEC mov    eax, [ebp-0x10]
NP:0000000008048CEF add    esp, +0x10
NP:0000000008048CF2 pop    ebx
NP:0000000008048CF3 pop    esi
NP:0000000008048CF4 pop    edi
NP:0000000008048CF5 pop    ebp
NP:0000000008048CF6 ret
```

The second entry, record -0027232827, is also highlighted with a red box and shows a 'Target IP' packet. The assembly code for this entry is:

```
NP:0000000008048C80 ptrace
...main+0x29F 0.010us
```

Below this, the assembly code for entry 705 is shown:

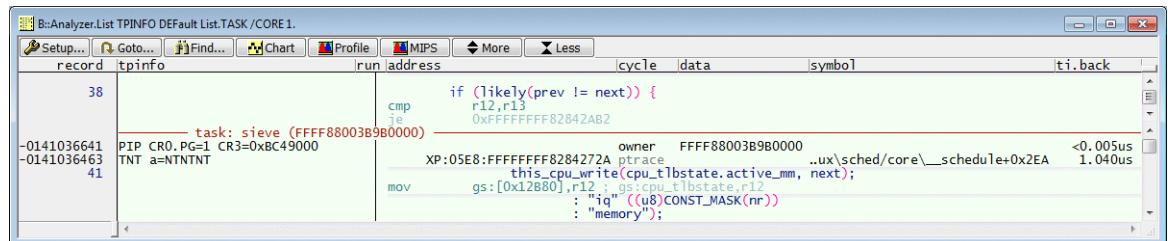
```
/* func40(); */
```

OS-Aware Tracing

Paging Information Packet (PIP)

x86/x64 processors have a CR3 control register that contains the Process Context Identifier (PCID). On every context switch the corresponding PCID is loaded to CR3.

Intel® PT generates a Paging Information Packet (PIP) when a write to CR3 occurs.



The screenshot shows the B::Analyzer.List TPINFO Default List.TASK /CORE 1 window. The table lists several trace entries. The first entry, record 38, is highlighted with a red box and shows a 'task: sieve' packet. The assembly code for this entry is:

```
if (likely(prev != next)) {
    r12,r13
    0xFFFFFFFF82842AB2
```

Below this, the assembly code for entry 41 is shown:

```
task: sieve (FFFF88003B9B0000)
PIP CR0.PG=1 CR3=0xBC49000
TNT a=NTNTNT
XP:05E8:FFFFFFFFFF8284272A ptrace
    this_cpu_write(cpu_tlbstate.active_mm, next);
    gs:[0x12880].r12 := this_cpu_tlbstate.r12;
        : "io" ((u8)CONST_MASK(nr))
        : "memory");
```

The second entry, record -0141036641, is also highlighted with a red box and shows a 'task: sieve' packet. The assembly code for this entry is:

```
<0.005us
...ux\ sched\core\__schedule+0x2EA 1.040us
```

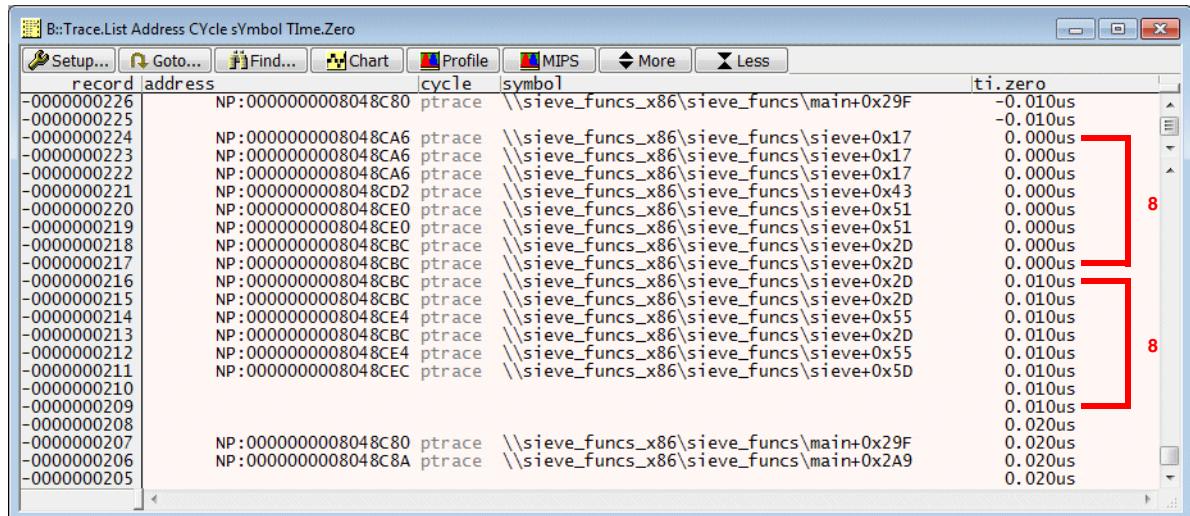
Tool Timestamp (POWER TRACE II / POWER TRACE III only)

POWER TRACE II / POWER TRACE III timestamps the trace information when it is stored in its trace buffer.

The resolution of the POWER TRACE II / POWER TRACE III timestamp is 5 ns.

8 trace record have always an identical timestamp. There are two reasons for this:

- The TRACE32 recording technology.
- The smallest Intel® PT packet is one byte.



record	address	cycle	symbol	ti.zero
-0000000226	NP:0000000008048C80	ptrace	\\sieve_funcs_x86\\sieve_funcs\\main+0x29F	-0.010us
-0000000225				-0.010us
-0000000224	NP:0000000008048CA6	ptrace	\\sieve_funcs_x86\\sieve_funcs\\sieve+0x17	0.000us
-0000000223	NP:0000000008048CA6	ptrace	\\sieve_funcs_x86\\sieve_funcs\\sieve+0x17	0.000us
-0000000222	NP:0000000008048CA6	ptrace	\\sieve_funcs_x86\\sieve_funcs\\sieve+0x17	0.000us
-0000000221	NP:0000000008048CD2	ptrace	\\sieve_funcs_x86\\sieve_funcs\\sieve+0x43	0.000us
-0000000220	NP:0000000008048CE0	ptrace	\\sieve_funcs_x86\\sieve_funcs\\sieve+0x51	0.000us
-0000000219	NP:0000000008048CE0	ptrace	\\sieve_funcs_x86\\sieve_funcs\\sieve+0x51	0.000us
-0000000218	NP:0000000008048CBC	ptrace	\\sieve_funcs_x86\\sieve_funcs\\sieve+0x2D	0.000us
-0000000217	NP:0000000008048CBC	ptrace	\\sieve_funcs_x86\\sieve_funcs\\sieve+0x2D	0.000us
-0000000216	NP:0000000008048CBC	ptrace	\\sieve_funcs_x86\\sieve_funcs\\sieve+0x2D	0.010us
-0000000215	NP:0000000008048CBC	ptrace	\\sieve_funcs_x86\\sieve_funcs\\sieve+0x2D	0.010us
-0000000214	NP:0000000008048CE4	ptrace	\\sieve_funcs_x86\\sieve_funcs\\sieve+0x55	0.010us
-0000000213	NP:0000000008048CE4	ptrace	\\sieve_funcs_x86\\sieve_funcs\\sieve+0x2D	0.010us
-0000000212	NP:0000000008048CE4	ptrace	\\sieve_funcs_x86\\sieve_funcs\\sieve+0x55	0.010us
-0000000211	NP:0000000008048CEC	ptrace	\\sieve_funcs_x86\\sieve_funcs\\sieve+0x5D	0.010us
-0000000210				0.010us
-0000000209				0.010us
-0000000208				0.020us
-0000000207	NP:0000000008048C80	ptrace	\\sieve_funcs_x86\\sieve_funcs\\main+0x29F	0.020us
-0000000206	NP:0000000008048C8A	ptrace	\\sieve_funcs_x86\\sieve_funcs\\main+0x2A9	0.020us
-0000000205				0.020us

In the standard trace display timestamp information is displayed for the first record with the new timestamp. All following records with an identical timestamp show <0.005us.

	record	run	address	cycle	data	symbol	ti.back
-00000000224	0	jle	0x8048CA6			NP:0000000008048CA6 ptrace	..\sieve+0x17 0.010us
	0	mov	byte ptr [ebx+0x8049328],0x1			ebx,+0x1	

	record	run	address	cycle	data	symbol	ti.back
-00000000223	0	jle	0x8048CA6			NP:0000000008048CA6 ptrace	..\sieve+0x17 <0.005us

CycleAccurate Tracing

If configured Intel® PT can generate cycle count information. The cycle count information indicates how much core clocks it took to execute a program section.

B:Trace List TPIINFO CLOCKS.Back DEF

		Setup...	Goto...	Find...	Chart	Profile	MIPS	More	Less	
		clocks.b		run	address	cycle		data	symbol	
-00000000231	TNT	a=TTTNTNT	cc=0x23	35.	0	jle	0x8048CA6	NP:0000000008048CA6	ptrace	\\sieve_funcs_x86\\sieve_funcs\\sieve+0x17
					0	mov	byte ptr [ebx+0x8049328],0x1			
					0	add	ebx, +0x1			
					0	cmp	ebx, +0x12			
					0	jle	0x8048CA6			
					0	mov	byte ptr [ebx+0x8049328],0x1			
					0	add	ebx, +0x1			
					0	cmp	ebx, +0x12			
					0	jle	0x8048CA6			
					0	mov	byte ptr [ebx+0x8049328],0x1			
					0	add	ebx, +0x1			
					0	cmp	ebx, +0x12			
					0	jle	0x8048CA6			
					0	for	(i = 0 ; i <= SIZE ; i++)			
					0	mov	ebx, 0x0			
					0	jmp	0x8048CE7			
					0	cmp	ebx, +0x12			
					0	jle	0x8048CBC			
					0	{				
					0	if	(flags[i])			
					0	test	eax, byte ptr [ebx+0x8049328]			
					0	je	al, al			
					0	0x8048CE4				
					0	{				
					0	primz = i + i + 3;				
					0	lea	eax, [ebx+ebx]			
					0	edi	, [eax+0x3]			
					0	k = i + primz;				
					0	lea	esi, [edi+ebx]			
					0	while	(k <= SIZE)			
					0	jmp	0x8048CDB			
					0	primz = i + i + 3;				
					0	cmp	esi, +0x12			
					0	jle	0x8048CDB			
-00000000209	TNT	a=TTTTTNT	cc=0x26	38.	0	NP:0000000008048C02	ptrace		\\sieve_funcs_x86\\sieve_funcs\\sieve+0x43	
					0	{				
					0	flags[k] = FALSE;				
					0	mov	byte ptr [esi+0x8049328],0x0			
					0	k += primz;				

Cycle accurate tracing requires up to 2 times more bandwidth.

Synchronization Time

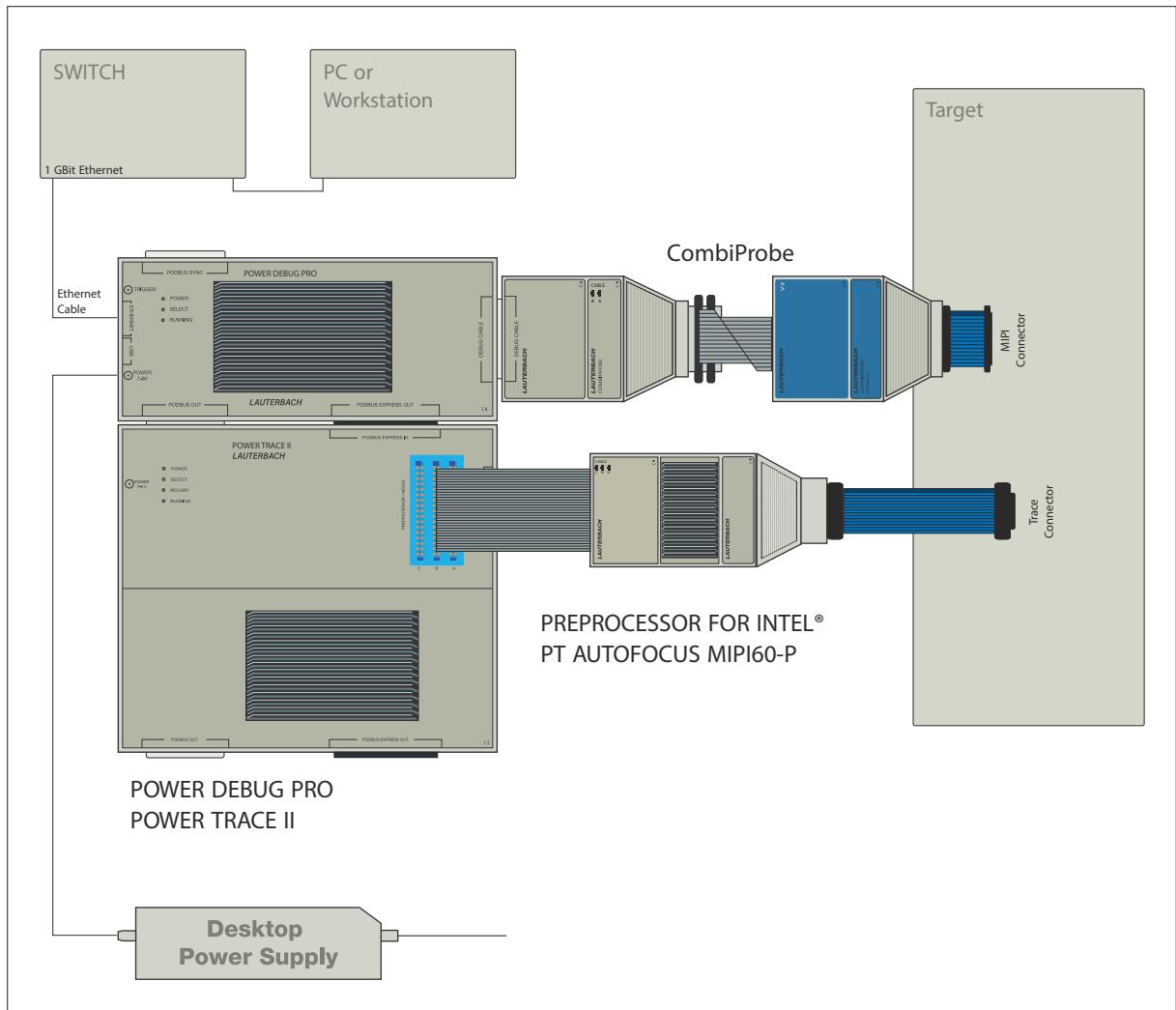
Not implemented yet.

Trace Configuration

Off-chip Trace

Recording the trace information exported via a PTI (Parallel Trace Interface) requires:

- A POWER TRACE II hardware (1 GByte, 2 GByte or 4 GByte of trace memory) or a POWER TRACE III hardware (4 GByte or 8 GByte of trace memory)
TRACE32 PowerView uses the name **Analyzer** to refer to the trace memory within POWER TRACE II / POWER TRACE III.
- An *Preprocessor for Intel® Atom™ AUTOFOCUS 600 MIPI*



The following configuration steps are required for off-chip tracing:

1. Configure Parallel Trace Interface on target.

Configuration is required for:

- PTI port size
- PTI frequency
- GPIO pins used for PTI

The following commands are provided for this purpose:

```
; write <value> to the configuration register addressed by A:<physical_address>
; in the specified <format>
PER.Set.simple A:<physical_address> %<format> <value>

; write <value> to the memory location addressed by A:<physical_address>
; in the specified <format>
Data.Set A:<physical_address> %<format> <value>
```

Data.Set is equivalent to **PER.Set.simple** if the configuration register is memory mapped.

The **access class** **A:** allow to use the physical address for the write operations.

```
Per.Set.simple A:0xf9009000 %Long 0x3e715
Data.Set A:0xf9009000 %Long 0x3e715
```

Please refer to your chip manual for the physical addresses of the configuration registers.

2. Configure TRACE32 for a PTI that exports STP (System Trace Protocol) packets.

```
SYStem.CONFIG STM Mode STP64 ; inform TRACE32 that your
                                ; chip provides a STM that
                                ; generated 64-bit STPv1
                                ; packets
STM.PortSize 16. ; inform TRACE32 that your
                  ; PTI size is 16 pins
```

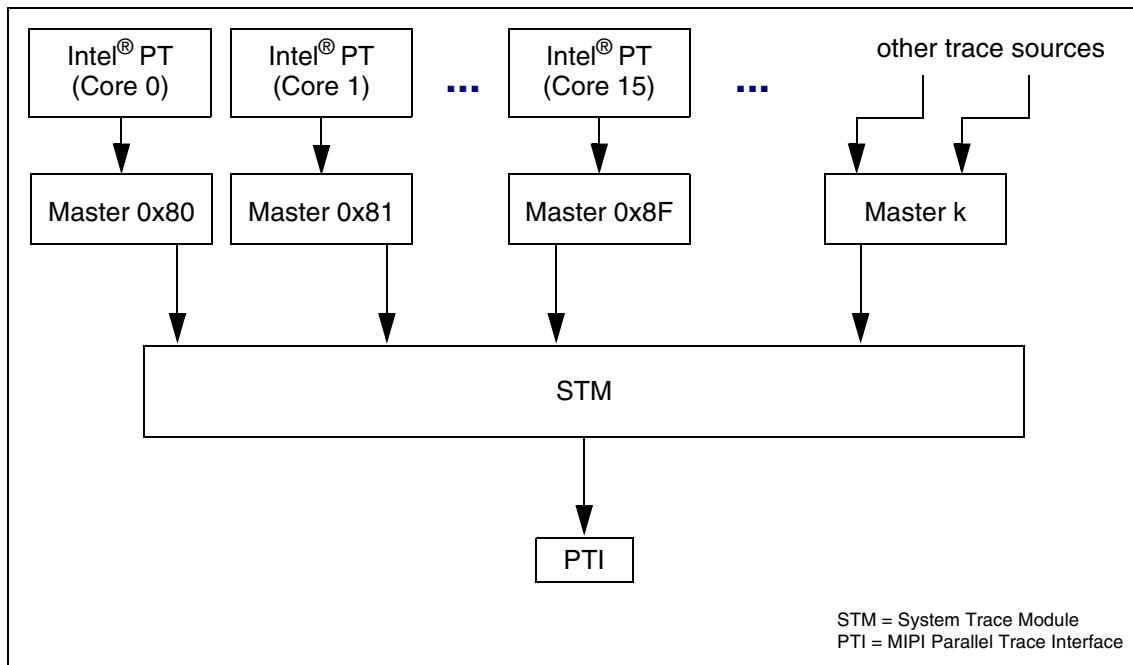
3. Inform TRACE32 which core traces you want to analyze.

IPT.TraceID <value> | <bitmask>

Specify which masters/channels (that produce Intel® PT trace information) you want to analyze with the help of TRACE32.

<value>	<value> is a 32-bit number. The first 16 bits represent the master ID, the last 16 bits represent the channel ID.
<bitmask>	bitmask representation of <value>

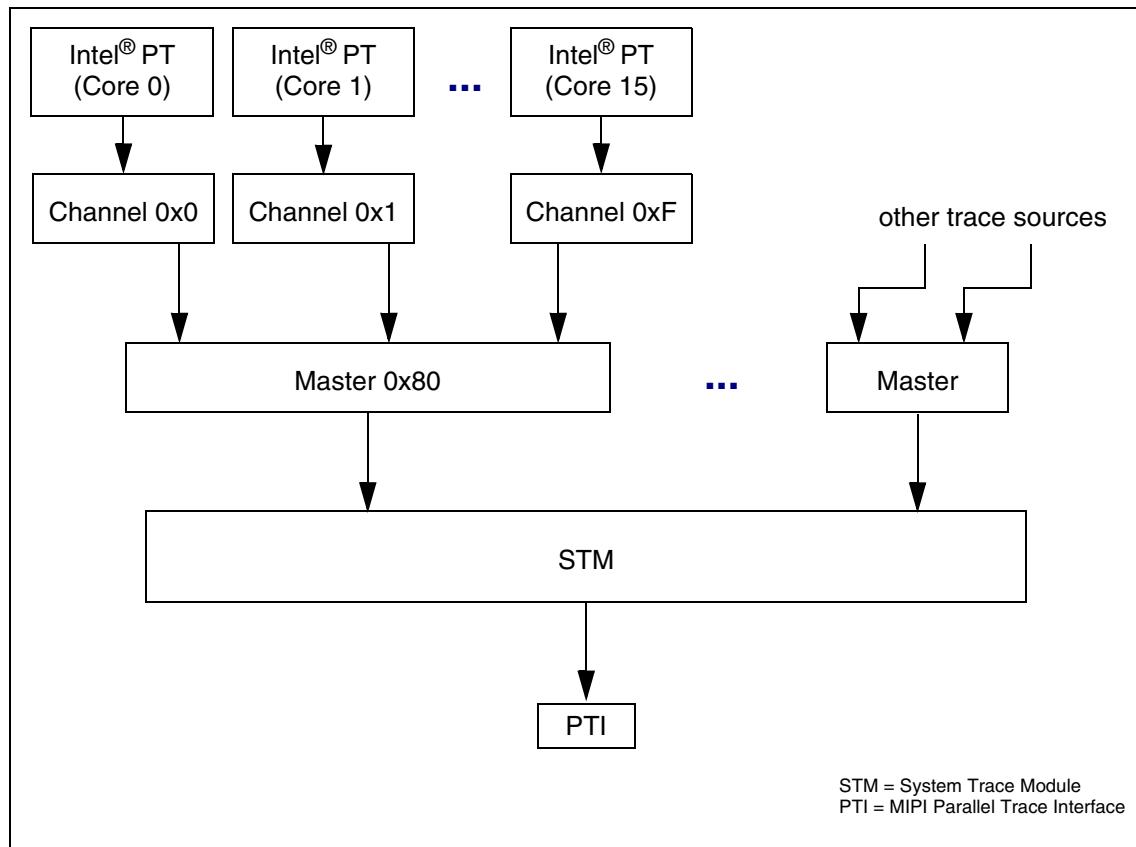
Example 1: Each core has its own master ID.



```
IPT.TraceID 0x00800000 ; master ID 0x80 is used to export Intel®
; PT trace information for core 0

IPT.TraceID 0x008x0000 ; master ID 0x80, 0x81, 0x82 ... are used to
; export Intel® PT trace information
; master ID 0x80 represents core 0
; the other master IDs consecutively
; represent core 1 to core 15
```

Example 2: Each core has its own channel ID, all cores use the same master ID.



```
IPT.TraceID 0x0080000x ; master ID 0x80 is used to export Intel®  
; PT  
; trace information  
; channel ID 0x0 represents core 0  
; the other channel IDs consecutively  
; represent core 1 to core 15
```

4. Enable Intel® PT on the target and allow TRACE32 to configure it.

```
IPT.ON
```

5. Calibrate the *Preprocessor for Intel® Atom™ AUTOFOCUS 600 MIPI* for recording.

TRACE32 supports three methods of generating outputs on the trace lines for calibration.

- On-chip test pattern generator (not tested yet).
- Test executable provided by Lauterbach.
- Application program.

Please be aware that TRACE32 PowerView displays “**Analyzer data capture o.k.**” only if:

- All trace lines toggled while calibration is performed.
- There are no short circuits between the trace lines.
- An error-free trace decoding was possible.

Test executable provided by Lauterbach

In order to use the test executable provided by Lauterbach for calibration, the following command sequence is recommended.

```
; example for a free-running clock (Tangier)

AREA.view ; open TRACE32 Message AREA
            ; to observe calibration
            ; results

Analyzer.THreshold VCC ; advise TRACE32 to use
                        ; 1/2 VCC as threshold level
                        ; for the trace signals

Analyzer.AutoFocus /NoTHreshold ; start the calibration by
                                ; using test executable

                                ; advise TRACE32 to keep
                                ; the threshold level
```

A manual setup is required if your target is using a gated clock. Refer to “[Manual Setup](#)” in AutoFocus User’s Guide, page 18 (autofocus_user.pdf) for assistance.

Application program

In order to use the application program for calibration, the following command sequence is recommended.

```
; example for a free-running clock (Tangier)

AREA.view ; open TRACE32 Message AREA
            ; to observe calibration
            ; results

Data.LOAD.Elf demo_x86.elf /PlusVM ; download application program
                                    ; to the target,
                                    ; in order to perform trace
                                    ; decoding while the
                                    ; application program is
                                    ; running, the program code
                                    ; has to be copied to the
                                    ; TRACE32 Virtual Memory

Go ; start the execution of the
    ; application program

Analyzer.THreshold VCC ; advise TRACE32 to use
                        ; 1/2 VCC as threshold level
                        ; for the trace signals

Analyzer.AutoFocus /NoTHreshold ; start the calibration
                                    ; advise TRACE32 to keep
                                    ; the threshold level

WAIT 1.s ; wait 1 second

Break ; stop the program execution
```

A manual setup is required if your target is using a gated clock. Refer to “[Manual Setup](#)” in AutoFocus User’s Guide, page 18 (autofocus_user.pdf) for assistance.

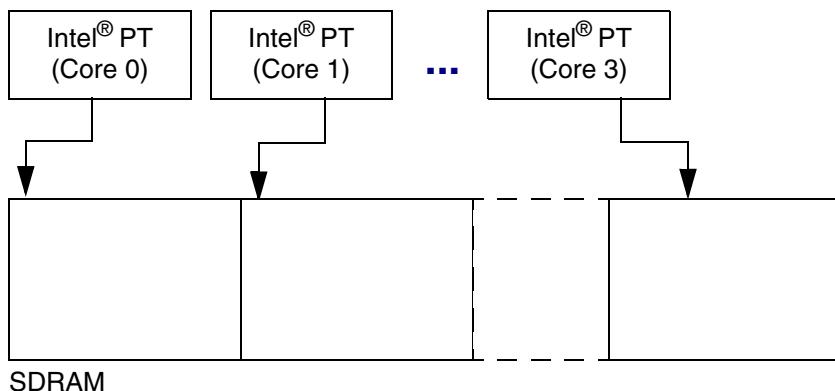
After a successful configuration of the off-chip tracing the following command can be used to inspect the STP packet stream:

STMAnalyzer.List		Display STP packet stream recorded to POWER TRACE II / POWER TRACE III.						
record	run	address	cycle	data	symbol	ti.back		
-00000000364		C:0000000000000800000	d64	B08C3BB08C1FB08C		0.010us		
-00000000356		C:0000000000000800000	d64	8C67B08C5CB08C57		0.010us		
-00000000322			master	80		0.170us		
-00000000321		C:0000000000000800000	c8	00		<0.005us		
-00000000319		C:0000000000000800000	d64	7E757F7F7F8C6FB0		0.010us		
-00000000311		C:0000000000000800000	d64	4F79734957756D6E		0.010us		
-00000000302		C:0000000000000800000	d64	757F7F7F8C80B066		0.010us		
-00000000294		C:0000000000000800000	d64	79734957756D6E7E		0.010us		
-00000000285		C:0000000000000800000	d64	7F7F7F8C80B0664F		0.010us		
-00000000277		C:0000000000000800000	d64	734957756D6E7E75		1.835us		
-00000000268		C:0000000000000800000	d64	7F7F8C80B0664F79		0.010us		
-00000000260		C:0000000000000800000	d64	4957756D6E7E757F		0.010us		
-00000000226			master	80		0.170us		
-00000000225		C:0000000000000800000	c8	00		<0.005us		
-00000000223		C:0000000000000800000	d64	7F8C80B0664F7973		0.010us		
-00000000215		C:0000000000000800000	d64	57756D6E7E757F7F		0.010us		
-00000000206		C:0000000000000800000	d64	8C80B0664F797349		0.010us		
-00000000198		C:0000000000000800000	d64	756D6E7E757F7F7F		0.010us		
-00000000189		C:0000000000000800000	d64	80B0664F79734957		0.010us		
-00000000181		C:0000000000000800000	d64	6D6E7E757F7F78C		1.725us		
-00000000172		C:0000000000000800000	d64	B064F7973495775		0.010us		
-00000000164		C:0000000000000800000	d64	6E7E757F7F78C80		0.010us		
-00000000130			master	80		0.170us		
-00000000129		C:0000000000000800000	c8	00		<0.005us		
-00000000127		C:0000000000000800000	d64	664F79734957756D		0.010us		

The Intel® PT based core traces can be displayed by the following command:

Analyzer.List		Display all core trace information decoded out of the STP packet stream.						
record	run	address	cycle	data	symbol	ti.back		
-0027244056	0	cmp	esi,+0x12					
	0	jle	0x8048CD2					
	0		NP:000000000008048CEO	ptrace	..\sieve+0x51	0.015us		
	700			anzahl++;				
	0	add	dword ptr [ebp-0x10],+0x1					
	689	0	for (i = 0 ; i <= SIZE ; i++)					
	0	add	ebx,+0x1					
	0	cmp	ebx,+0x12					
	0	jle	0x8048CBC					
	691	0	{					
	0	movzx	eax,byte ptr [ebx+0x8049328]					
	0	test	al,al					
	0	je	0x8048CE4					
	693	0	{					
	0	leah	primz = i + i + 3;					
	0	lea	eax,[ebx+ebx]					
	694	0	edi,[eax+0x3]	k = i + primz;				
	0	lea	esi,[edi+ebx]	while (k <= SIZE)				
	695	0	jmp	0x8048CDB				

If the Intel® PT trace information is routed to SDRAM, a fixed amount of memory is assigned to each core. The max. SDRAM size per core is currently 4 MByte.



Configure TRACE32

1. Advise TRACE32 to read the trace information from SDRAM.

```
Trace.METHOD Onchip
```

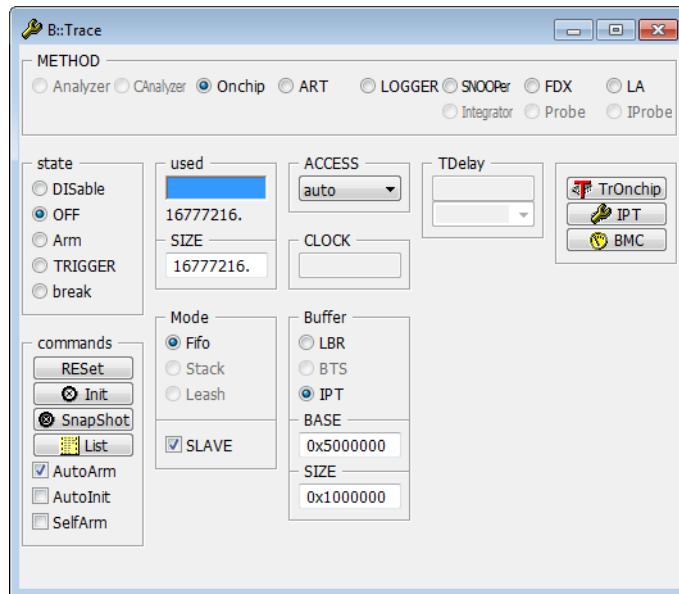
TRACE32 reads the onchip trace via JTAG.

2. Provide further details on the SDRAM configuration to TRACE32.

```
Onchip.Buffer IPT ; inform TRACE32 that the SDRAM
; provides Intel® PT trace
; information

Onchip.Buffer BASE 0x5000000 ; inform TRACE32 that the SDRAM
; allocated for Intel® PT trace
; starts at address 0x5000000

Onchip.Buffer SIZE 0x1000000 ; inform TRACE32 that the SDRAM
; allocated for Intel® PT trace has
; a size of 16 MByte
```



3. Enable Intel® PT on the target and allow TRACE32 to configure it.

IPPT.ON

If the command **Onchip.List** is used, TRACE32 merges the Intel® PT traces from the individual cores as follows:

SDRAM block
core 0

Intel® PT packet 1
Intel® PT packet 2
Intel® PT packet 3
Intel® PT packet 4
Intel® PT packet 5

SDRAM block
core 1

Intel® PT packet 1
Intel® PT packet 2
Intel® PT packet 3
Intel® PT packet 4
Intel® PT packet 5
Intel® PT packet 6
Intel® PT packet 7

SDRAM block
core 2

Intel® PT packet 1
Intel® PT packet 2
Intel® PT packet 3
Intel® PT packet 4
Intel® PT packet 5
Intel® PT packet 6

SDRAM block
core 3

Intel® PT packet 1

Onchip.List

Intel® PT packet 1 of core 0
Intel® PT packet 1 of core 1
Intel® PT packet 1 of core 2
Intel® PT packet 1 of core 3
Intel® PT packet 2 of core 0
Intel® PT packet 2 of core 1
Intel® PT packet 2 of core 2
Intel® PT packet 3 of core 0

This procedure will change with the decoding of synchronisation packets.

Onchip.List

; display trace listing for all
; cores

Onchip.List /CORE 1

; display trace listing for core 1

B::Onchip.List

rec	run	address	cycle	data	symbol
	2	mov	esi,[ebp-0x4]		
	2	mov	ebx,[ebp-0x8]		
	2	mov	esp,ebp		
	2	pop	ebp		
	2	ret			
-0005	3	NP:03E1:40078550	ptrace		
	3	push	ebp		
	3	mov	ebp,esp		
	3	push	edi		
	3	push	esi		
	3	push	ebx		
	3	lea	esp,[esp-0x2C]		
	3	mov	ebx,[ebp+0x8]		
	3	test	ebx,ebx		
	3	je	0x400785BB		
	3	mov	esi,[ebx]		
	3	mov	edi,esi		
	3	mov	edx,esi		
	3	and	edi,0x2000		
	3	and	edx,0xC000		
	3	mov	[ebp-0x28],edx		
	3	jne	0x400785C2		
	3	mfence			
	3	mov	eax,0xFFFFFFFF		
	→	interrupt			
-0004	0	NP:051E:C1A806C8	ptrace	..\ux\Global\apic_timer_interrupt	
-0003	1	NP:021D:C1A806C8	ptrace	..\ux\Global\apic_timer_interrupt	

B::Onchip.List /CORE 1

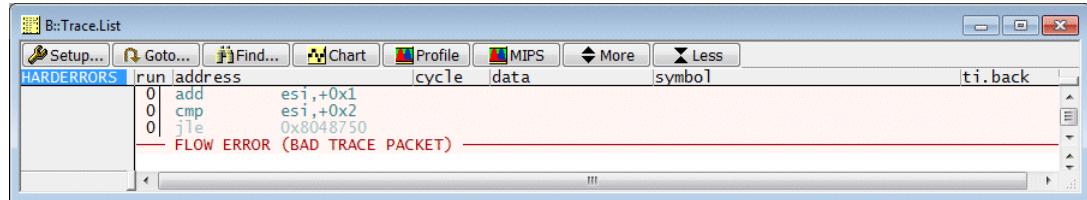
rec	run	address	cycle	data	symbol
	1	mov	ebx,[ebp-0x0C]		
	1	mov	esi,[ebp-0x8]		
	1	mov	edi,[ebp-0x4]		
	1	mov	esp,ebp		
	1	pop	ebp		
	1	ret			
-0015		NP:021D:C14A0B18	ptrace	\\vmlinux\Global\trace_hardirqs_on_thunk+0x0C	
		pop	edx		
		pop	ecx		
		pop	eax		
		ret			
-0011		NP:021D:C1A80420	ptrace	\\vmlinux\Global\restore_all_notrace	
				!!!	

ERRORS

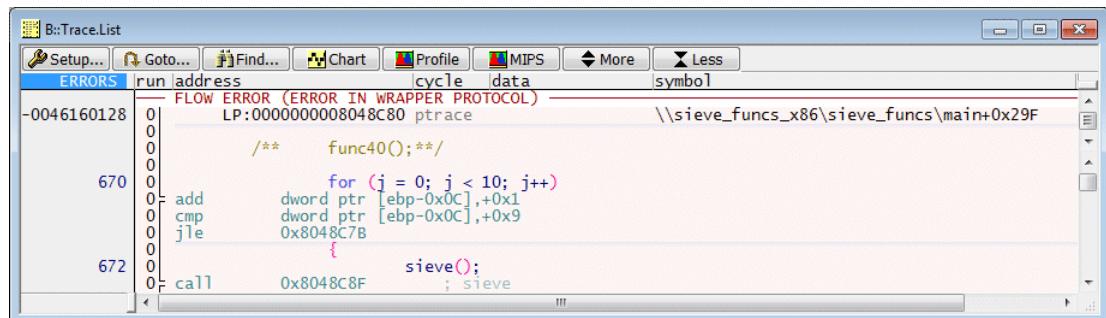
If the trace contains ERRORS, please try to set up a proper trace recording before you start to evaluate or analyze the trace contents.

ERRORS can be caused by the following:

- TRACE32 detected an invalid trace packet. TRACE32 additionally displays the error indicator HARDERROR, if it is likely that the error was caused by pin problems.



- TRACE32 could not decode the packet.

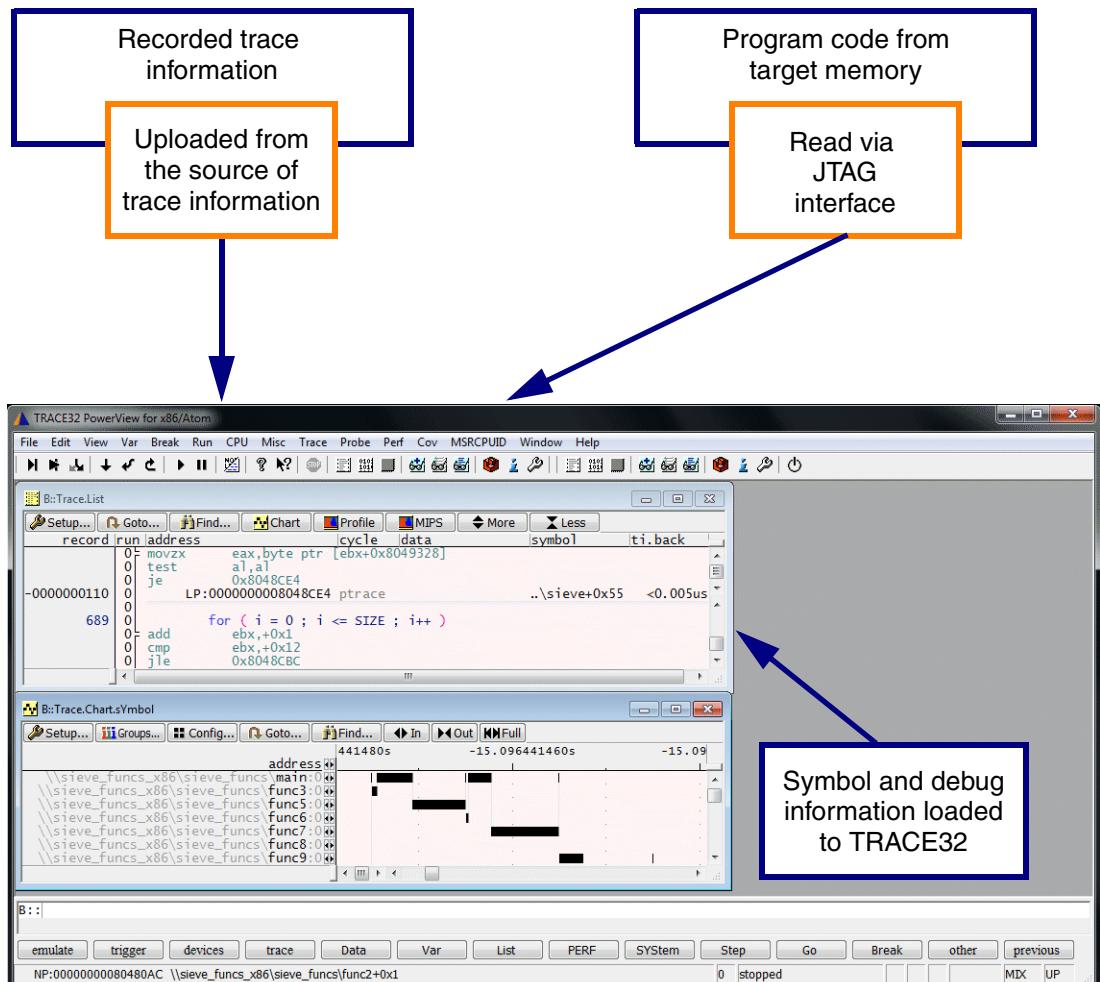


- The trace information is not consistent with the program code in the target memory.

0 pop esi
0 pop edi
0 pop ebp
0 ret
FLOW ERROR (UNEXPECTED INDIRECT BRANCH) —
LP:0000000008048C80 ptrace \sieve_funcs_x86\sieve_funcs\main+0x29F 18.155us
0 /* func40(); */
0 for (j = 0; j < 10; j++)
0 add dword ptr [ebp-0x0C],+0x1
0 cmp dword ptr [ebp-0x0C],+0x9
0 jle 0x8048C7B {
0
0

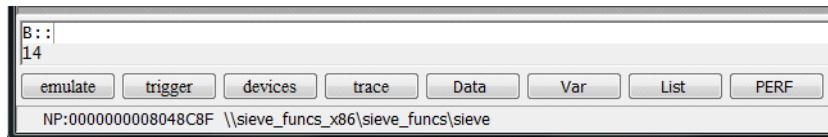
Background: In order to provide an intuitive trace display the following sources of information are merged:

- The trace information recorded.
- The program code from the target memory read via the JTAG interface.
- The symbol and debug information already loaded to TRACE32.

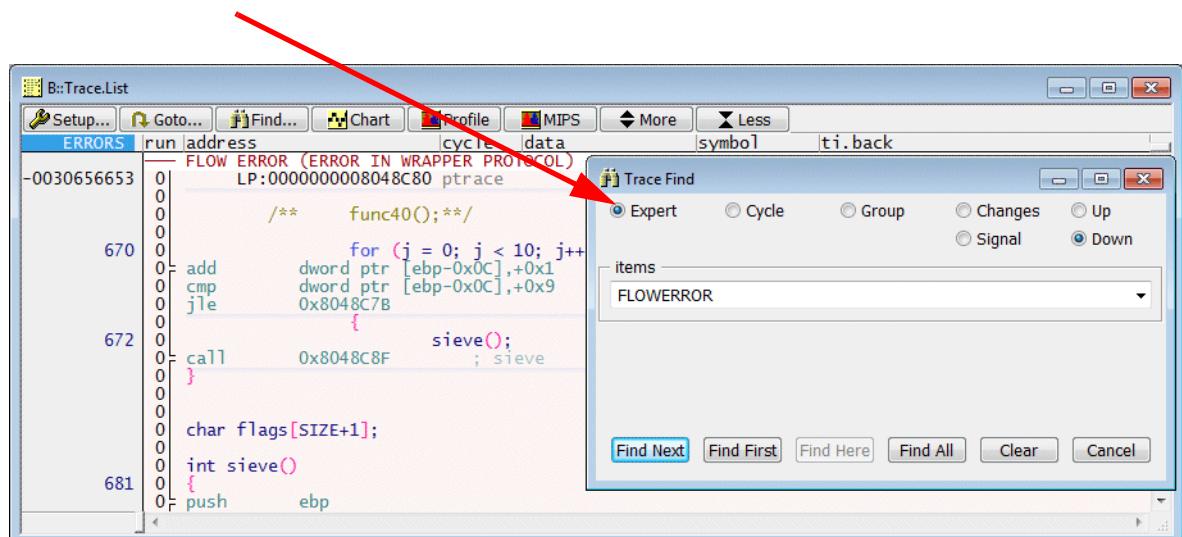


The TRACE32 function **Trace.FLOW.ERROR()** returns the number of ERRORS as a hex. number.

```
PRINT %Decimal Trace.FLOW.ERRORS() ; display the number of ERRORS
; as a decimal number in the
; TRACE32 PowerView Message Line
```



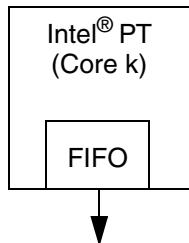
To find ERRORS in the trace use the keyword FLOWERROR on the Expert page of the **Trace Find** dialog.



Trace.Find FLOWERROR

TARGET FIFO OVERFLOW

Inside each Intel® PT generation module trace packets are queued to a FIFO buffer in order to send them out to the STM/SDRAM.



If trace packets are generated faster than can be sent out, the FIFO buffer can overflow and trace packets are lost.

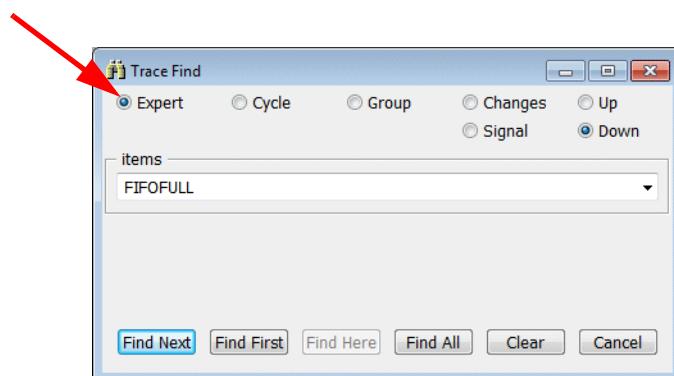
The affected Intel® PT generates a Buffer Overflow packet (FUP.OVF) to indicate that its FIFO is full and trace packets are no longer generated.

A Asynchronous Flow Update packet, that provides the address of the next instruction that will be executed, is generated to indicate that the packet generation now continues.

The TRACE32 function **Trace.FLOW.FIFOFULL()** returns the number of TARGET FIFO OVERFLOWS as a hex. number.

```
PRINT %Decimal Trace.FLOW.FIFOFULL() ; display the number of TARGET
; FIFO OVERFLOWS as a decimal
; number in the TRACE32
; PowerView Message Line
```

To find TARGET FIFO OVERFLOWS in the trace use the keyword **FIFOFULL** on the Expert page in the **Trace Find** dialog.



Trace.Find FIFOFULL

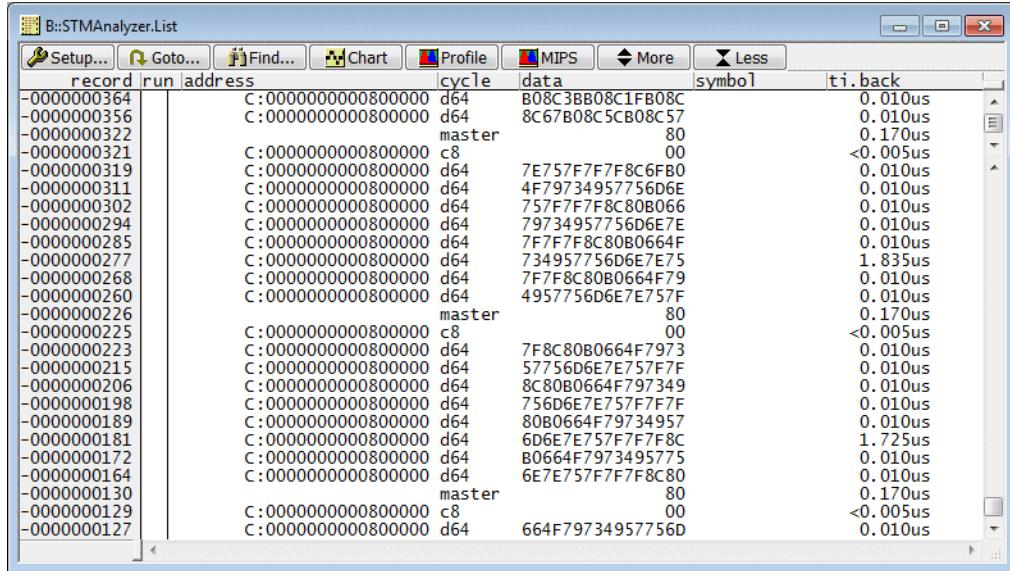
TARGET FIFO OVERFLOWS are strictly speaking not errors. They can occur in normal operation.

Since gaps in the instruction execution sequence are likely to disturb the nesting trace analyses, TRACE32 explicitly points them out.

SystemTrace

Depending on where the STP packets are stored, the following TRACE32 command groups can be used to analyze and display these packets:

- **STMAnalyzer.<sub_cmd>**, if the STP packets are stored in the trace memory provided by POWER TRACE II / POWER TRACE III.

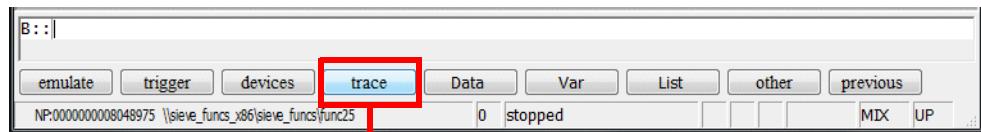


The screenshot shows a Windows application window titled "B:STMAnalyzer.List". The window contains a table with the following columns: record, run, address, cycle, data, symbol, and ti.back. The data is organized into several groups, likely representing different transactions or events. The "symbol" column contains memory addresses, and the "ti.back" column contains time values in microseconds (e.g., 0.010us, 0.170us, <0.005us).

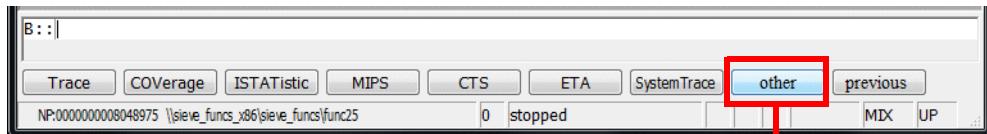
record	run	address	cycle	data	symbol	ti.back
-0000000364		C:0000000000800000	d64	B08C3BB08C1FB08C		0.010us
-0000000356		C:0000000000800000	d64	8C67B08C5CB08C57		0.010us
-0000000322			master	80		0.170us
-0000000321		C:0000000000800000	c8	00		<0.005us
-0000000319		C:0000000000800000	d64	7E757F7F7F8C6FB0		0.010us
-0000000311		C:0000000000800000	d64	4F79734957756D6E		0.010us
-0000000302		C:0000000000800000	d64	757F7F7F8C80B066		0.010us
-0000000294		C:0000000000800000	d64	79734957756D6E7E		0.010us
-0000000285		C:0000000000800000	d64	7F7F7F8C80B0664F		0.010us
-0000000277		C:0000000000800000	d64	734957756D6E7E75		1.835us
-0000000268		C:0000000000800000	d64	7F7F8C80B0664F79		0.010us
-0000000260		C:0000000000800000	d64	4957756D6E7E757F		0.010us
-0000000226			master	80		0.170us
-0000000225		C:0000000000800000	c8	00		<0.005us
-0000000223		C:0000000000800000	d64	7F8C80B0664F7973		0.010us
-0000000215		C:0000000000800000	d64	57756D6E7E757F7F		0.010us
-0000000206		C:0000000000800000	d64	8C80B0664F797349		0.010us
-0000000198		C:0000000000800000	d64	756D6E7E757F7F7F		0.010us
-0000000189		C:0000000000800000	d64	80B0664F79734957		0.010us
-0000000181		C:0000000000800000	d64	6D6E7E757F7F7F8C		1.725us
-0000000172		C:0000000000800000	d64	B0664F7973495775		0.010us
-0000000164		C:0000000000800000	d64	6E7E757F7F7F8C80		0.010us
-0000000130			master	80		0.170us
-0000000129		C:0000000000800000	c8	00		<0.005us
-0000000127		C:0000000000800000	d64	664F79734957756D		0.010us

- **STMIA.<sub_cmd>**, if the STP packets were recorded without a TRACE32 trace tool, and if they were loaded to TRACE32 PowerView for analysis.

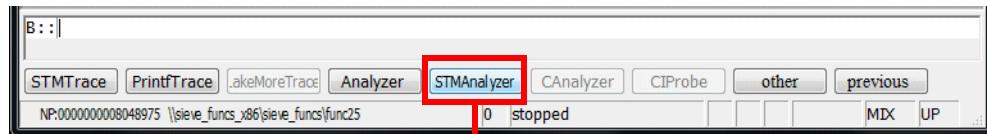
The command groups usable in your current configuration can be get from the TRACE32 PowerView Softkey line.



Push **trace** to get access to all command groups that analyze trace information.



Push **other** to see more command groups.



POWER TRACE II / POWER TRACE III is used in the current configuration, so the command group STMAnalyzer is enabled.



The command group STMLA is always enabled.

TRACE32 PowerView offers the following abstraction, since most *<sub_cmd>* are identical for all command groups:

SystemTrace.METHOD Analyzer | LA

SystemTrace.METHOD Analyzer

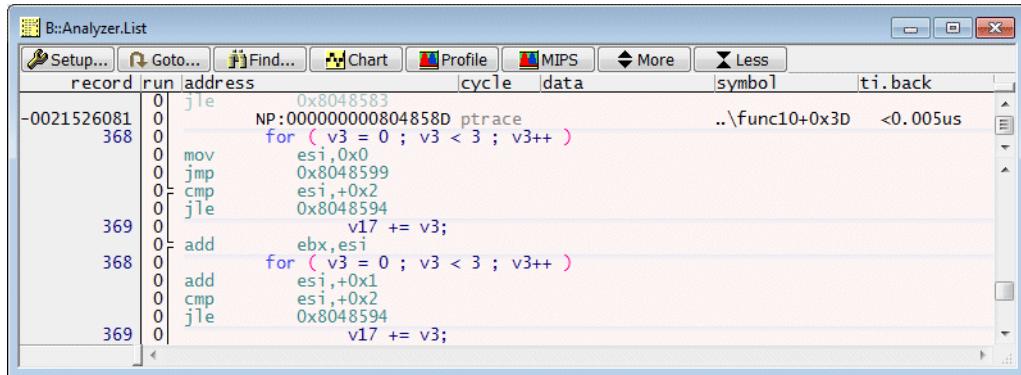
; inform TRACE32 PowerView that the
; STP packets are stored in POWER
; TRACE II

SystemTrace.List

; List STP packet stream

Depending on where the trace packets are stored, the following TRACE32 command groups can be used to analyze and display the core trace information:

- **Analyzer.<sub_cmd>**, if the STP packets are stored in the trace memory provided by POWER TRACE II / POWER TRACE III.



The screenshot shows the TRACE32 PowerView interface with the 'Analyzer.List' tab selected. The window has a toolbar with buttons for 'Setup...', 'Goto...', 'Find...', 'Chart', 'Profile', 'MIPS', 'More', and 'Less'. The main area is a table with columns: record, run, address, cycle, data, symbol, and ti.back. The table displays several trace records (e.g., -0021526081, 368, 369) with their assembly instructions and corresponding trace symbols. The assembly code includes instructions like jne, mov, jmp, cmp, and add, with memory addresses like 0x8048583 and 0x8048599.

record	run	address	cycle	data	symbol	ti.back
-0021526081	0	jne 0x8048583				
	0	NP:000000000804858D ptrace			..\\func10+0x3D	<0.005us
368	0	for (, v3 = 0 ; v3 < 3 ; v3++)				
	0	mov esi,0x0				
	0	jmp 0x8048599				
	0	cmp esi,+0x2				
	0	jle 0x8048594				
	369	v17 += v3;				
	0	add ebx,esi				
	368	for (, v3 = 0 ; v3 < 3 ; v3++)				
	0	add esi,+0x1				
	0	cmp esi,+0x2				
	0	jle 0x8048594				
	369	v17 += v3;				

- **Onchip.<sub_cmd>**, if the Intel® PT trace packets are stored in the target SDRAM.
- **LA.<sub_cmd>**, if the trace packets were recorded without a TRACE32 trace tool, and if they were loaded to TRACE32 PowerView for analysis.

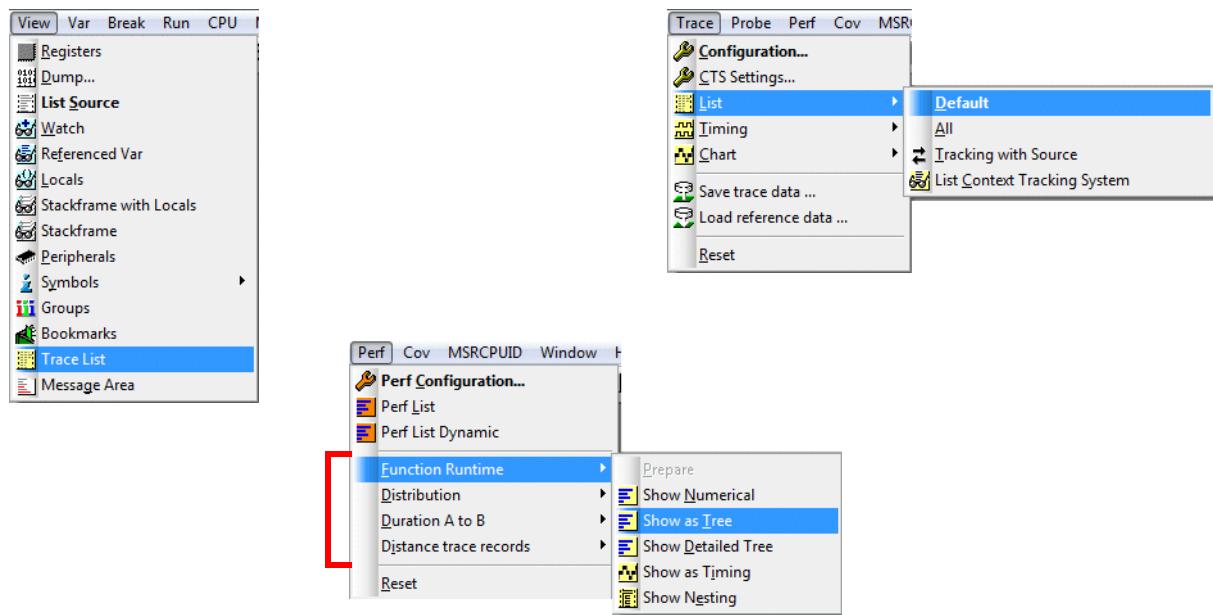
TRACE32 PowerView offers the following abstraction, since most *<sub_cmd>* are identical for all command groups:

Trace.METHOD Analyzer | Onchip | LA

```
Trace.METHOD Analyzer ; inform TRACE32 PowerView that the
; trace packets are stored in POWER
; TRACE II
Trace.List ; List core trace information
```

Selecting the trace METHOD has the following additional consequences:

All **Trace.<sub_cmd>** commands offered in the TRACE32 PowerView menu apply to the selected trace METHOD.



TRACE32 is advised to use the trace information from the trace specified by METHOD as source for the trace evaluations of the following command groups:

COVerage.<sub_cmd> Trace-based code coverage

ISTAT.<sub_cmd> Detailed instruction analysis

MIPS.<sub_cmd> MIPS analysis

Influencing Factors on the Trace Information

The main influencing factor on the trace information is the **Intel® PT**. It specifies what type of trace information is generated for the user.

Basics about the trace messages are described in “[Protocol Description](#)”, page 6.

Advanced setting can be found in “[Trace Control by Filters](#)”, page 68.

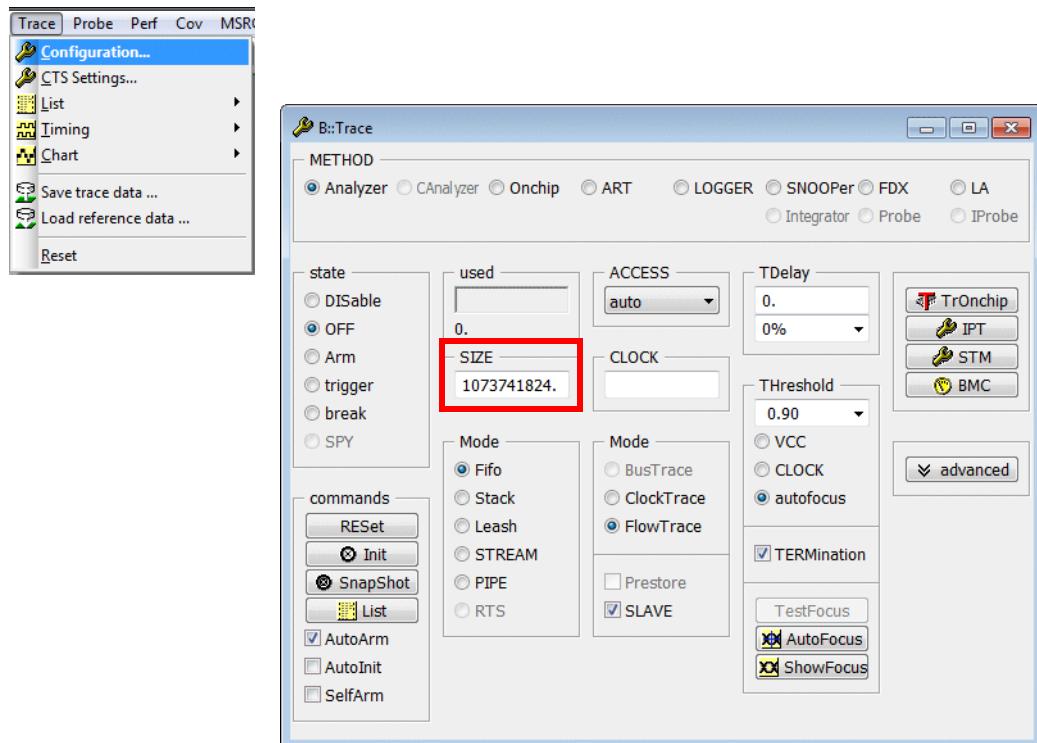
Another important influencing factor are the settings in the **TRACE32 Trace Configuration** window. They specify how much trace information can be recorded and when the trace recording is stopped.

Settings in the TRACE32 Trace Configuration Window

The Mode settings in the Trace Configuration window specify how much trace information can be recorded and when the trace recording is stopped.

The following modes are provided, if the **Trace.METHOD Analyzer** is selected:

- **Fifo, Stack, Leash Mode:** allow to record as much trace records as indicated in the **SIZE** field of the Trace Configuration window.



- **STREAM Mode:** STREAM mode specifies that the trace information is immediately streamed to a file on the host computer. STREAM mode allows a trace memory size of several T Frames.

- **PIPE Mode:** PIPE mode specifies that the trace information is immediately streamed to a named pipe on the host computer.

PIPE mode creates the path to convey trace raw data to an application outside of TRACE32 PowerView. The named pipe has to be created by the receiving application before TRACE32 can connect to it.

Trace.Mode PIPE

Trace.PipeWrite <pipe_name>

Connect to named pipe

Trace.PipeWrite \\.\pipe\<pipe_name>

Connect to named pipe (Windows)

Trace.PipeWrite

Disconnect from named pipe

...

Trace.Mode PIPE ; switch trace to PIPE mode

Trace.PipeWRITE \\.\pipe\ppproto00 ; connect to named pipe
; (Windows)

...

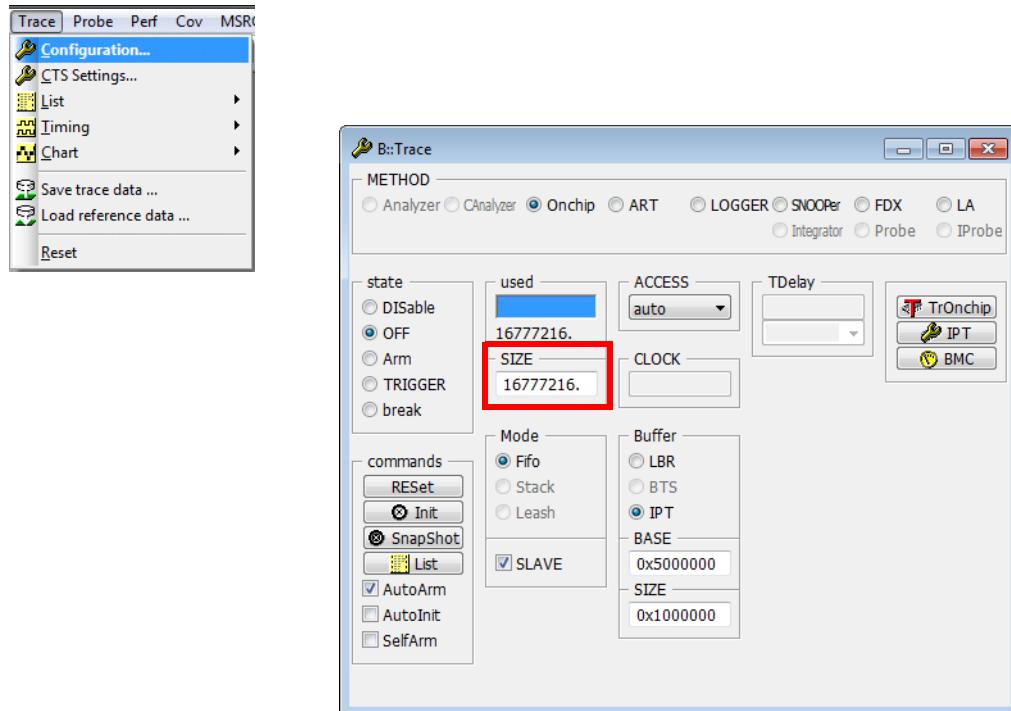
Trace.PipeWRITE ; disconnect from named pipe



STP packets (no timestamp) are conveyed in PIPE mode.

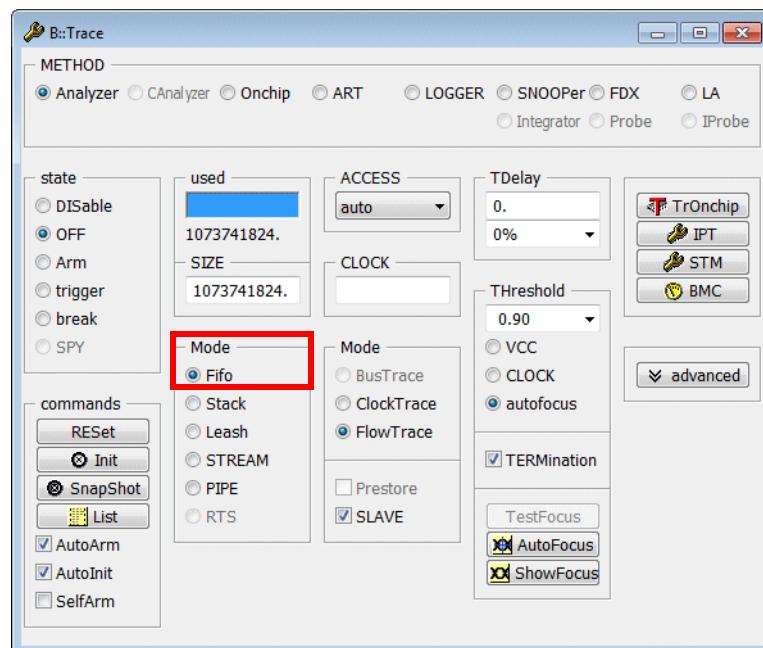
If the **Trace.METHOD Onchip** is selected only Fifo mode can be used:

- **Fifo:** allows to record as much trace records as indicated in the **SIZE** field of the Trace Configuration window.



Trace.Mode Fifo

```
; default mode
; when the trace memory is full
; the newest trace information will
; overwrite the oldest one
; the trace memory contains all
; information generated until the
; program execution stopped
```



The screenshot shows the 'B:Trace.List' window displaying a list of trace records. The table has columns: record, run, address, cycle, data, symbol, and ti.back. A red arrow points from the text 'In Fifo mode negative record numbers are used. The last record gets the smallest negative number.' to the 'record' column, which shows values like 366, -0000000082, 368, 369, and 368. The 'symbol' column shows assembly code for a loop, and the 'ti.back' column shows the file path and timestamp. The 'More' and 'Less' buttons are visible at the top of the window.

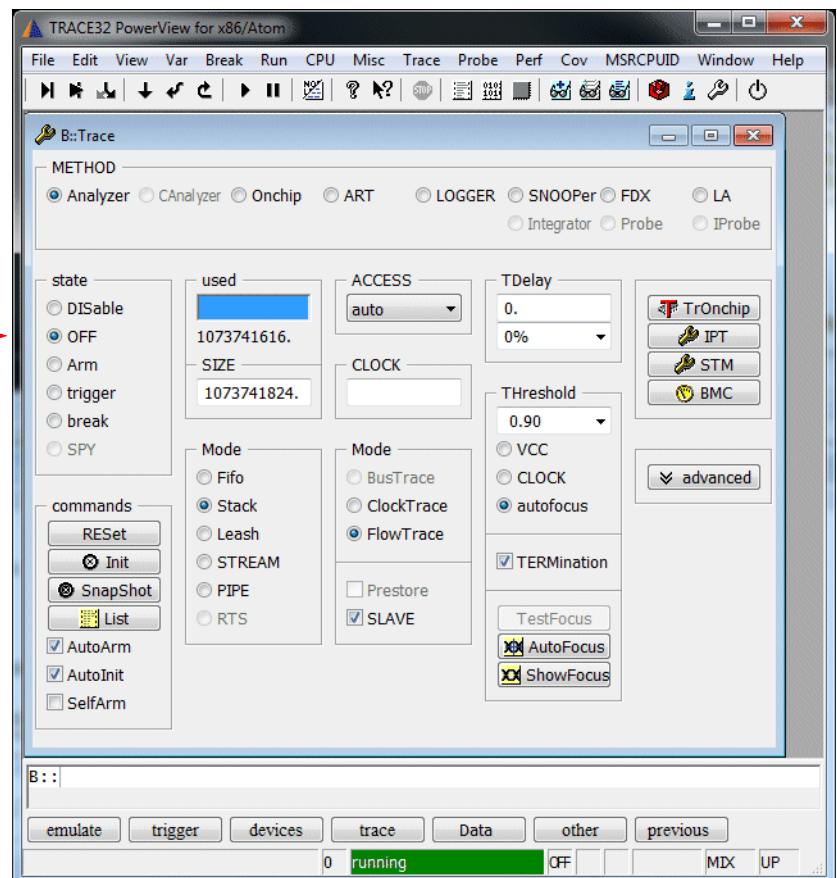
record	run	address	cycle	data	symbol	ti.back
366	0	add	ebx,esi		for (v2 = 0 ; v2 < 3 ; v2++)	
0	0	add	esi, +0x1		esi, +0x1	
0	0	cmp	esi, +0x2		esi, +0x2	
0	0	jle	0x8048583		0x8048583	
-0000000082	368				NP:0000000000804858D ptrace	
368	0	for	(v3 = 0 ; v3 < 3 ; v3++)		for (v3 = 0 ; v3 < 3 ; v3++)	..\sieve_funcs\func10+0x3D <0.005us
0	0	mov	esi, 0x0		mov esi, 0x0	
0	0	jmp	0x8048599		jmp 0x8048599	
0	0	cmp	esi, +0x2		cmp esi, +0x2	
0	0	jle	0x8048594		jle 0x8048594	
369	0		v17 += v3;		v17 += v3;	
368	0	add	ebx,esi		add ebx,esi	
0	0	add	esi, +0x1		for (v3 = 0 ; v3 < 3 ; v3++)	
0	0	cmp	esi, +0x2		cmp esi, +0x2	
0	0	jle	0x8048594		jle 0x8048594	
369	0		v17 += v3;		v17 += v3;	

In Fifo mode negative record numbers are used. The last record gets the smallest negative number.

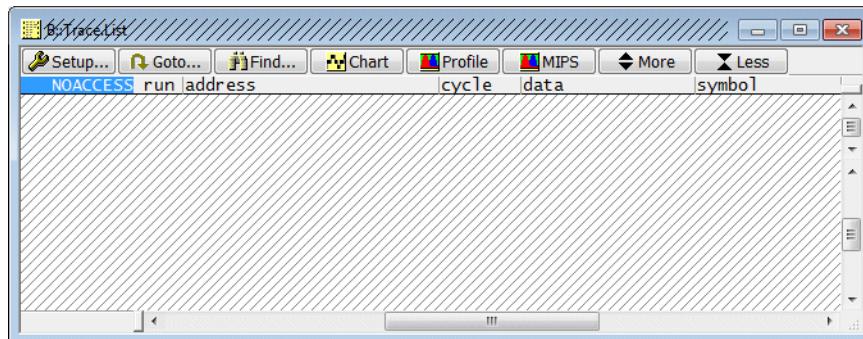
Trace.Mode Stack

; when the trace memory is full
; the trace recording is stopped

; the trace memory contains all
; information generated directly
; after the start of the program
; execution



TRACE32 needs to read the program code from the target memory in order to display the core trace information. This is not possible while the program execution is running. This is the reason why the **Trace.List** window indicates **NOACCESS**.

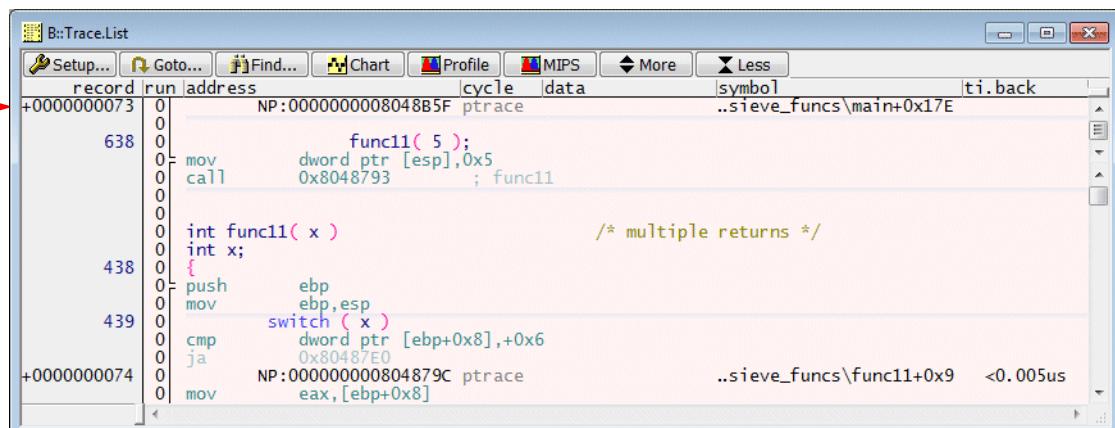


Stop the program execution to allow TRACE32 to read the program code from the target. Or if you need to display the core trace information while the program execution is running, load a copy of the program code to the [TRACE32 Virtual Memory](#).

Data.LOAD.Elf <file> /PlusVM

Load the program code to the target and to the TRACE32 Virtual Memory.

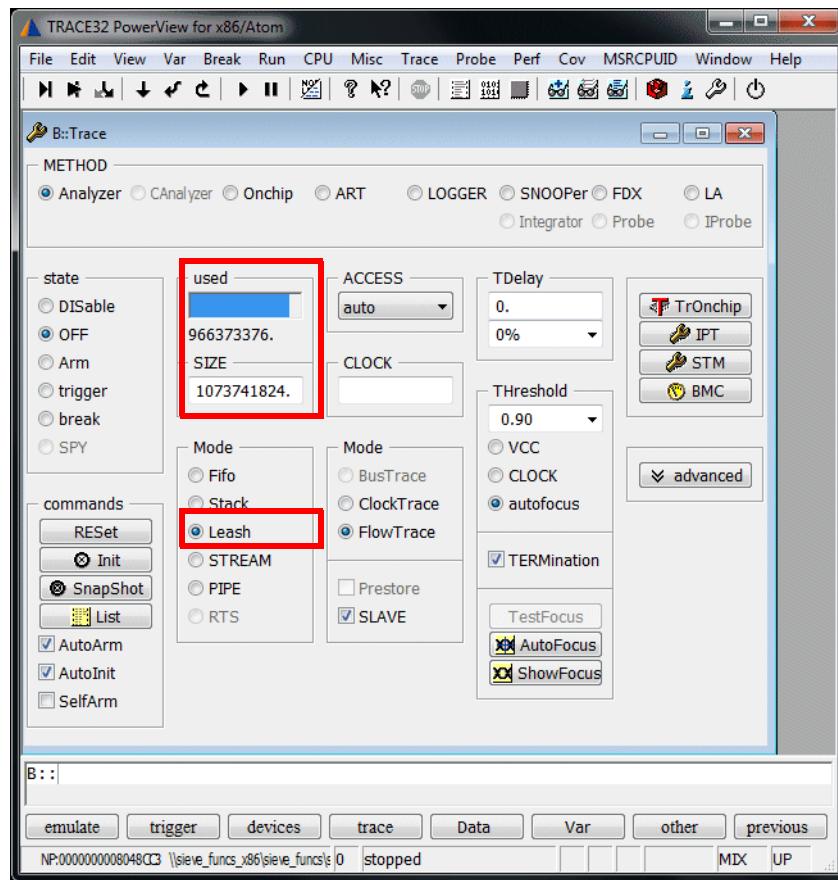
Since the trace recording starts with the program execution and stops, when the trace memory is full, positive record numbers are used in **Stack** mode. The first record in the trace gets the smallest positive number.



Trace.Mode Leash

; when the trace memory is nearly
; full the program execution is
; stopped

; Leash mode uses the same record
; numbering scheme as Stack mode



The program execution is **stopped** as soon as
the trace buffer is nearly full.

Since stopping the program execution when the trace
buffer is nearly full requires some logic/time, **used** is
smaller than the maximum **SIZE**.

```
Trace.Mode STREAM ; stream the recorded trace
; information to a file on the host
; computer

; STREAM mode uses the same record
; numbering scheme as Stack mode
```

The trace information is immediately streamed to a file on the host computer after it was placed into the trace memory. This procedure extends the size of the trace memory to several T Frames.

- STREAM mode requires a 64-bit host computer and a 64-bit TRACE32 executable to handle the large trace record numbers.

By default the streaming file is placed into the TRACE32 temp. directory ([OS.PresentTemporaryDirectory\(\)](#)).

The command **Trace.STREAMFILE** <file> allows to specify a different name and location for the streaming file.

```
Trace.STREAMFILE d:\temp\mystream.t32 ; specify the location for
; your streaming file
```

TRACE32 stops the streaming when less then 1 GByte free memory is left on the drive by default.

The command **Trace.STREAMFileLimit** <+/- limit in bytes> allows a user-defined free memory limitation.

```
Trace.STREAMFileLimit 5000000000. ; streaming file is limited to
; 5 GByte

Trace.STREAMFileLimit -5000000000. ; streaming is stopped when less
; the 5 GByte free memory is left
; on the drive
```

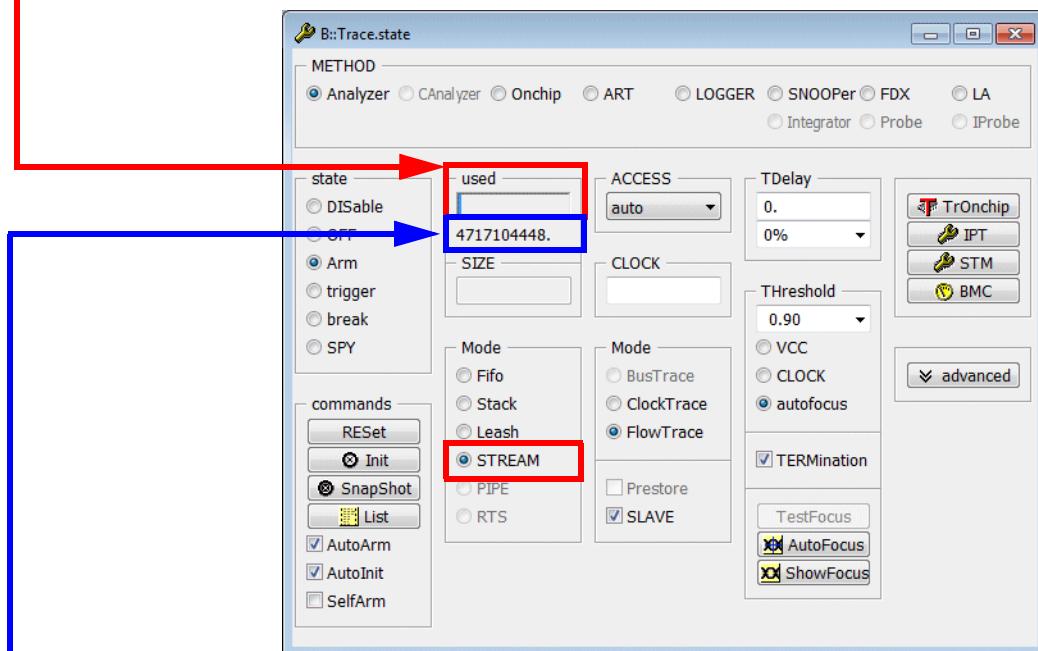
Please be aware that the streaming file is deleted as soon as you de-select the STREAM mode or when you exit TRACE32.

At high data rates your host computer might have problems saving the trace data to the streaming file. The command **Trace.STREAMCompression** allow to configure a better compression.

Trace.STREAMCompression HIGH

In STREAM mode the **used** field is split:

Number of records buffered by the trace memory of POWER TRACE II / POWER TRACE III



Number of records saved to streaming file

record	run	address	cycle	data	symbol	ti.back
698	0	mov byte ptr [esi+0x8049328],0x0			k += primz;	
695	0	add esi,edi			while (k <= SIZE)	
+00001416618712	0	cmp esi,+0x12			NP:0000000008048CEO ptrace	
	0	jle 0x8048CD2			}	
700	0	add dword ptr [ebp-0x10],+0x1			anzahl++;	
689	0	for (i = 0 ; i <= SIZE ; i++)				
	0	add ebx,+0x1				
	0	cmp ebx,+0x12				

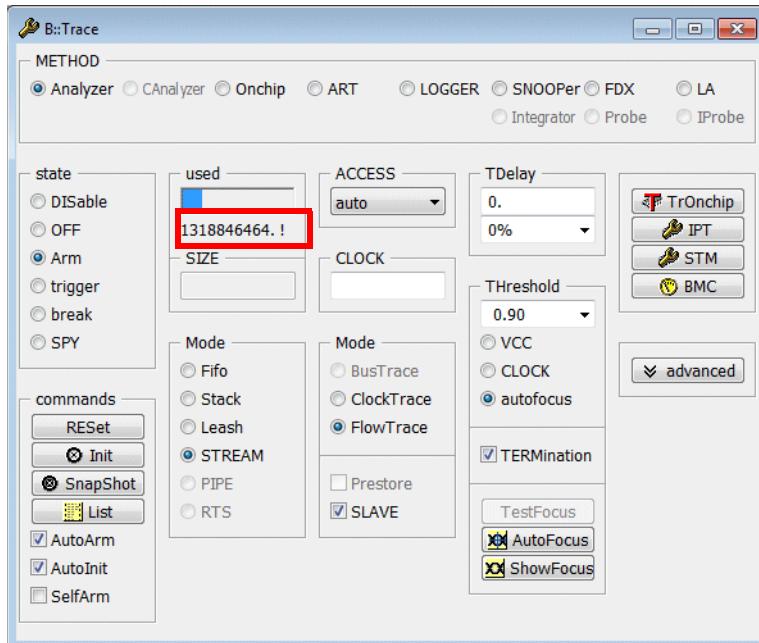
STREAM mode can generate very large record numbers

STREAM mode can only be used if the average data rate at the trace port does not exceed the maximum transmission rate of the host interface in use. Peak loads at the trace port are intercepted by the memory in POWER TRACE II / POWER TRACE III, which can be considered to be operating as a large FIFO.

If the average data rate at the trace port exceeds the maximum transmission rate of the host interface in use, a **PowerTrace FIFO Overrun** occurs. TRACE32 stops streaming and empties the POWER TRACE II / POWER TRACE III FIFO. Streaming is re-started after the POWER TRACE II / POWER TRACE III FIFO is empty.

A **PowerTrace FIFO Overrun** is indicated as follows:

1. A **!** in the **used** area of the Trace Configuration window indicates an overrun of the POWER TRACE II / POWER TRACE III FIFO.



2. The OVERRUN is indicated in all trace display windows.

OVERRUN	run	address	cycle	data	symbol	ti.back
689	0	je 0x8048CE4				
	0	for (i = 0 ; i <= SIZE ; i++)				
	0	add ebx,+0x1				
	0	cmp ebx,+0x12				
	0	jle 0x8048CBC				
+0588212177	0	NP:000000008048CBC ptrace			..\\sieve+0x2D	21.475s
691	0	{				
	0	if (flags[i])				
	0	eax,byte ptr [ebx+0x8049328]				
	0	test al,al				
	0	je 0x8048CE4				
	0	}				

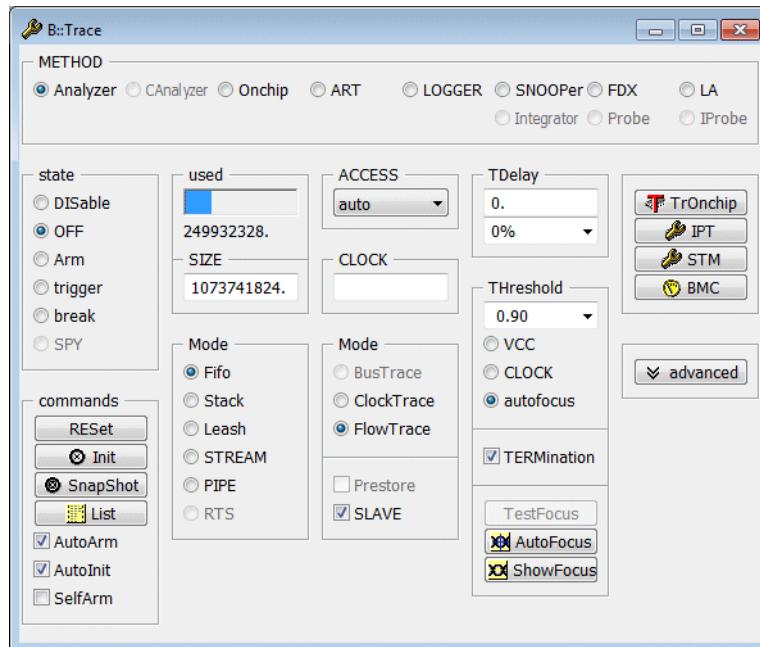
OVERRUNs are not visible at record level.

A large **ti.back** value (**tool timestamp** only) can be considered as an OVERRUN indicator.

```
Trace.FindAll TIme.Back 10.s--50.s ; find all trace records with
; a timestamp between 10.s and
; 50.s
```

States of the Trace

The trace buffer can either sample or allows the read-out for information display.



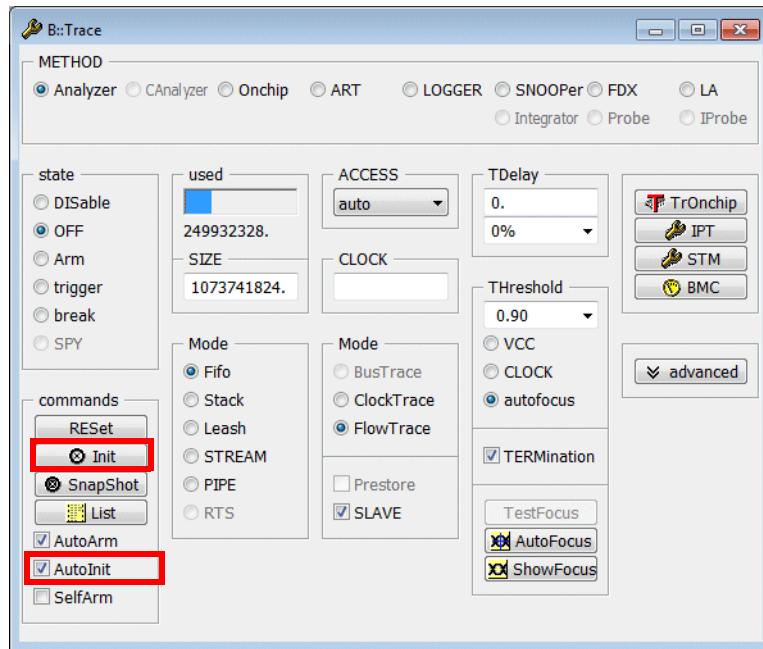
States of the Trace	
DISable	The trace is disabled.
OFF	The trace is not sampling. The trace contents can be analyzed and displayed.
Arm	The trace is sampling. There is no access to the trace contents.

The current state of the trace is always indicated in the **Trace State** field of the TRACE32 state line.



Since Intel® PT does not provide a mean to indicate a trigger, the Trace states **trigger** and **break** are never reached.

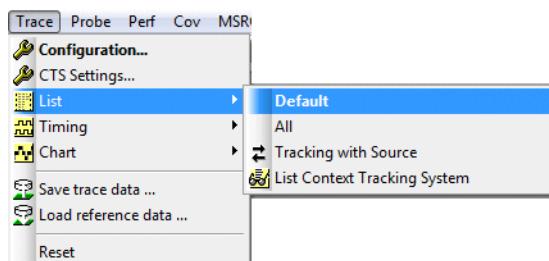
The AutoInit Command



Init Button	Clear the trace memory. All other settings in the Trace configuration window remain valid.
AutoInit CheckBox	ON: The trace memory is cleared whenever the program execution is started (Go, Step).

Basic Display Commands

Default Listing



Conditional branch taken

Timing information

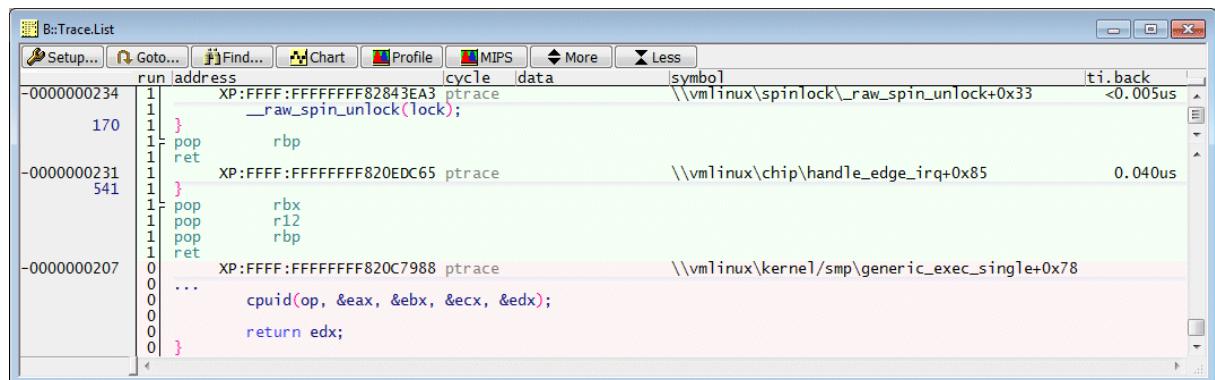
The screenshot shows the B::Trace.List window with assembly code and timing information. The assembly code is as follows:

record	run	address	cycle	data	symbol	ti.back
689	0	for (i = 0 ; i <= SIZE ; i++)				
	0	add				
	0	cmp				
	0	jle 0x8048C8C				
-0111449584	0	NP:0000000008048C8C	ptrace		..\\sieve+0x2D	0.010us
	0	{				
	0	if (flags[i])				
	0	movzx eax,byte ptr [ebx+0x8049328]				
	0	test al,al				
	0	je 0x8048C8E				
	0	primz = i + i + 3;				
	0	lea eax,[ebx+ebx]				
	0	edi,[eax+0x3]				
	0	k = i + primz;				
	0	esi,[edi+ebx]				
	0	lea esi,[edi+ebx]				
	0	jmp 0x8048CDB				
	0	while (k <= SIZE)				
	0	cmp esi,+0x12				
	0	je 0x8048CD2				

Annotations in the screenshot highlight specific assembly instructions and their timing information. Red boxes are placed around the 'jle' instruction at address 0x8048C8C and the 'je' instruction at address 0x8048C8E. A red box also surrounds the timing value '0.010us' for the 'jle' instruction. A red line connects the 'jle' instruction in the assembly code to the 'Conditional branch taken' text above. Another red line connects the 'je' instruction in the assembly code to the 'Conditional branch not taken (pastel printed)' text below. The 'je' instruction is printed in pastel colors.

Conditional branch not taken
(pastel printed)

The trace information for all cores is displayed by default in the **Trace.List** window. The column **run** and the coloring of the trace information are used for core indication.

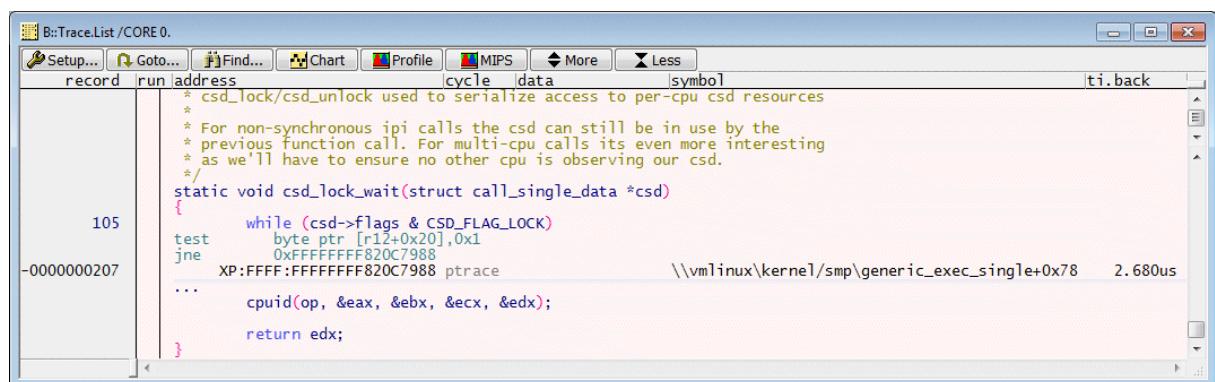


The screenshot shows the **Trace.List** window with the following trace entries:

run	address	cycle	data	symbol	ti.back
-0000000234 170	XP:FFFF:FFFFFFF82843EA3 ptrace } __raw_spin_unlock(lock); pop rbp ret			\\vmlinux\\spinlock_raw_spin_unlock+0x33	<0.005us
-0000000231 541	XP:FFFF:FFFFFFF820EDC65 ptrace } pop rbx pop r12 pop rbp ret			\\vmlinux\\chip\\handle_edge_irq+0x85	0.040us
-0000000207	XP:FFFF:FFFFFFF820C7988 ptrace ... cpuid(op, &eax, &ebx, &ecx, &edx); return edx;			\\vmlinux\\kernel\\smp\\generic_exec_single+0x78	

Trace.List /CORE <n>

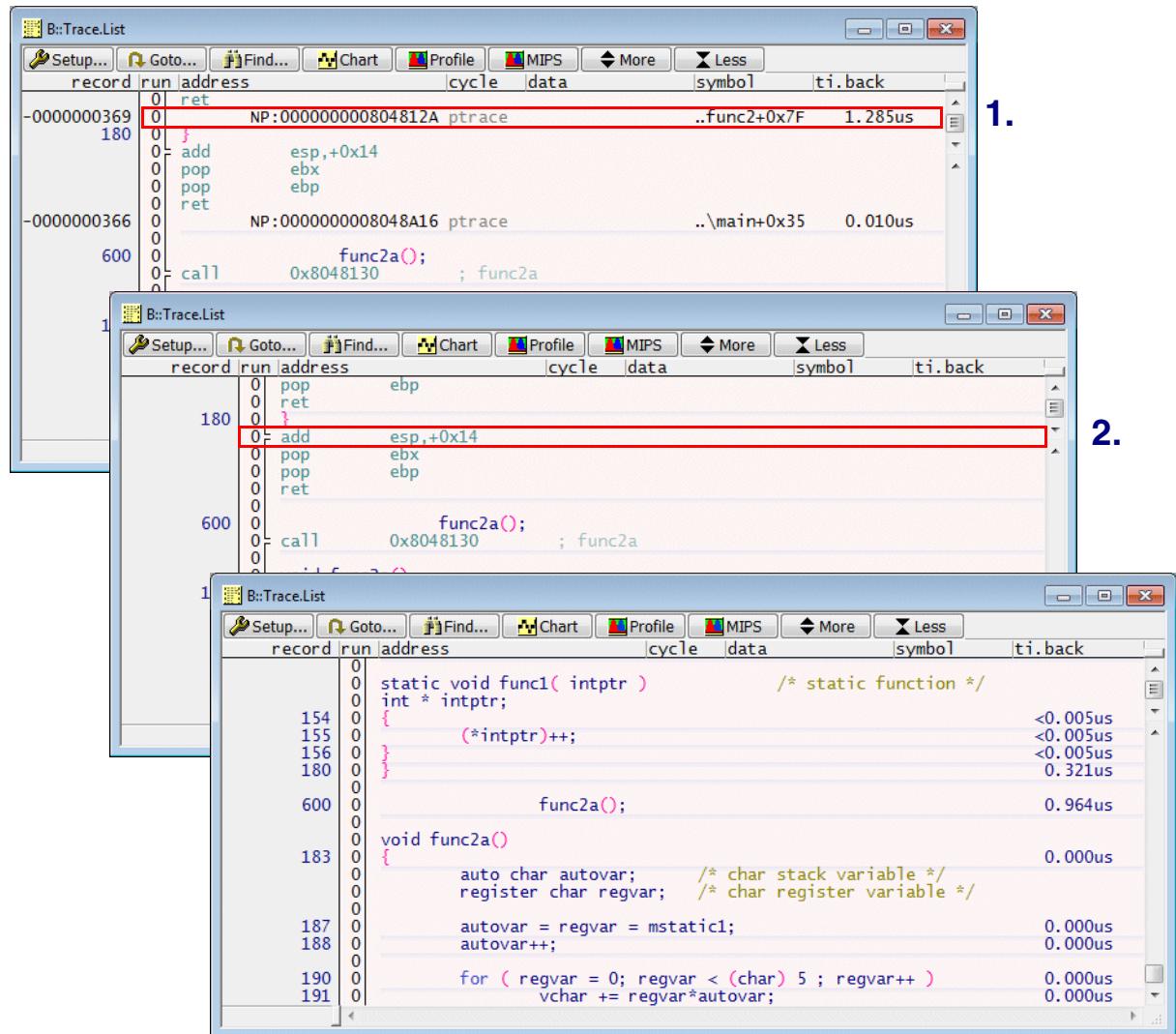
The option **CORE** allows a per core display of the trace information.



The screenshot shows the **Trace.List /CORE 0** window with the following trace entries:

record	run address	cycle	data	symbol	ti.back
105	* csd_lock/csd_unlock used to serialize access to per-cpu csd resources * * For non-synchronous ipi calls the csd can still be in use by the * previous function call. For multi-cpu calls its even more interesting * as we'll have to ensure no other cpu is observing our csd. */ static void csd_lock_wait(struct call_single_data *csd) { while (csd->flags & CSD_FLAG_LOCK) test byte ptr [r12+0x20],0x1 jne 0xFFFFFFFFF820C7988 XP:FFFF:FFFFFFF820C7988 ptrace ... cpuid(op, &eax, &ebx, &ecx, &edx); return edx;			\\vmlinux\\kernel\\smp\\generic_exec_single+0x78	2.680us
-0000000207					

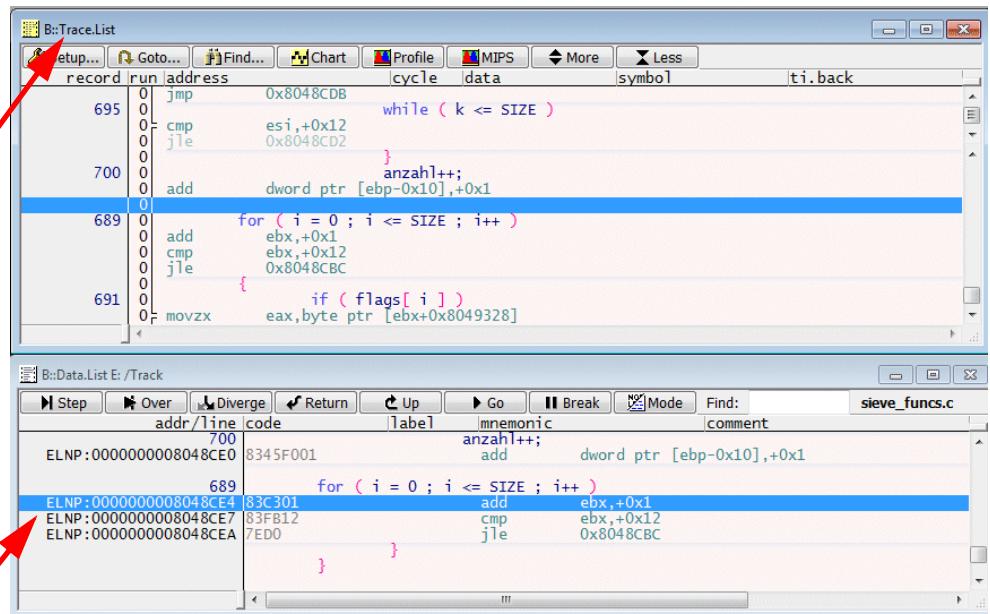
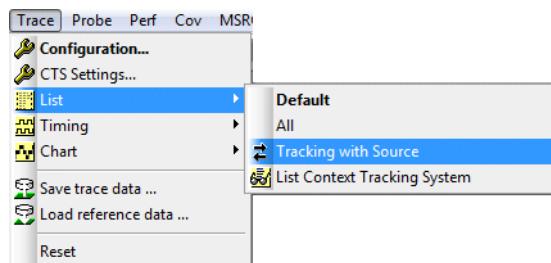
Basic Formatting



1. time Less	Suppress the display of the ptrace packets.
2. time Less	Suppress the display of the assembly code.

The **More** button works vice versa.

Correlating the Trace Listing with the Source Listing

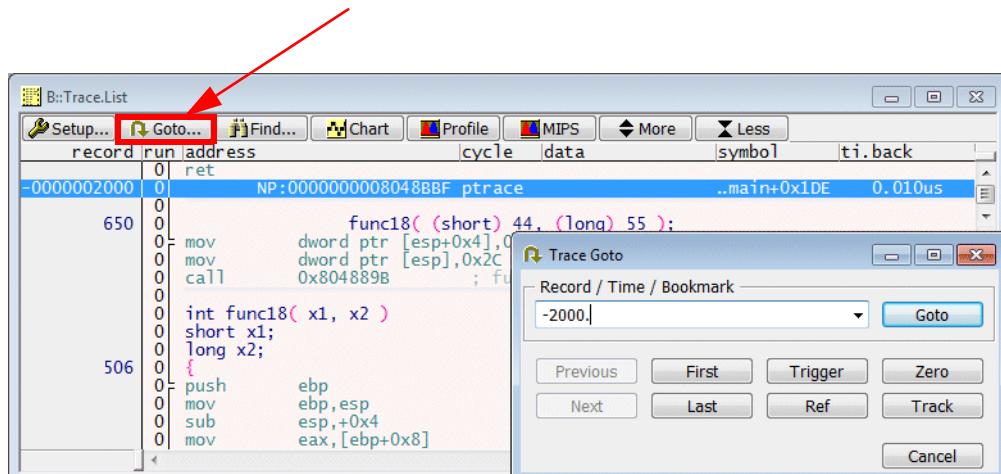


Active Window

All windows opened with
the **/Track** option follow the
cursor movements in the
active window

Tracking between the Trace Listing and the Source Listing is based on the program addresses.

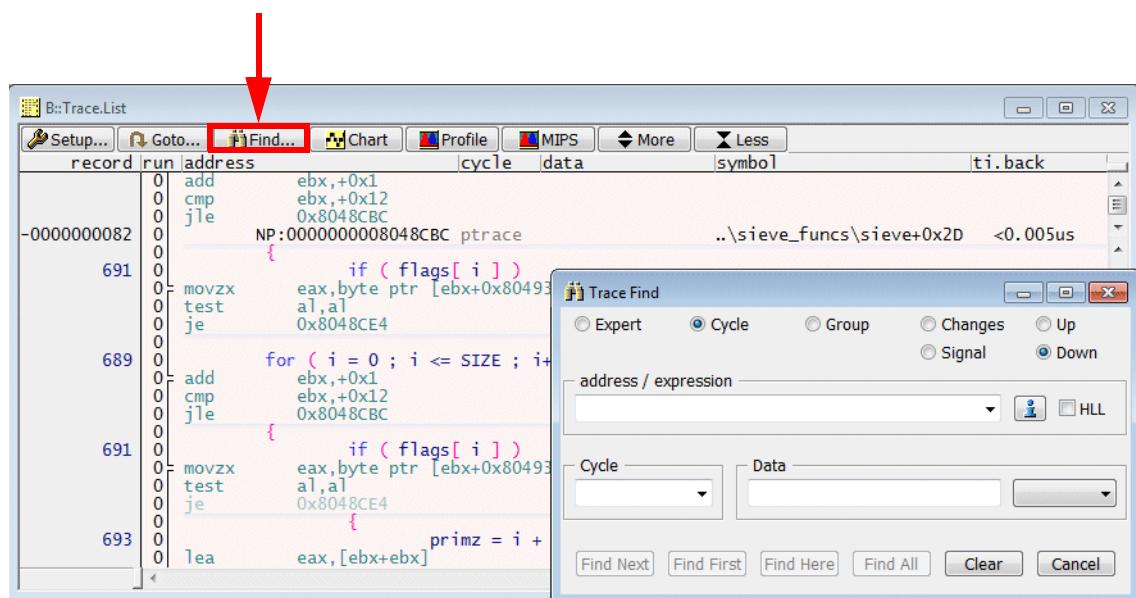
Browsing through the Trace Buffer



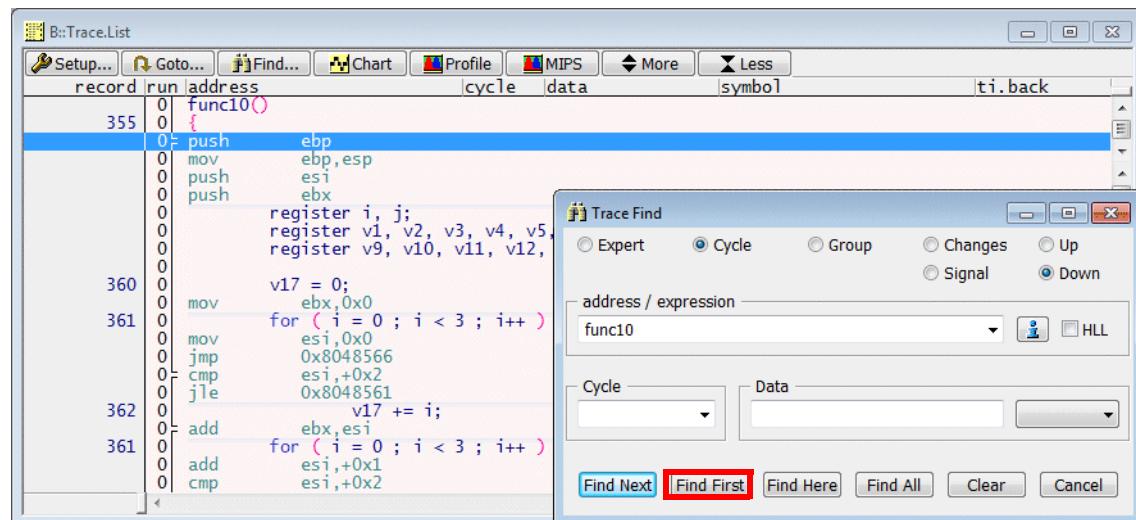
Pg ↑	Scroll page up.
Pg ↓	Scroll page down.
Ctrl - Pg ↑	Go to the first record sampled in the trace buffer.
Ctrl - Pg ↓	Go to the last record sampled in the trace buffer.

Find a Specific Record

The **Trace.List** window provides a “Find...” button to open the **Trace Find** dialog. The **Trace Find** dialog allows to search for events of interest in the trace.



Example: Find the entry to the function func10.



A detailed description of the **Trace Find dialog** can be found in “[Application Note for Trace.Find](#)” (app_trace_find.pdf).

Display Items

Default Display Items

record	run	address	cycle	data	symbol	ti.back
-0111449333	0	NP:0000000008048B5A	ptrace		..main+0x179	1.175us
636	0	0	func10()	0x8048550	; func10	
355	0	0	func10()	{		
	0	0	push	ebp		
	0	0	mov	ebp,esp		
	0	0	push	esi		
	0	0	push	ebx		
	0	0	register	i, j;		
	0	0	register	v1, v2, v3, v4, v5, v6, v7, v8;		
	0	0	register	v9, v10, v11, v12, v13, v14, v15, v16, v17;		
	0	0				

- **Column record**

Displays the record numbers

- **Column run**

The column run displays some graphic element to provide a quick overview on the instruction execution sequence.

Trace.List List.ADDRESS DEFault

Sequential
program execution
(solid line)
Non-sequential
program execution
(broken line)

record	run	address	cycle	data	symbol
691	0	{			
	0	if (flags[i])			
	0	NP:0000000008048CBC	movzx		eax,byte ptr [ebx+0x8049328]
	0	NP:0000000008048CC3	test		al,al
	0	NP:0000000008048CC5	je		0x8048CE4
	0	{			
	693	primz = i + i + 3;			
	0	NP:0000000008048CC7	lea		eax,[ebx+ebx]
	0	NP:0000000008048CCA	lea		edi,[eax+0x3]
	694	k = i + primz;			
	0	NP:0000000008048CCD	lea		esi,[edi+ebx]
	695	while (k <= SIZE)			
	0	NP:0000000008048CD0	jmp		0x8048CDB
	695	NP:0000000008048CD8	while (k <= SIZE)		
	0	NP:0000000008048CDB	cmp		esi,+0x12
	700	NP:0000000008048CDE	jle		0x8048CD2
	0	}			
	0	anzahl++;			
	0	!!!			

The column run also indicates Interrupts and TRAPs.

B::Trace.List

	Setup...	Goto...	Find...	Chart	Profile	MIPS	More	Less	
	run	address		cycle	data	symbol			ti.back
-0193607871	0	static void csd_lock_wait(struct call_single_data *csd)							
	105	0	while (csd->flags & CSD_FLAG_LOCK)						
		0	test byte ptr [r12+0x20],0x1						
		0	interrupt						
		0	XP:FFFF:FFFFFFFF8284AD80 ptrace						
		0	nop						
		0	reboot_interrupt smp_reboot_interrupt						
		0	#endif						
		0	#endif						
		0	#endif						

- **Column cycle**
The main cycle type is:
 - ptrace (program trace info)
- **Column address/symbol**

record	run	address	cycle	data	symbol	ti.back
-0111449333	0	NP:000000000804885A	ptrace		..main+0x179	1.175us
636	0		func10();			
	0	call 0x8048550			; func10	
355	0	func10()				
	0	{				
	0	push ebp				
	0	mov ebp,esp				
	0	push esi				
	0	push ebx				
	0	register i, j;				
	0	register v1, v2, v3, v4, v5, v6, v7, v8;				
	0	register v9, v10, v11, v12, v13, v14, v15, v16, v17;				
	0					

The **address** column shows the following information:

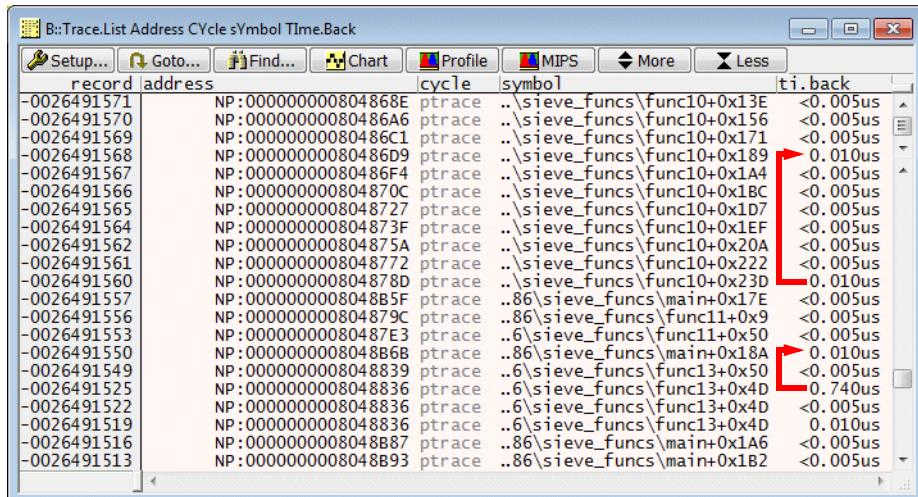
<access class>:<address>

Access Classes	
NP	Program address in 32-bit Protected Mode
XP	Program address in 64-bit mode

Information on the other available access classes can be found in [“Intel® x86/x64 Debugger” \(debugger_x86.pdf\)](#).

The **symbol column** shows the corresponding symbolic address.

- **Column *ti.back***



record	address	cycle	symbol	ti.back
-0026491571	NP:0000000000804868E	ptrace	..\sieve_funcs\func10+0x13E	<0.005us
-0026491570	NP:000000000080486A6	ptrace	..\sieve_funcs\func10+0x156	<0.005us
-0026491569	NP:000000000080486C1	ptrace	..\sieve_funcs\func10+0x171	<0.005us
-0026491568	NP:000000000080486D9	ptrace	..\sieve_funcs\func10+0x189	0.010us
-0026491567	NP:000000000080486F4	ptrace	..\sieve_funcs\func10+0x1A4	<0.005us
-0026491566	NP:0000000000804870C	ptrace	..\sieve_funcs\func10+0x1BC	<0.005us
-0026491565	NP:00000000008048727	ptrace	..\sieve_funcs\func10+0x1D7	<0.005us
-0026491564	NP:0000000000804873F	ptrace	..\sieve_funcs\func10+0x1EF	<0.005us
-0026491562	NP:0000000000804875A	ptrace	..\sieve_funcs\func10+0x20A	<0.005us
-0026491561	NP:00000000008048772	ptrace	..\sieve_funcs\func10+0x222	<0.005us
-0026491560	NP:0000000000804878D	ptrace	..\sieve_funcs\func10+0x23D	0.010us
-0026491557	NP:00000000008048B5F	ptrace	..86\sieve_funcs\main+0x17E	<0.005us
-0026491556	NP:0000000000804879C	ptrace	..86\sieve_funcs\func11+0x9	<0.005us
-0026491553	NP:000000000080487E3	ptrace	..6\sieve_funcs\func11+0x50	<0.005us
-0026491550	NP:00000000008048B6B	ptrace	..86\sieve_funcs\main+0x18A	0.010us
-0026491549	NP:00000000008048839	ptrace	..6\sieve_funcs\func13+0x50	<0.005us
-0026491525	NP:00000000008048836	ptrace	..6\sieve_funcs\func13+0x4D	0.740us
-0026491522	NP:00000000008048836	ptrace	..6\sieve_funcs\func13+0x4D	<0.005us
-0026491519	NP:00000000008048836	ptrace	..6\sieve_funcs\func13+0x4D	0.010us
-0026491516	NP:00000000008048B87	ptrace	..86\sieve_funcs\main+0x1A6	<0.005us
-0026491513	NP:00000000008048B93	ptrace	..86\sieve_funcs\main+0x1B2	<0.005us

The **ti.back** column shows the time distance to the previous timestamped record.

For details on the TRACE32 tool timestamp refer to “[Tool Timestamp \(POWER TRACE II / POWER TRACE III only\)](#)”, page 8.

Further Display Items

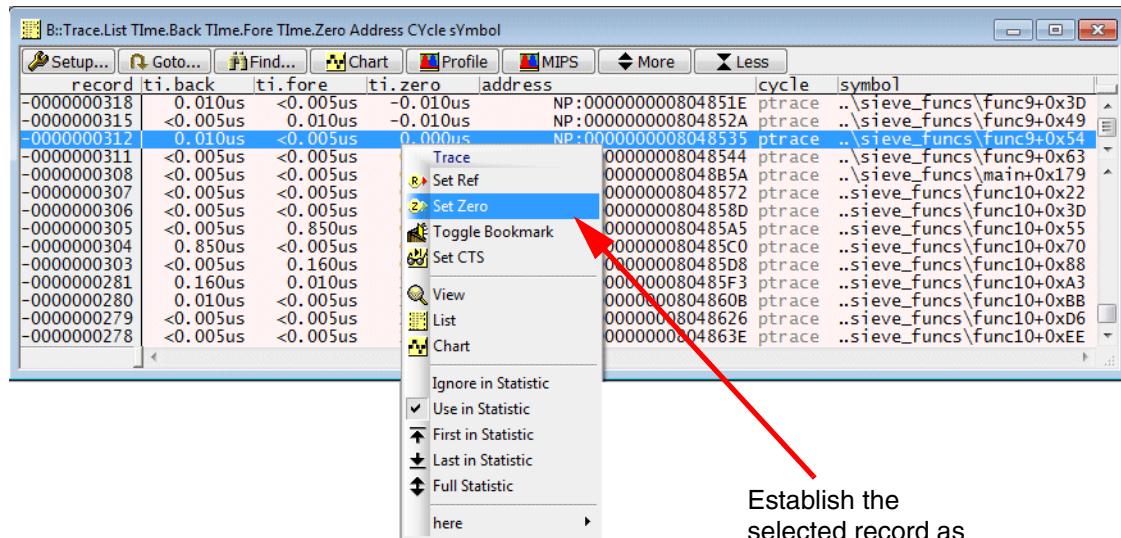
Time Information

Tlme.Back	Time relative to the previous record (red)
Tlme.Fore	Time relative to the next record (green).
Tlme.Zero	Time relative to the global zero point.

Trace.List Tlme.Back Tlme.Fore Tlme.Zero Address CYcle sYmbol

record	ti.back	ti.fore	ti.zero	address	cycle	symbol
-0000000332	<0.005us	<0.005us	-0.030us	NP:0000000008048B28	ptrace	..\sieve_funcs\main+0x147
-0000000329	<0.005us	0.010us	-0.030us	NP:0000000008048B4E	ptrace	..\sieve_funcs\main+0x16D
-0000000326	0.010us	<0.005us	-0.020us	NP:0000000008048B55	ptrace	..\sieve_funcs\main+0x174
-0000000329	<0.005us	<0.005us	-0.020us	NP:0000000008048507	ptrace	..\sieve_funcs\func9+0x26
-0000000322	<0.005us	0.010us	-0.020us	NP:0000000008048513	ptrace	..\sieve_funcs\func9+0x32
-0000000318	0.010us	<0.005us	-0.010us	NP:000000000804851E	ptrace	..\sieve_funcs\func9+0x3D
-0000000315	<0.005us	0.010us	-0.010us	NP:000000000804852A	ptrace	..\sieve_funcs\func9+0x49
-0000000312	0.010us	<0.005us	0.000us	NP:0000000008048535	ptrace	..\sieve_funcs\func9+0x54
-0000000311	<0.005us	<0.005us	0.000us	NP:0000000008048544	ptrace	..\sieve_funcs\func9+0x63
-0000000308	<0.005us	<0.005us	0.000us	NP:0000000008048B5A	ptrace	..\sieve_funcs\main+0x179
-0000000307	<0.005us	<0.005us	0.000us	NP:0000000008048572	ptrace	..\sieve_funcs\func10+0x22
-0000000306	<0.005us	<0.005us	0.000us	NP:000000000804858D	ptrace	..\sieve_funcs\func10+0x3D
-0000000305	<0.005us	0.850us	0.000us	NP:00000000080485A5	ptrace	..\sieve_funcs\func10+0x55
-0000000304	0.850us	<0.005us	0.850us	NP:00000000080485C0	ptrace	..\sieve_funcs\func10+0x70
-0000000303	<0.005us	0.160us	0.850us	NP:00000000080485D8	ptrace	..\sieve_funcs\func10+0x88
-0000000281	0.160us	0.010us	1.010us	NP:00000000080485F3	ptrace	..\sieve_funcs\func10+0xA3
-0000000280	0.010us	<0.005us	1.020us	NP:000000000804860B	ptrace	..\sieve_funcs\func10+0xBB
-0000000279	<0.005us	<0.005us	1.020us	NP:0000000008048626	ptrace	..\sieve_funcs\func10+0xD6
-0000000278	<0.005us	<0.005us	1.020us	NP:000000000804863E	ptrace	..\sieve_funcs\func10+0xEE
-0000000277	<0.005us	<0.005us	1.020us	NP:0000000008048659	ptrace	..\sieve_funcs\func10+0x109
-0000000276	<0.005us	<0.005us	1.020us	NP:0000000008048671	ptrace	..\sieve_funcs\func10+0x121
-0000000275	<0.005us	<0.005us	1.020us	NP:000000000804868E	ptrace	..\sieve_funcs\func10+0x13E
-0000000274	<0.005us	<0.005us	1.020us	NP:00000000080486A6	ptrace	..\sieve_funcs\func10+0x156
-0000000273	<0.005us	0.010us	1.020us	NP:00000000080486C1	ptrace	..\sieve_funcs\func10+0x171

Set the Global Zero Point (PowerTrace II only)



ZERO.RESET
(tool timestamp only)

Tlme.Zero is the zero point of the timestamp counter commonly used by all TRACE32 hardware modules.

ZERO.offset <time>

Tlme.Zero is the zero point of the timestamp counter commonly used by all TRACE32 hardware modules minus the specified <time>.

```
PRINT Trace.RECORD.TIME(-99.)
```

```
; print the timestamp of  
; record -99.
```

```
ZERO.offset Trace.RECORD.TIME(-99.)
```

```
; specify the time of record  
; -99. as global zero point
```

- **Cycle Accurate Tracing Pros.**

Provides how much core clocks it took to execute a program section.

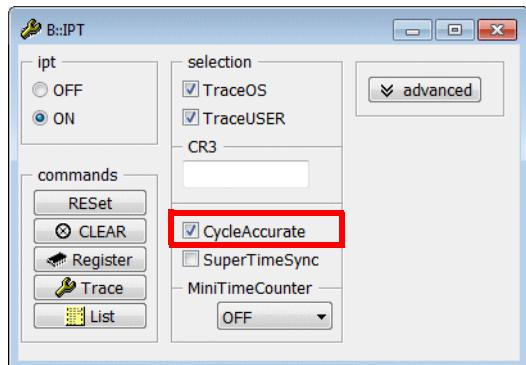
Allows to synchronize traces from different trace sources if Time Synchronization packets are available (not implemented yet).

- **Cycle Accurate Tracing Cons.**

Cycle accurate tracing requires up 2 times more bandwidth.

Cycle accurate tracing and changing core clock while recording

Cycle accurate tracing has to be enabled in the IPT configuration window.



IPT.CycleAccurate ON

Advise Intel® PT to generate cycle count information.

```
; advise TRACE32 to display a trace listing with
; cycle count information (CLOCKS.Back)
; advise TRACE32 to suppress the display
; of the timestamp information (TIme.Back.OFF)
Trace.List CLOCKS.Back DEFault TIme.Back.OFF
```

The following command allows to specify this display as default for the **Trace.List** window.

```
SETUP.ALIST CLOCKS.Back DEFault TIme.Back.OFF
```



TRACE32 displays the warning above when the recorded trace information is analyzed and displayed the first time. This warning points out that all displayed time information (TIme.Back, TIme.Zero) might be inaccurate.

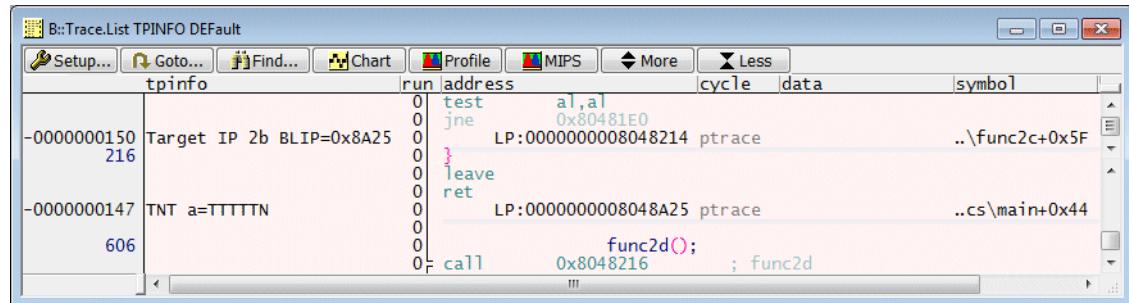
B::Trace.List CLOCKS.Back DEFAULT Time.Back.OFF

		run	address	cycle	data	symbol
-0000000303	11.	0	add ebx, +0x1 0 cmp ebx, +0x12 0 jle 0x8048CBC	LP:0000000008048CEC	ptrace	..sieve_funcs\sieve+0x5D
		0	}		}	
704		0	return anzahl;			
705		0	mov eax, [ebp-0x10]			
		0	}			
		0	add esp, +0x10			
		0	pop ebx			
		0	pop esi			
		0	pop edi			
		0	pop ebp			
-0000000299	24.	0	ret	LP:0000000008048C80	ptrace	..sieve_funcs\main+0x29F
		0	/* func40(); */			
670		0	for (j = 0; j < 10; j++)			
		0	add dword ptr [ebp-0x0C], +0x1			
		0	cmp dword ptr [ebp-0x0C], +0x9			
		0	jle 0x8048C7B			

24.

Cycle count information
relative to the previous record

```
; advise TRACE32 to display a trace listing with the decoded trace packet
; (TPINFO)
Trace.List TPINFO DEFault
```



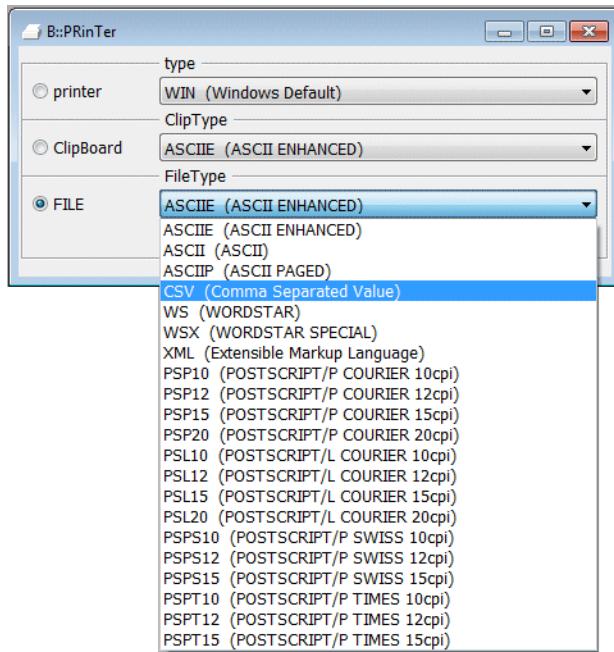
The screenshot shows a software window titled "B::Trace.List TPINFO DEFault". The window has a toolbar with icons for Setup, Goto, Find, Chart, Profile, MIPS, More, and Less. The main area is a table with columns: run, address, cycle, data, and symbol. The table contains two rows of trace data. The first row is for a target IP at 0x8A25, and the second row is for a target IP at 0x8A25. The assembly code shown includes test, jne, leave, ret, and call instructions, along with their addresses and symbols.

run	address	cycle	data	symbol
-0000000150 216	0 test a1,a1 0 jne 0x80481E0 0 } 0 leave 0 ret	LP:0000000008048214	ptrace	..\func2c+0x5F
-0000000147 606	0 func2d(); 0 r call 0x8048216	LP:0000000008048A25	ptrace	..cs\main+0x44

Belated Trace Analysis

There are several ways for a belated trace analysis:

1. Save a part of the trace contents into a file (ASCII, CSV or XML format) and analyze this trace contents outside of TRACE32 PowerView.

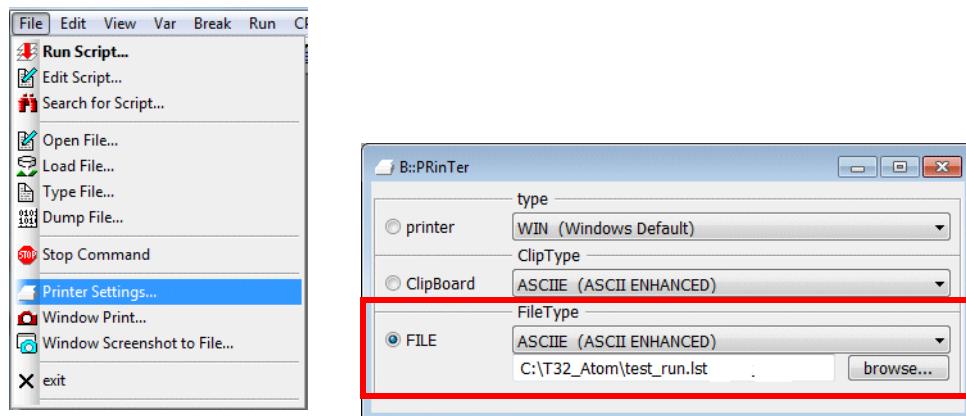


2. Save the trace contents in a compact format into a file. Load the trace contents at a subsequent date into a TRACE32 Instruction Set Simulator and analyze it there.
3. Export the STP byte stream to postprocess it with an external tool.

Save the Trace Information to an ASCII File

Saving a part of the trace contents to an ASCII file requires the following steps:

1. Select **Printer Setting...** in the **File** menu to specify the file name and the output format.



```
PRinTer.FileType ASCIIIE ; specify output format
                           ; here enhanced ASCII
PRinTer.FILE test_run.lst ; specify the file name
```

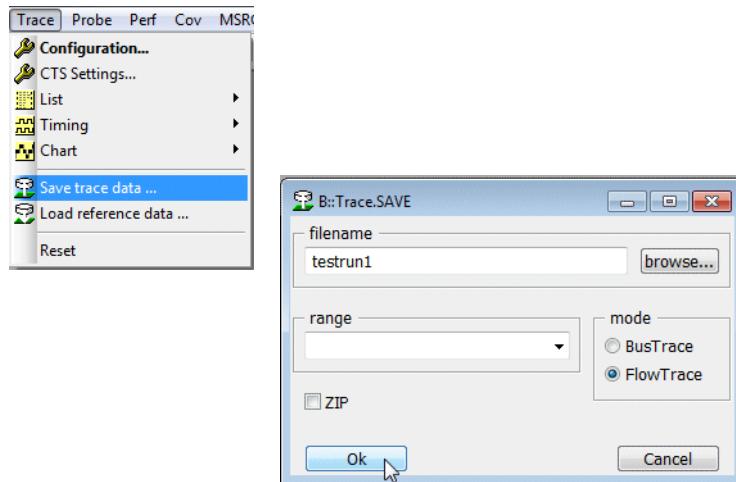
2. It might make sense to save only a part of the trace contents into the file. Use the record numbers to specify the trace part you are interested in.

TRACE32 provides the command prefix **WinPrint.** to redirect the result of a display command into a file.

```
; save the trace record range (-8976.)--(-2418.) into the
; specified file
WinPrint.Trace.List (-8976.)--(-2418.)
```

3. Analyze the result outside of TRACE32.

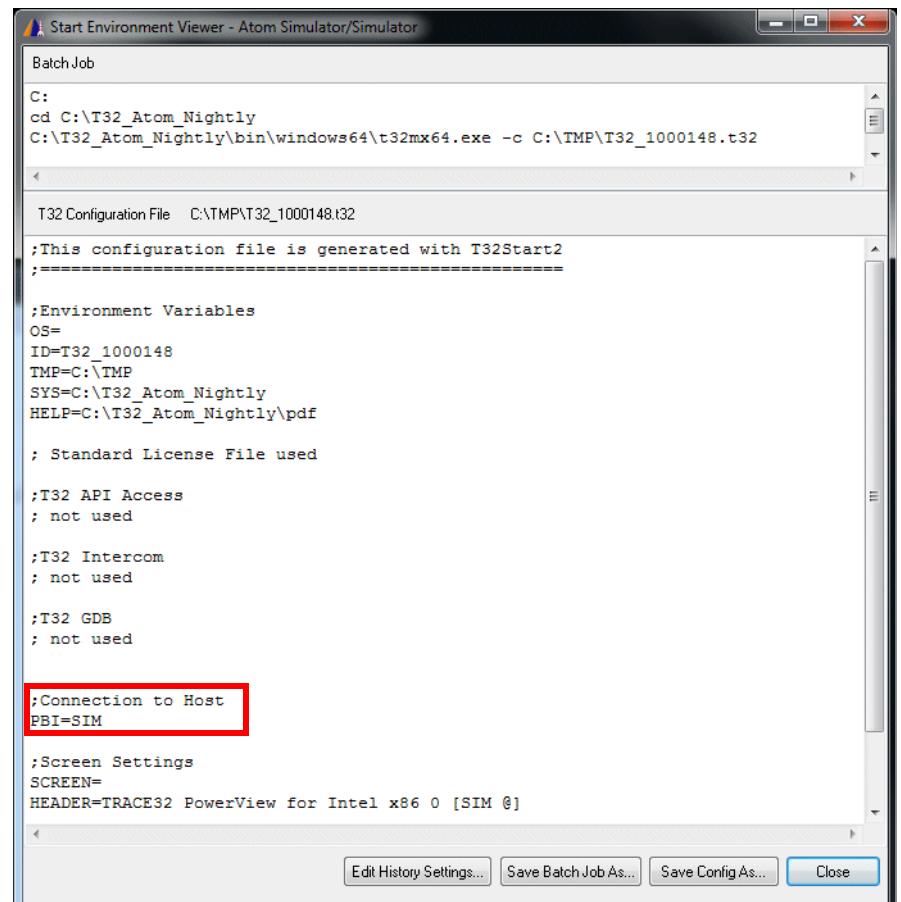
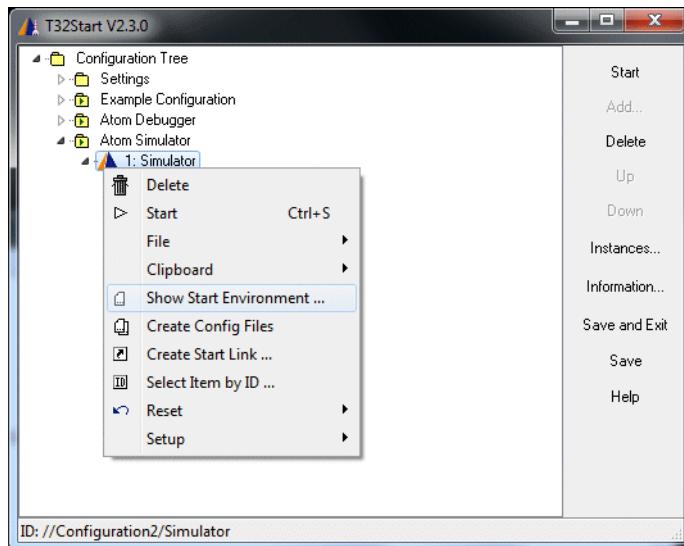
1. Save the contents of the trace memory into a file.



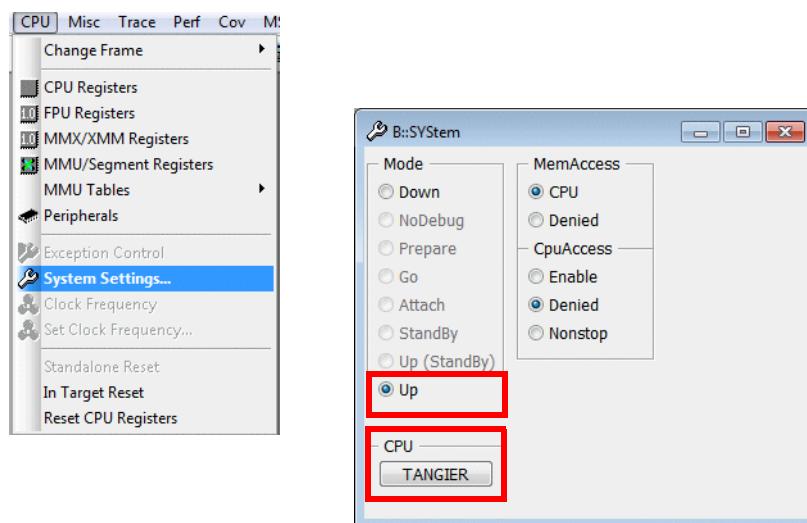
The default extension for the trace file is **.ad**.

```
Trace.SAVE testrun1
```

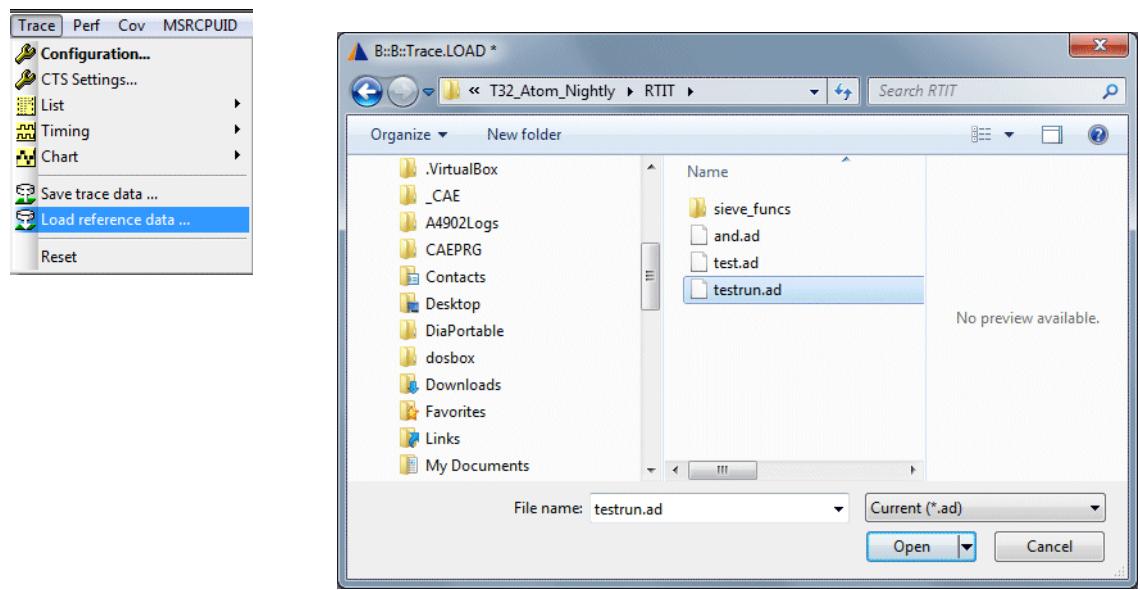
2. Start a TRACE32 Instruction Set Simulator (PBI=SIM).



3. Select your target CPU within the simulator. Then establish the communication between TRACE32 and the simulator.

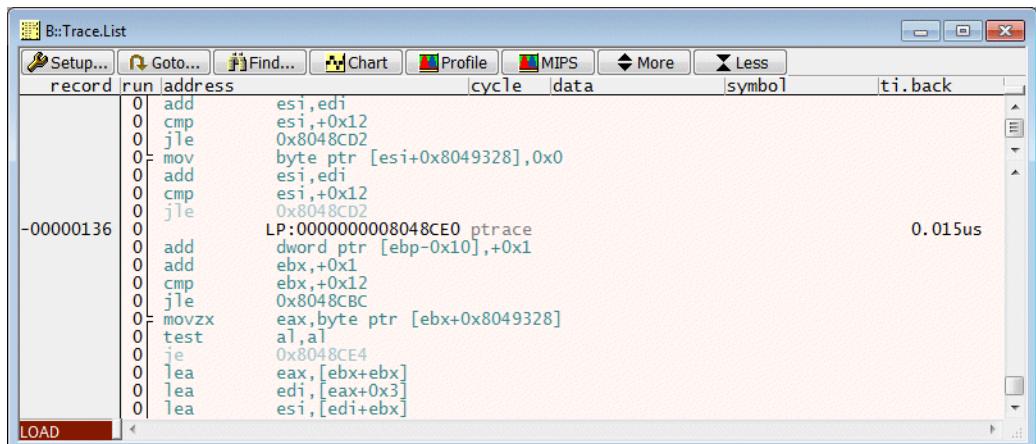


4. Load the trace file.



```
Trace.LOAD testrun
```

5. Display the trace contents.



record	run	address	cycle	data	symbol	ti.back
	0	add	esi,edi			
	0	cmp	esi,+0x12			
	0	jle	0x8048CD2			
	0	mov	byte ptr [esi+0x8049328],0x0			
	0	add	esi,edi			
	0	cmp	esi,+0x12			
	0	jle	0x8048CD2			
-000000136	0		LP:00000000008048CEO	ptrace		0.015us
	0	add	dword ptr [ebp-0x10],+0x1			
	0	add	ebx,+0x1			
	0	cmp	ebx,+0x12			
	0	jle	0x8048C8C			
	0	movzx	eax,byte ptr [ebx+0x8049328]			
	0	test	al,al			
	0	je	0x8048CE4			
	0	lea	eax,[ebx+ebx]			
	0	lea	edi,[eax+0x3]			
	0	lea	esi,[edi+ebx]			

LOAD indicates that the source for the trace information is the loaded file.

6. Load symbol and debug information if you need it.

```
Data.LOAD.Elf sieve_funcs_x86.elf /NoCODE
```

The TRACE32 Instruction Set Simulator provides the same trace display and analysis commands as the TRACE32 debugger.



Postprocessing of recorded trace information with the TRACE32 Instruction Set Simulator becomes more complex if an operating system that uses dynamic memory management to handle processes/task is used (e.g. Linux).

Script version

Save the trace contents in the recording TRACE32 instance:

```
Trace.SAVE testrun.ad
```

Prepare the TRACE32 Instruction Set Simulator for off-line processing of the trace information:

```
SYStem.CPU TANGIER
SYStem.Up
Trace.LOAD testrun.ad
Data.LOAD.Elf sieve_funcs_x86.elf /NoCODE
Trace.List
```

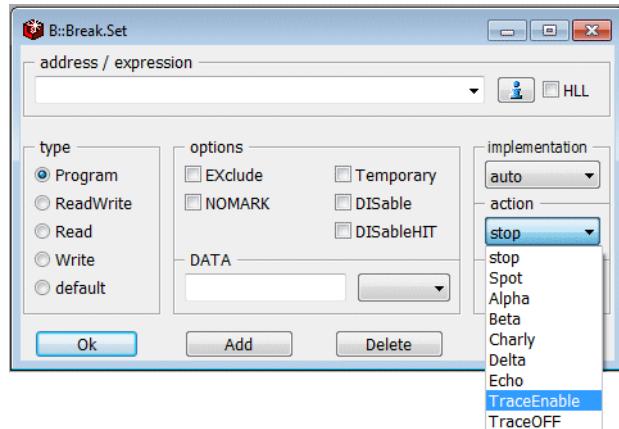
Trace.EXPORT.TracePort <file> Export trace raw data (no timestamps).

```
SystemTrace.EXPORT.TracePort mytest1.ad
```

Trace Control by Filters

Intel® PT provides 2 address ranges for trace control. The smallest range size is 4 bytes.

TRACE32 PowerView provides access to these address ranges by the **action** field in the **Break.Set** dialog.



The 2 address ranges can be used for the following purposes:

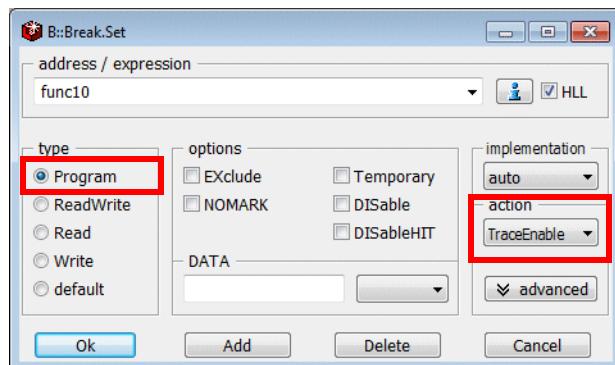
TraceEnable advises Intel® PT to generate program flow information for the specified address range only.

TraceOFF advises Intel® PT to stop the generation of program flow information as soon as a specified address range is reached.

Both filters are programmed to all Intel® PT in an SMP configuration.

Example 1: Advise Intel® PT to generate program flow information only for function func10.

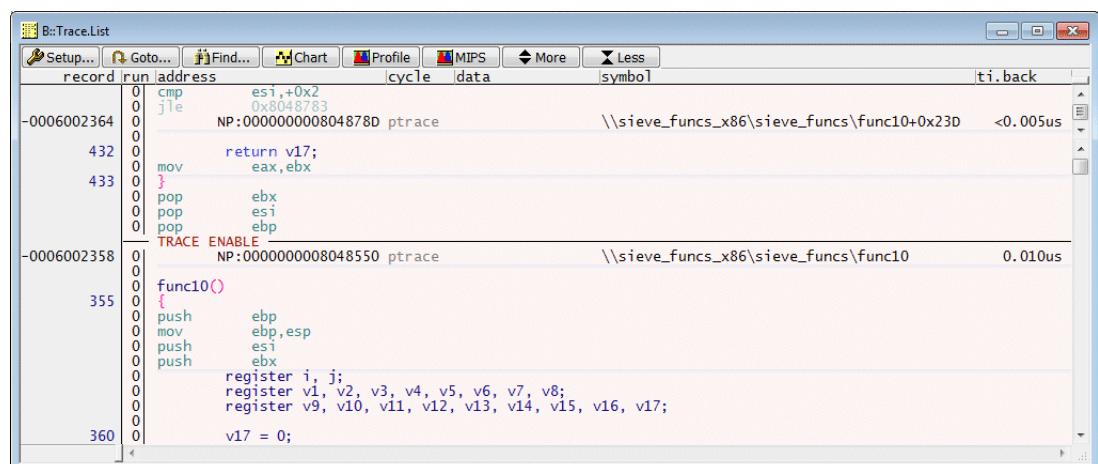
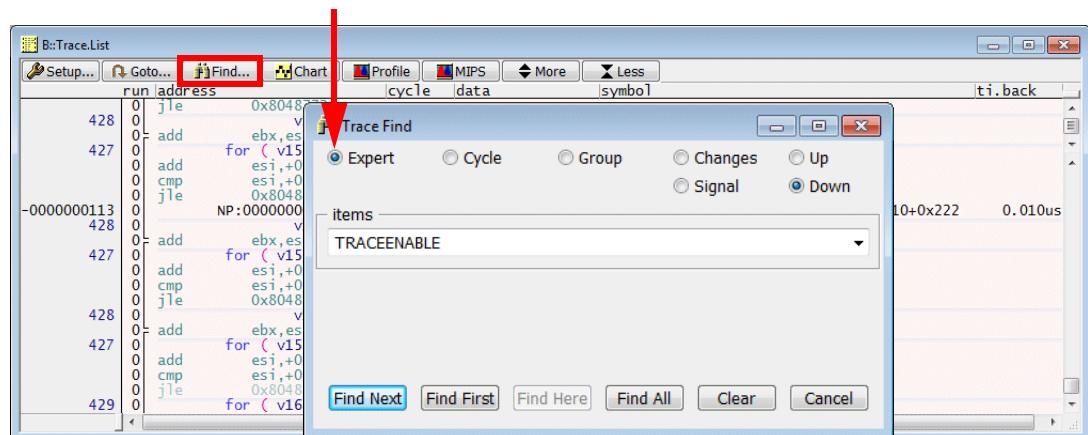
1. Set a Program breakpoint to the address range of func10 and select the action TraceEnable.



2. Start and stop the program execution.

3. Display the result.

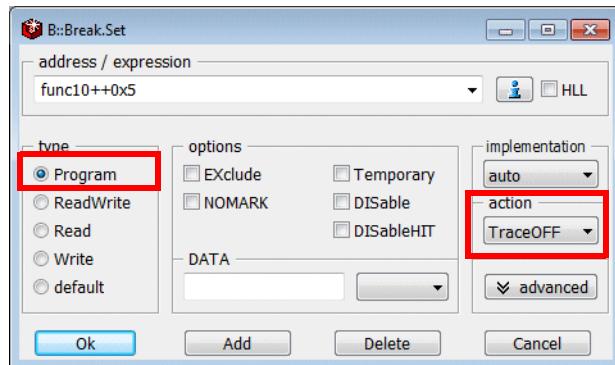
TRACE ENABLE indicates the start of the message generation. It might be necessary to search for it.



```
Break.Delete /ALL
Var.Break.Set func10 /Program /TraceEnable
Go
...
Break
Trace.List
```

Example 2: Advise Intel® PT to stop the generation of program flow information as soon as function func10 is entered.

1. Set a Program breakpoint to the start address of func10 plus 5 bytes and select the action TraceOFF.



2. Start the program execution.

TRACE32 has, unfortunately, no way to detect that Intel® PT stopped the generation of trace information.

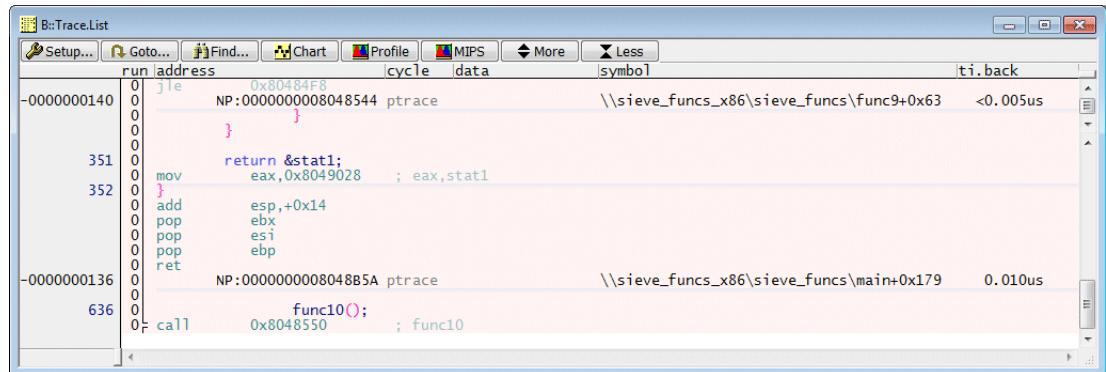
Off-chip trace: Since the Analyzer is recording STP packets, **used** could increase, because other trace sources continue generating STP packets.



Onchip trace: TRACE32 can not read the filling level of the onchip trace while recording.

3. Stop the program execution.

4. Display the result.



```
Break.Delete /ALL
```

```
Break.Set func10++0x5 /Program /TraceOFF
```

```
Go
```

```
...
```

```
Break
```

```
Trace.List
```

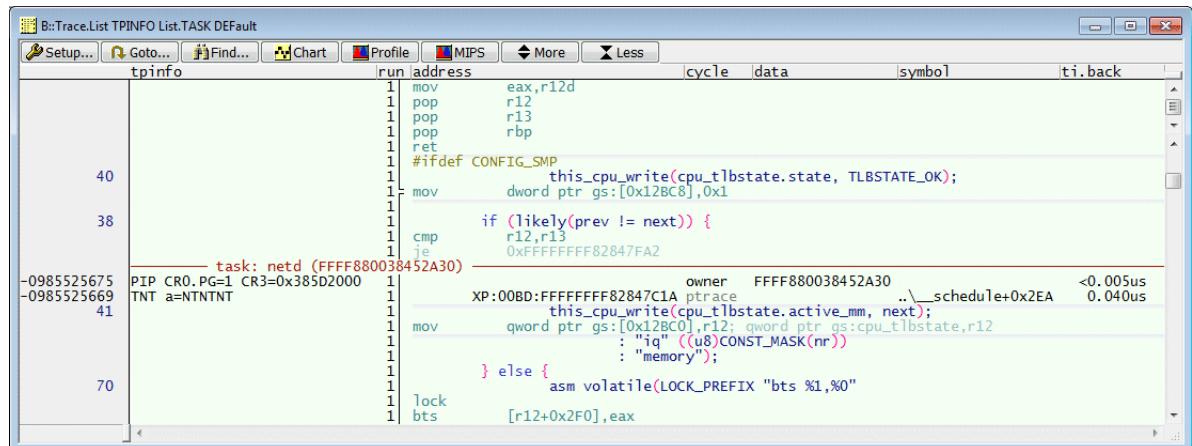
OS-Aware Tracing

OS-aware tracing requires that OS-aware debugging is configured. For more information refer to “[OS-aware Debugging](#)” (glossary.pdf).

Process Switch Packets

x86/x64 processors have a CR3 control register that contains the Process Context Identifier (PCID). On every context switch the corresponding PCID is loaded to CR3.

Intel® PT generates a Paging Information Packet (PIP) when a write to CR3 occurs.

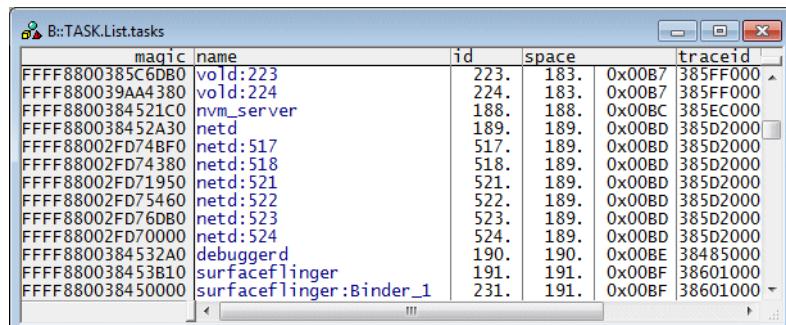


Intel PT Trace List showing a process switch. The assembly code shows a context switch (task switch) to netd (task: netd (FFFF880038452A30)). The trace list shows the write to CR3 and the generation of a Paging Information Packet (PIP) with the following details:

run	address	cycle	data	symbol	ti.back
40	mov eax,r12d pop r12 pop r13 pop rbp ret #ifdef CONFIG_SMP this_cpu_write(cpu_tlbstate.state, TLBSTATE_OK); mov dword ptr gs:[0x12BC8],0x1				
38	cmp r12,r13 je 0xFFFFFFFF82847FA2				
41	task: netd (FFFF880038452A30) PIP CRO.PG=1 CR3=0x385D2000 TNT a=NTNTNT 0985525675 0985525669 41 XP:00BD:FFFFFF82847C1A ptrace owner FFFF880038452A30 ..\schedule+0x2EA <0.005us this_cpu_write(cpu_tlbstate.active_mm, next); mov qword ptr gs:[0x12BC0],r12; qword ptr gs:cpu_tlbstate,r12 : "iq" ((u8)CONST_MASK(nr)) : "memory"; } else { asm volatile(LOCK_PREFIX "bts %1,%0" [r12+0x2F0],eax	0.040us			
70					

TRACE32 names the cycle type **owner** if the PCID loaded to CR3 can be assigned to a process.

The command **TASK.List.tasks** can be used to check all assignments currently known to TRACE32. The **traceid** represents the PCID in this display.



magic	name	id	space	traceid
FFFF8800385C6DB0	vold:223	223.	183.	0x0087 385FF000
FFFF880039AA4380	vold:224	224.	183.	0x0087 385FF000
FFFF8800384521C0	nvm_server	188.	188.	0x008C 385EC000
FFFF880038452A30	netd	189.	189.	0x008D 385D2000
FFFF88002FD74BF0	netd:517	517.	189.	0x008D 385D2000
FFFF88002FD74380	netd:518	518.	189.	0x008D 385D2000
FFFF88002FD71950	netd:521	521.	189.	0x008D 385D2000
FFFF88002FD75460	netd:522	522.	189.	0x008D 385D2000
FFFF88002FD76DB0	netd:523	523.	189.	0x008D 385D2000
FFFF88002FD70000	netd:524	524.	189.	0x008D 385D2000
FFFF8800384532A0	debuggerd	190.	190.	0x008E 38485000
FFFF880038453B10	surfaceflinger	191.	191.	0x008F 38601000
FFFF880038450000	surfaceflinger:Binder_1	231.	191.	0x00BF 38601000

tpinfo		run	address	cycle	data	symbol	ti.back
38		1	pop r13				
		1	pop rbp				
		1	ret				
		1	if (likely(prev != next)) {				
		1	rcx,qword ptr [rbp-0x40]				
		1	rbx,r14				
		1	0xFFFFFFFF82174C19				
-0986647737	PIP CRO.PG=1 CR3=0xC93000			XP:FFFF:FFFFFF82174F3	context 00000000CD93000		<0.005us
-0986647730	TNT a=NNNNNT			ptrace	..\\flush_old_exec+0x303		0.040us
40		1	#ifdef CONFIG_SMP				
41		1	this_cpu_write(cpu_tlbstate.state, TLBSTATE_OK);				
		1	dword ptr gs:[0x128C8],0x1				
		1	this_cpu_write(cpu_tlbstate.active_mm, next);				
		1	mov qword ptr gs:[0x0],rbx				
		1	: "iq" ((u8)CONST_MASK(nr))				
		1	: "memory");				
		1	} else {				

TRACE32 names the cycle type **context** if the PCID loaded to CR3 can not be assigned to a process.

The fact that the PCID can not be assigned to a process results in the following,::

- Since TRACE32 does not require the PCID to decode trace information for the common address range, full trace decoding is possible.

```
; command in the setup for the OS Awareness
TRANSLATION.COMMON 0xffff880000000000--0xfffffffffffffff
```

- For all other address ranges a decoding of the trace information is not possible. The cycle type **unknown** is used for trace information that can not be decoded.

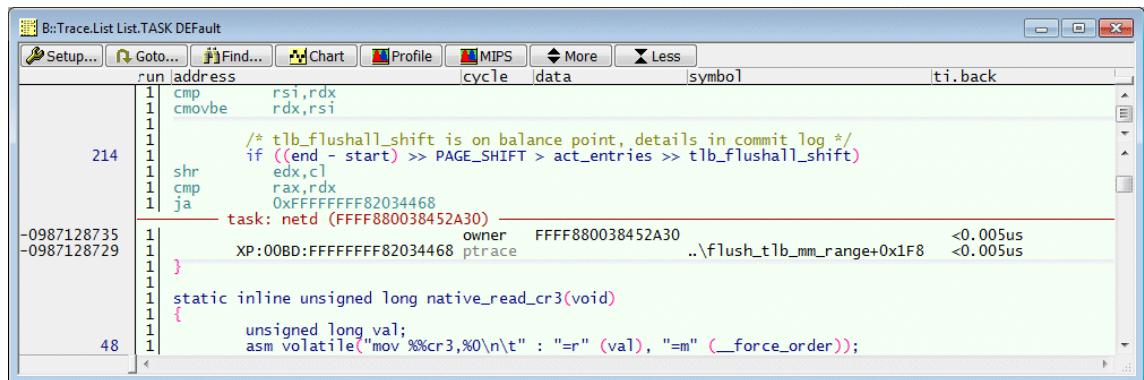
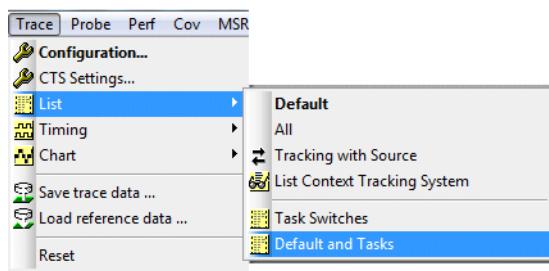
B:Trace.List.TASK DEFault		run	address	cycle	data	symbol	ti.back
-1016945789	1		XP:FFFF:0000000F770C9F2	unknown			<0.005us
-1016945788	1		XP:FFFF:0000000F770C9F2	unknown			<0.005us
-1016945786	1		XP:FFFF:0000000F770C9F2	unknown			<0.005us
-1016945781	1		XP:FFFF:0000000F76E7F00	unknown			0.040us
-1016945780	1		XP:FFFF:0000000F76E7F00	unknown			<0.005us
-1016945777	1		XP:FFFF:0000000F76E81C2	unknown			<0.005us
-1016945776	1		XP:FFFF:0000000F76E81C2	unknown			0.040us
-1016945775	1		XP:FFFF:0000000F76E81C2	unknown			<0.005us

NOTE:

The Real-Time Instruction Trace (RTIT), doesn't feature the process switching packets. If multiple user space applications are traced, it is only possible to decode the trace packets of the kernel. The cycle type **unknown** is used for the user space trace packets. For decoding the trace packets of a user application, it is necessary to filter the process of interest using the CR3 filter.

RTIT was implemented on very few devices, then it was extended to the Intel Processor Trace which supports the process switching trace. The RTIT trace is also covered by TRACE32 using the IPT command group.

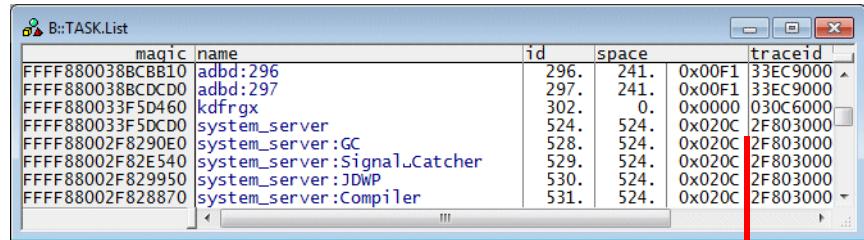
Program Flow and Process Switches



```
Trace.List List.TASK DEFAULT ; display trace listing with
; decoded task switch information
```

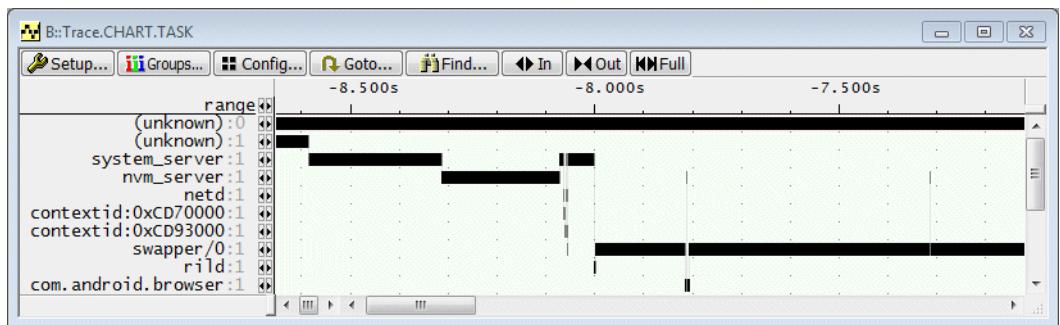
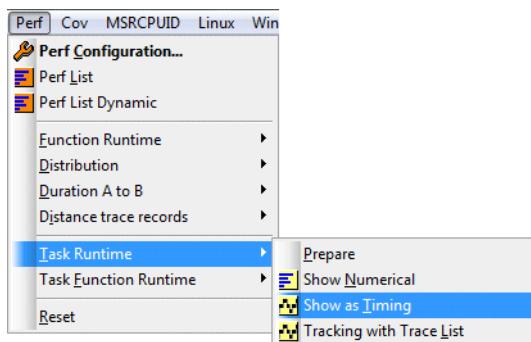
NOTE:

This is a process switch analysis, since Paging Information Packets (PIP) only indicate process switches, but no thread switches.



magic	name	id	space	traceid
FFFFF880038BCBB10	adbdb:296	296.	241.	0x00F1 33EC9000
FFFFF880038BCDCD0	adbdb:297	297.	241.	0x00F1 33EC9000
FFFFF880033F5D460	kdfrgx	302.	0.	0x0000 030C6000
FFFFF880033F5DCD0	system_server	524.	524.	0x020C 2F803000
FFFFF88002F8290E0	system_server:GC	528.	524.	0x020C 2F803000
FFFFF88002F82E540	system_server:Signal_Catcher	529.	524.	0x020C 2F803000
FFFFF88002F829950	system_server:JDWP	530.	524.	0x020C 2F803000
FFFFF88002F828870	system_server:Compiler	531.	524.	0x020C 2F803000

Threads do not have their own traceid



contextid:<trace_id> indicates process switches for which the <trace_id> can not be assigned to a process.

Trace.Chart.TASK [/SplitCORE]

Display process time chart

- graphical display
- split the results per core
- sort the results per recording order

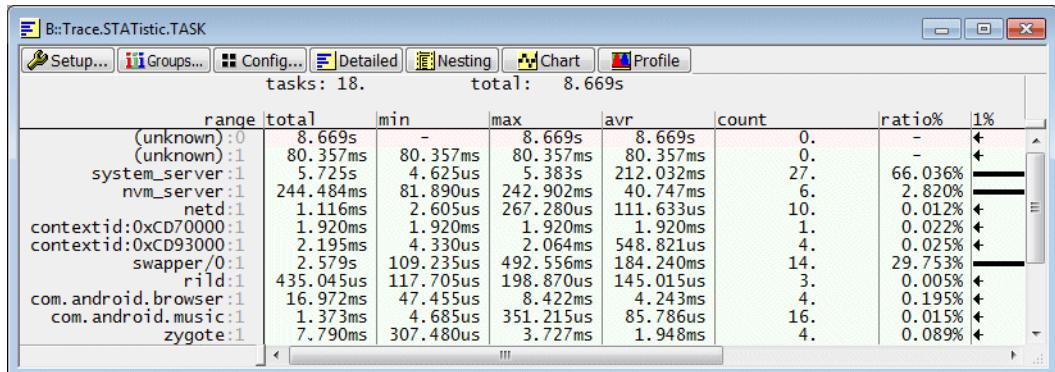
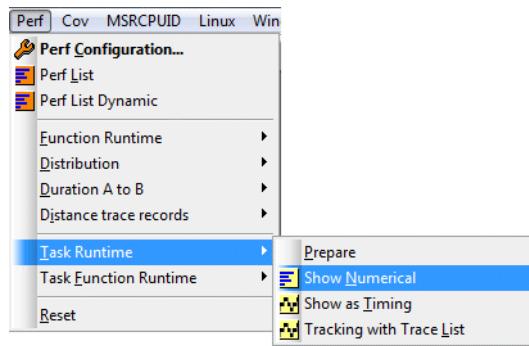
Trace.Chart.TASK /MergeCORE

Display process time chart

- graphical display
- merge the results of all cores

Trace information is analyzed independently for each core.
The time chart summarizes these results to a single result.

The recording time before the first Paging Information Packet (PIP) is assigned to the **(unknown)** task.



Trace.STATistic.TASK [/SplitCORE]

- Process runtime statistic
- numerical display
- split the results per core
- sort the results per recording order

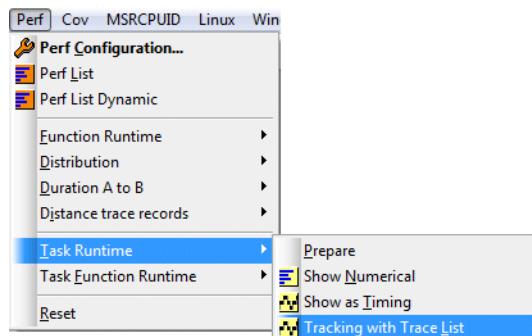
Trace.STATistic.TASK /MergeCORE

- Process runtime statistic
- numerical display
- merge the results of all cores

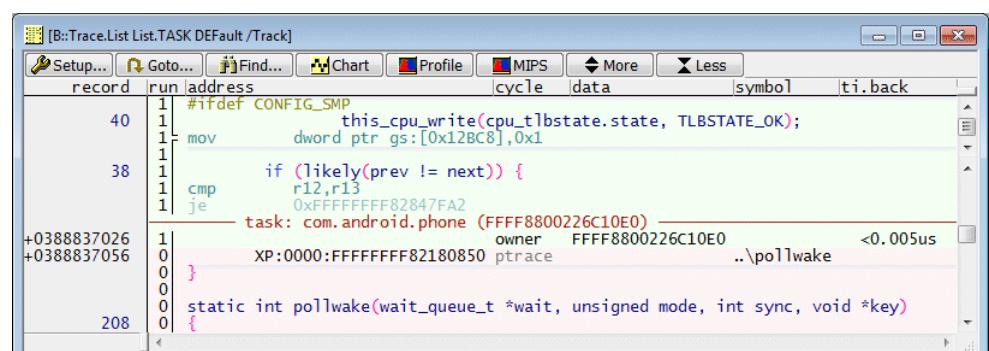
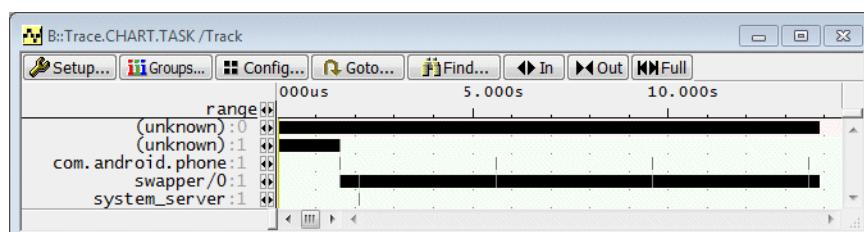
Trace information is analyzed independently for each core. The statistic summarizes these results to a single result.

Find Process Switches in the Trace

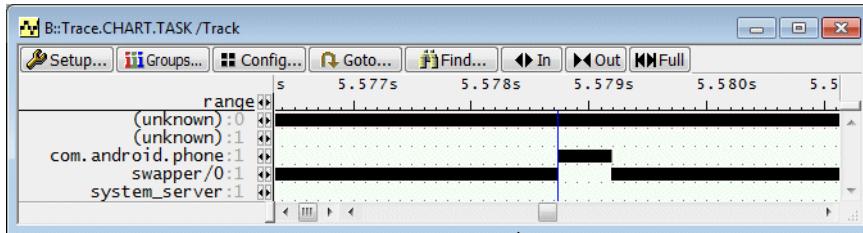
1. Open a process time chart window and a trace listing with decoded process switch information. Link both windows by using the /Track option.



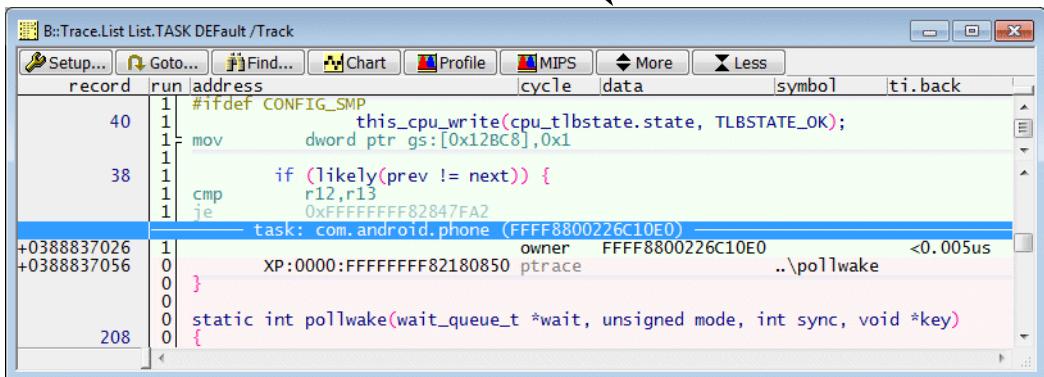
```
Trace.Chart.TASK /Track ; open process time chart  
; window  
  
Trace.List List.TASK DEFault /Track ; open a default trace  
; listing that includes  
; process information  
  
; both windows use the /Track option  
; a window opened with the /Track option follows the cursor movement  
; of the active window  
  
; tracking between trace windows is based on the timestamp  
; information
```



2. Use the arrow keys  of the process of interest to move to next state change.



The trace listing follows the cursor movement in the Trace.CHART.TASK window



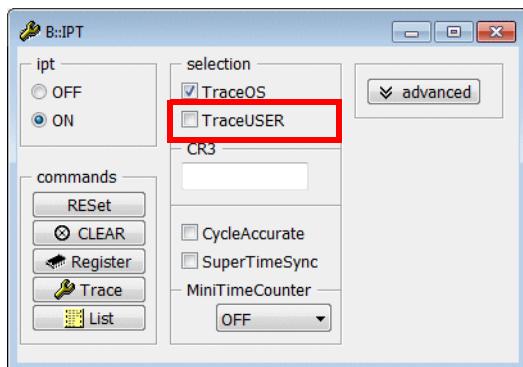
Filtering by Privilege Level

Intel® PT can be advised to generate program flow information only for:

- privilege level 0
- all privilege levels greater than 0

Example: Advise Intel® PT to generate only program flow information for privilege level 0.

1. Uncheck TraceUSER in the IPT configuration window.



2. Start and stop the program execution.

3. Display the result.

```
IPT.state
IPT.TraceUSER OFF
Go
...
Trace.List
```

Filtering by Process

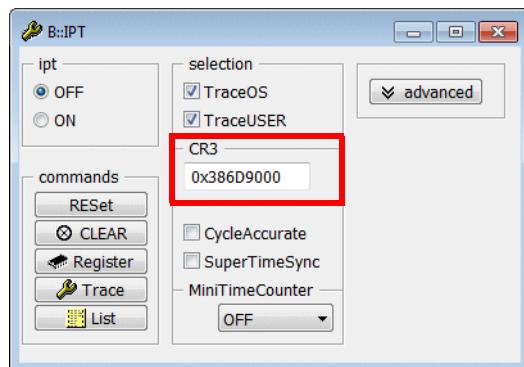
Intel® PT can be advised to generate program flow information only for a process of interest.

Example: Advise Intel® PT to generate only program flow information for the process “logcat”.

1. Program the CR3 filter via the IPT window.

```
IPT.state
```

; open IPT configuration
; window



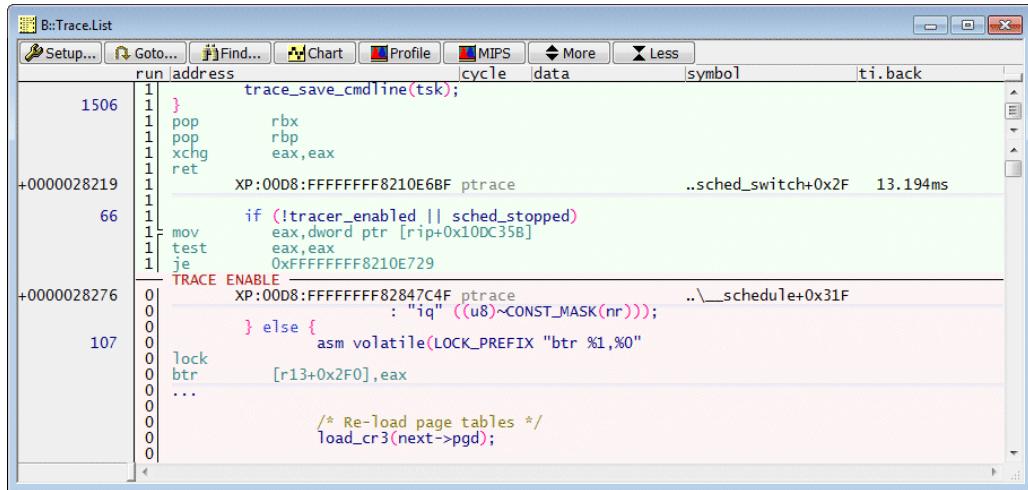
```
; specify the <trace_id> of the process "logcat"  
IPT.CR3 0x386D9000  
  
; IPT.CR3 TASK.PROC.NAME2TRACEID("logcat")
```

TASK.PROC.NAME2TRACEID(<process_name>)

Returns the *<trace_id>* of specified process.

2. Start and stop the program execution.

3. Display the result.



The screenshot shows the B:Trace.List window with the following assembly code and trace data:

```
1506    trace_save_cmdLine(tsk);
1      }
1      pop    rbx
1      pop    rbp
1      xchg   eax, eax
1      ret
+00000028219  XP:0008:FFFFFFFFFF8210E6BF ptrace          .sched_switch+0x2F  13.194ms
66      if (!tracer_enabled || sched_stopped)
1      mov    eax,dword ptr [rip+0x10DC358]
1      test   eax, eax
1      je     0x00000028276
+00000028276  TRACE ENABLE
0      XP:0008:FFFFFFFFFF82847C4F ptrace          ..\_\schedule+0x31F
0      : "iq"  ((u8)^CONST_MASK(nr));
0      } else {
0      asm volatile(LOCK_PREFIX "btr %1,%0"
0      lock
0      btr   [r13+0x2F0],eax
0      ...
0      /* Re-load page tables */
0      load_cr3(next->pgd);
0
```

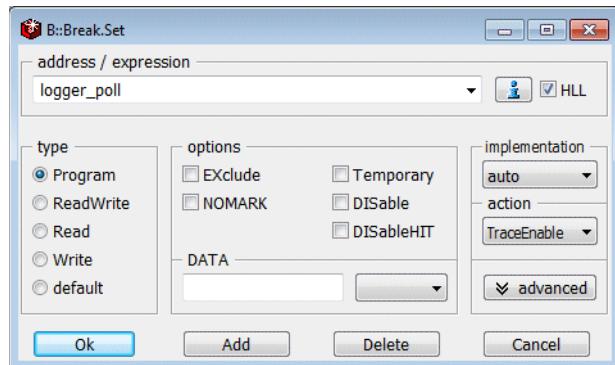
TRACE ENABLE indicates the re-start of the program flow trace generation.

Please be aware that TRACE32 decodes all trace information for the process specified in the command **IPT.CR3 <trace_id>**. Intel® PT does not generate Paging Information Packet (PIP) in this scenario.

Filter on Function executed by Process

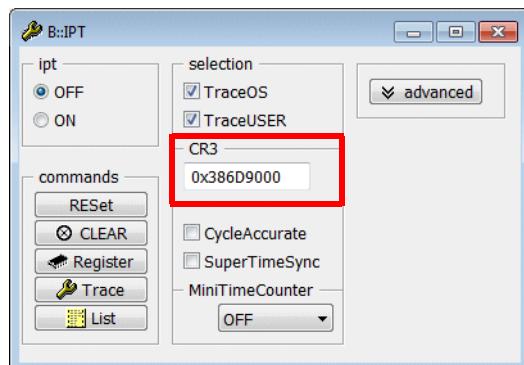
Example: Advise Intel® PT to generate only program flow information when the function “logger_poll” is running in the context of the process “logcat”.

1. Set a Program breakpoint to the address range of the function logger_poll and select the action TraceEnable.



2. Program the CR3 filter via the IPT window.

```
IPT.state ; open IPT configuration  
; window
```



```
IPT.CR3 TASK.PROC.NAME2TRACEID("logcat")
```

3. Start and stop the program execution.

4. Display the result.

B::Trace.List List.TASK DEFAULT

	record	run	address	cycle	data	symbol	ti.back
	662		1 if (log->w_off != reader->r_off) 1 ret = POLLIN POLLRDNORM; 1 mutex_unlock(&log->mutex); 1 0xFFFFFFFF828464D0; mutex_unlock				
+00000738672			1 TRACE_ENABLE	XP:0102:FFFFFFFFFF8262CA67	ptrace	\\vmlinux\\logger\\logger_poll+0x87	<0.005us
	665		1 } 1 return ret; 1 }				
			1 mov eax,ebx 1 pop rbx 1 pop r12 1 pop r13 1 pop rbp 1 ret				
+00000738686			1 TRACE_ENABLE	XP:0102:FFFFFFFFFF8262C9E0	ptrace	\\vmlinux\\logger\\logger_poll	0.080us

TRACE ENABLE indicates the re-start of the program flow trace generation.

Belated Analysis

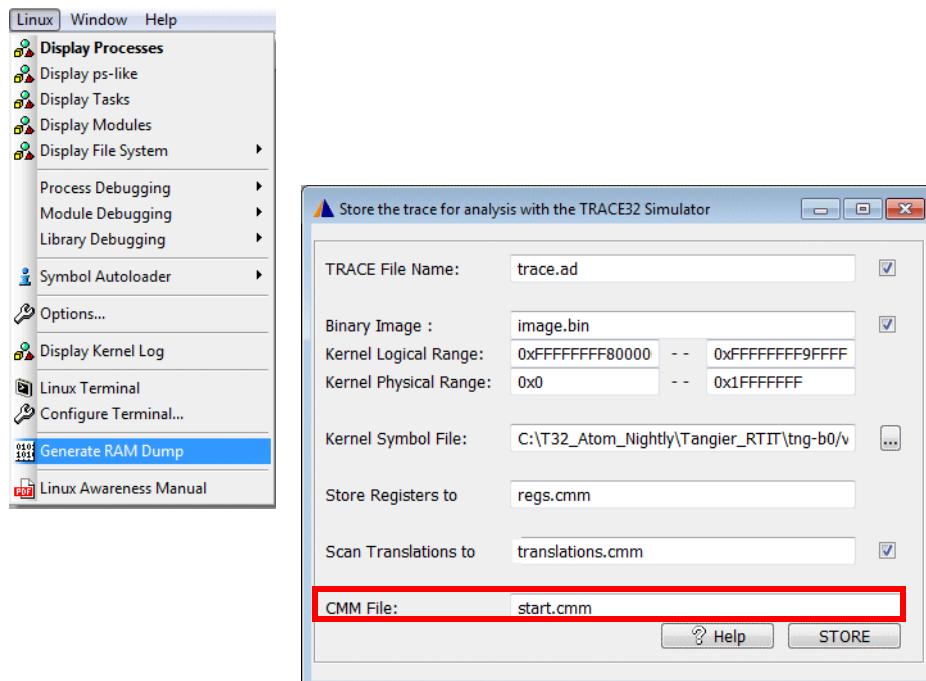
Postprocessing of recorded trace information with the TRACE32 Instruction Set Simulator requires complex preparations if an operating system that uses dynamic memory management to handle processes is used (e.g. Linux).

The following information has to be stored after recording and re-loaded to the TRACE32 Instruction Set Simulator:

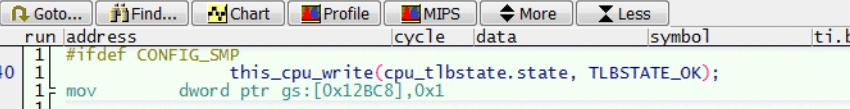
- The recorded trace information
- The whole kernel address space (code and data)
- The core registers
- All MMU-related registers
- The settings of the Debugger Address Translation (TRACE32 command group: [TRANSlation](#))

Example for Linux

The **Generate RAM Dump** command in the **Linux** menu provides a store framework. It generates a **CMM file** that summarizes all commands for the TRACE32 Instruction Set Simulator.



If you start a TRACE32 Instruction Set Simulator and run the generated script, the recorded trace information can be analyzed there. Please be aware that additional settings might be necessary e.g. the specification of the search paths for the C/C++ sources.



The screenshot shows the assembly code for task switching in a debugger. The code is annotated with comments and assembly instructions. The assembly code is as follows:

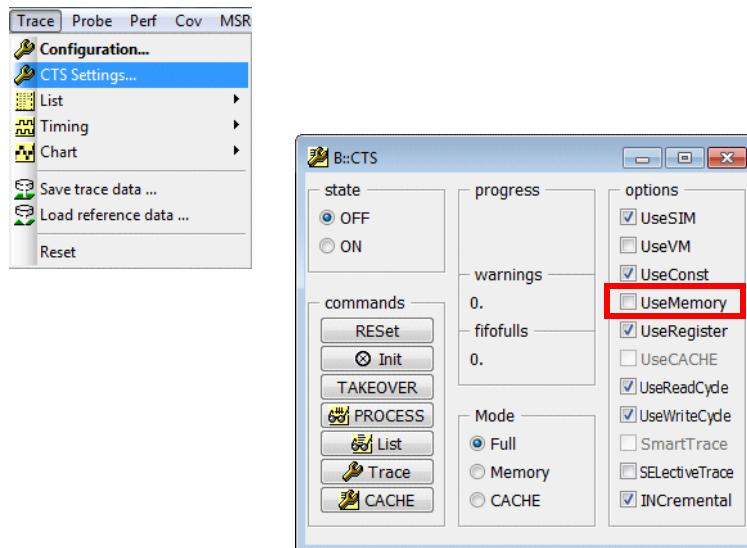
```
1 #ifndef CONFIG_SMP
1     this_cpu_write(cpu_tlbstate.state, TLBSTATE_OK);
1     mov    dword ptr gs:[0x12BC8],0x1
1
1     if (likely(prev != next)) {
1         cmp    r12,r13
1         je    0xFFFFFFFF82847FA2
1
1         task: r1d (FFFF880012382A30) -
1             owner    FFFF880012382A30
1             <0.005us
+0939133235
+0939133246
1             XP:0000:FFFFFFFFFFA0086CAB ptrace
0             rdi,rbx
0             xor    ecx,ecx
0             mov    edx,0x1
0             mov    esi,0x3
0             call   0xFFFFFFFF8209E200; __wake_up
0
0     ...
0     * @q: the waitqueue
0     * @mode: which threads
```

Trace-based Debugging (CTS)

Trace-based debugging allows to re-run the recorded program section within TRACE32 PowerView.

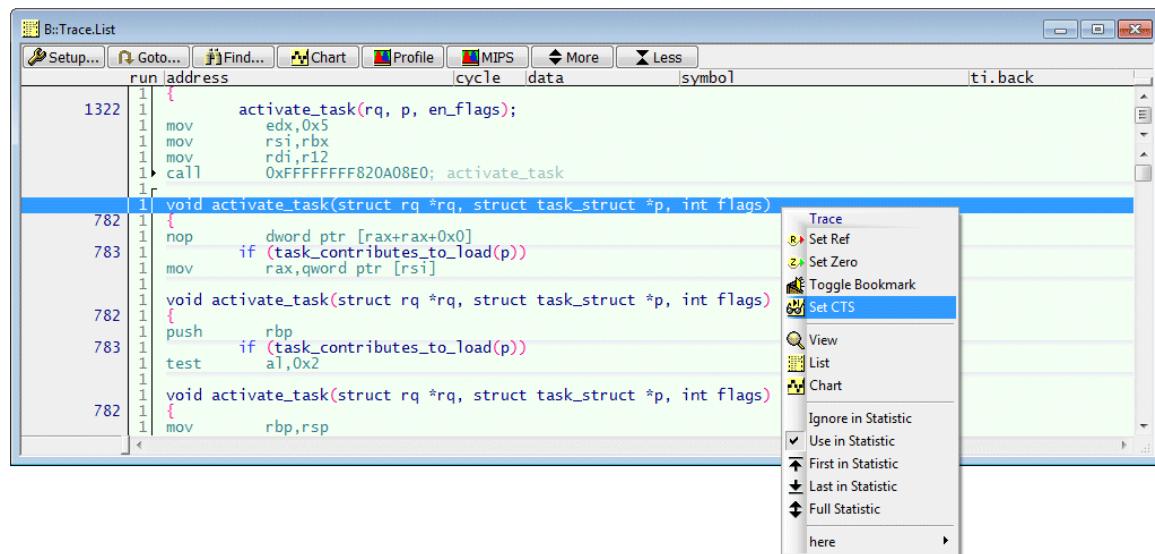
Setup

Since Intel® PT does not provide any information on read/write accesses, **UseMemory** has to be unchecked. A full explanation on this is given later in the chapter “[CTS Technique](#)”, page 93.



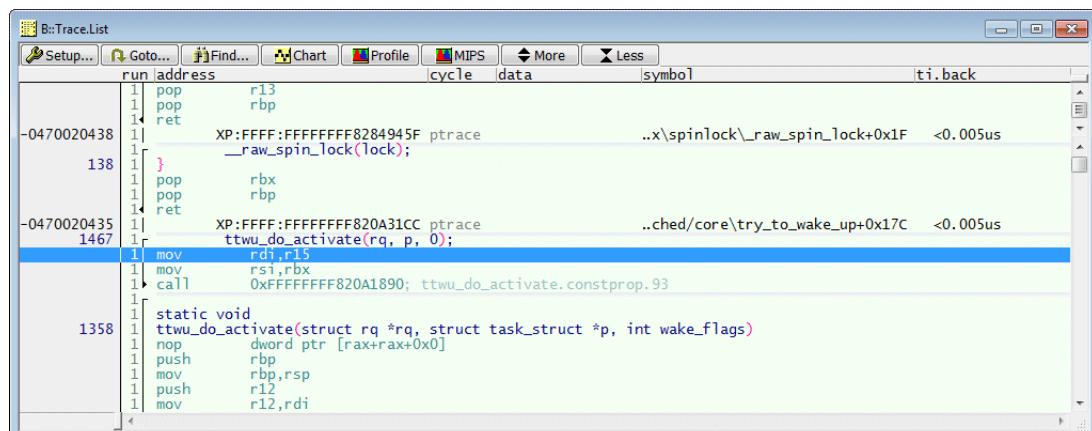
CTS.UseFinalMemory OFF

Specify the starting point for the trace re-run by selecting **Set CTS** from the Trace pull-down menu. The starting point in the example below is the entry to the function **activate_task** executed by core 1.



Selecting **Set CTS** has the following effect:

- TRACE32 PowerView will use the preceding trace packet as starting point for the trace re-run.



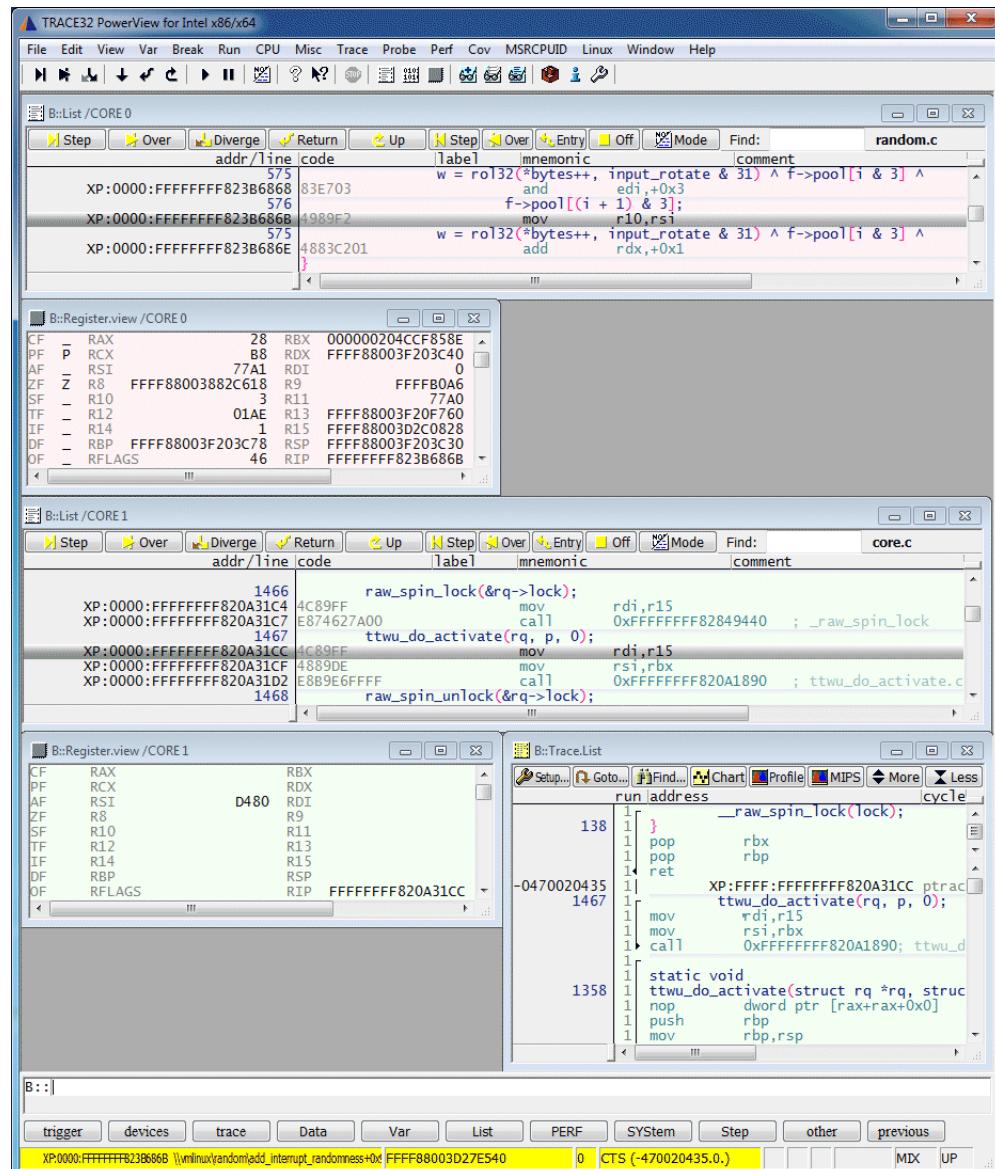
- The TRACE32 PowerView GUI does no longer show the current state of the target system, but it shows the target state as it was, when the starting point instruction was executed. This display mode is called CTS View.

CTS View means:

- The instruction pointers of all cores are set to the values they had when the starting point instruction was executed.
- The content of the core registers of all cores is reconstructed (as far as possible) to the values they had when the starting point instruction was executed. If TRACE32 can not reconstruct the content of a register it is displayed as empty.

TRACE32 PowerView uses a yellow look-and-feel to indicate CTS View.

The **Off** button in the source listing can be used to switch off the CTS View.





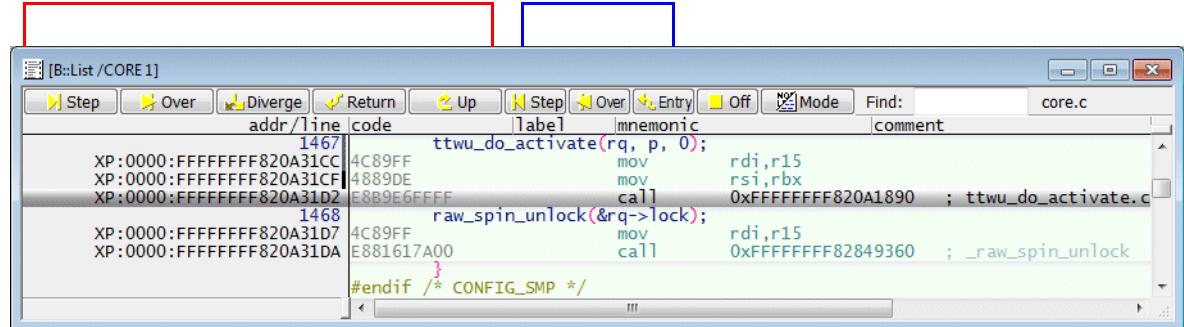
TRACE32 PowerView displays the state of the target as it was when the instruction of the trace record -470020435.0 was executed

Forward and Backward Debugging

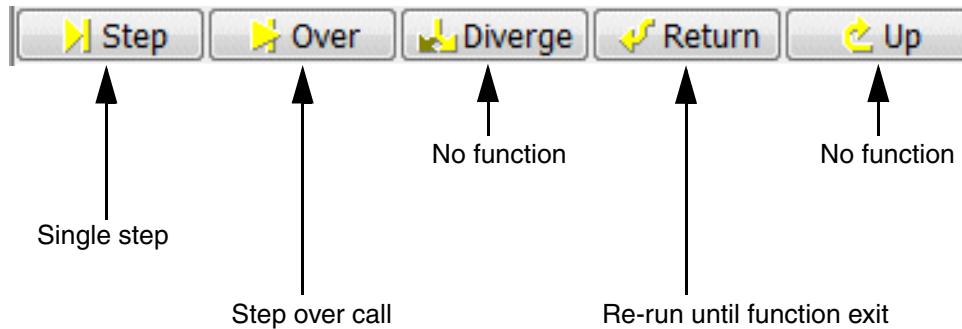
Now you can start to re-run the recorded program section within TRACE32 PowerView by forward or backward debugging.

Forward debugging commands

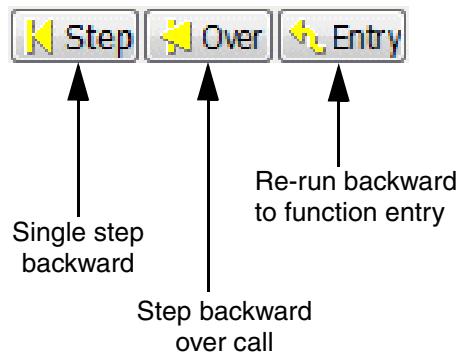
Backward debugging commands

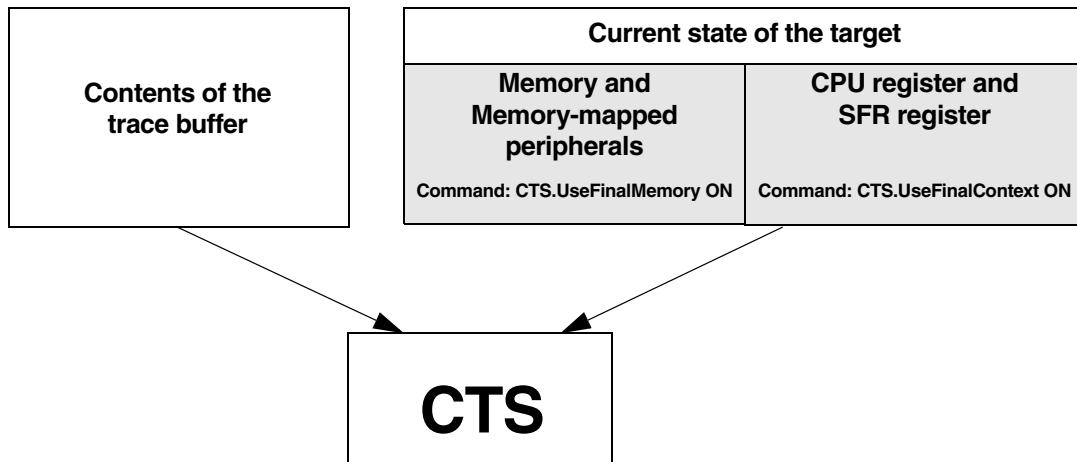


Forward Debugging



Backward Debugging





CTS.UseFinalMemory ON Default setting within TRACE32

If **CTS.UseFinalMemory** is ON and TRACE32 detects that a memory address was not changed by the recorded program section, TRACE32 PowerView displays the current content of this memory in CTS display mode.

Since Intel® PT does not provide any information on read/write accesses and since most read/write accesses are done by using an indirect address, TRACE32 can not detect which memory content was changed. This is the reason why **CTS.UseFinalMemory** has to be set to OFF.

If **CTS.UseFinalMemory** is switch OFF, but your memory contains constants, you can configure TRACE32 to use these constants by the following commands:

MAP.CONST <address_range>

CTS.MapConst ON

CTS.UseFinalContext ON Default setting within TRACE32

If **CTS.UseFinalContext** is ON and TRACE32 detects that a register was not changed by the recorded program section, TRACE32 PowerView displays the current content of this register in CTS display mode.

CTS.UseFinalContext has to be set to OFF, if you are using **Stack** mode for tracing.

Software under Analysis (no OS, OS or OS+MMU)

For the use of the function run-time analysis it is helpful to differentiate between three types of application software:

1. Software without operating system (abbreviation: **no OS**)
2. Software that includes an operating system (abbreviation: **OS**)
3. Software with an operating system that uses dynamic memory management to handle processes/tasks (**OS+MMU**).

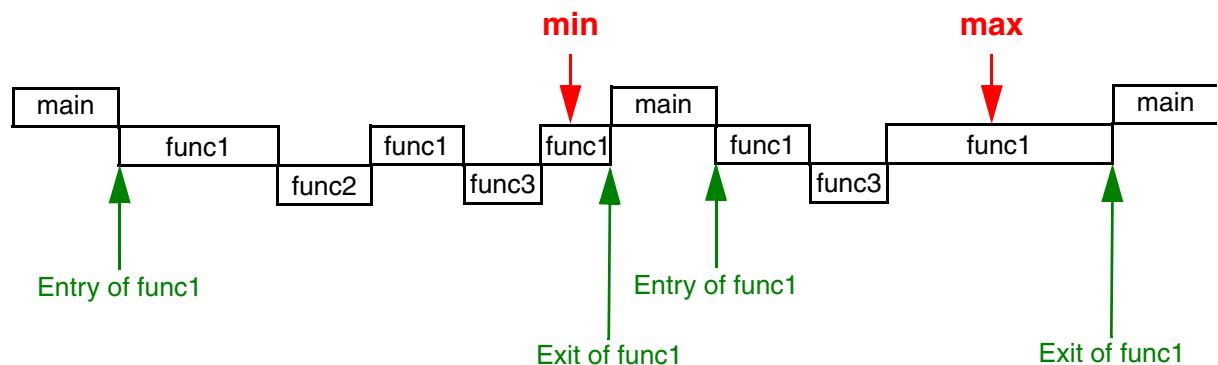
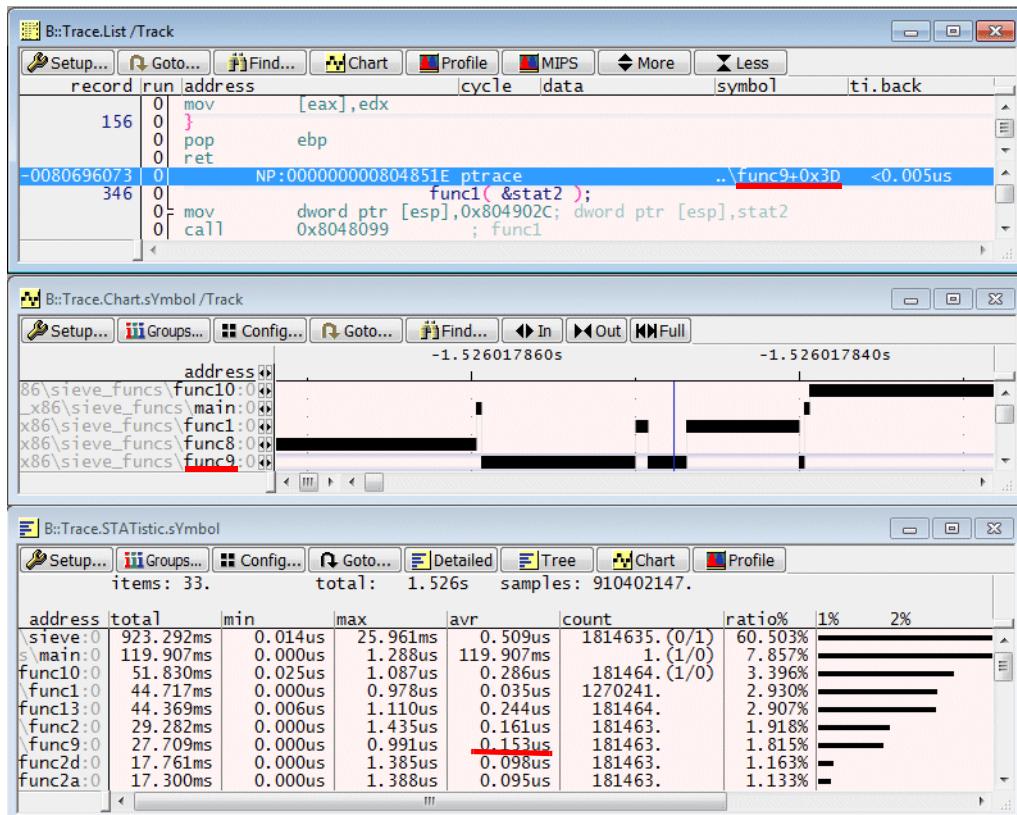
Flat vs. Nesting Analysis

TRACE32 provides two methods to analyze function run-times:

- Flat analysis
- Nesting analysis

Basic Knowledge about Flat Analysis

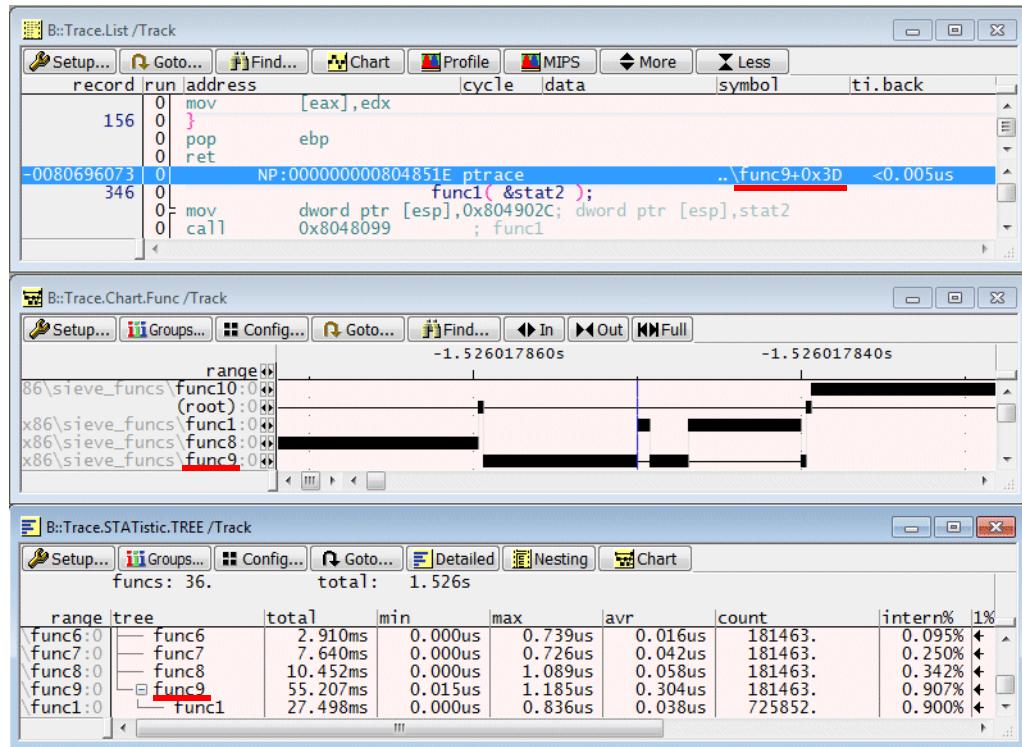
The flat function run-time analysis bases on the symbolic instruction addresses of the trace entries. The time spent by an instruction is assigned to the corresponding function/symbol region.

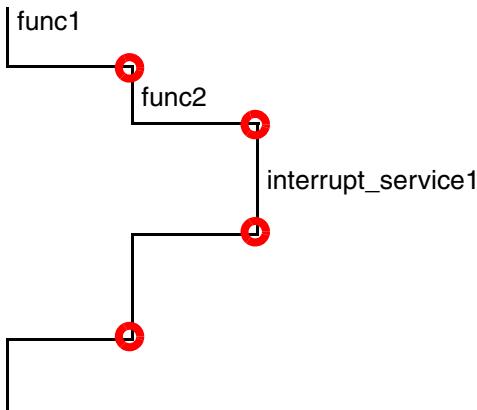


min	shortest time continuously in the address range of the function/symbol region
max	longest time continuously in the address range of the function/symbol region

Basic Knowledge about Nesting Analysis

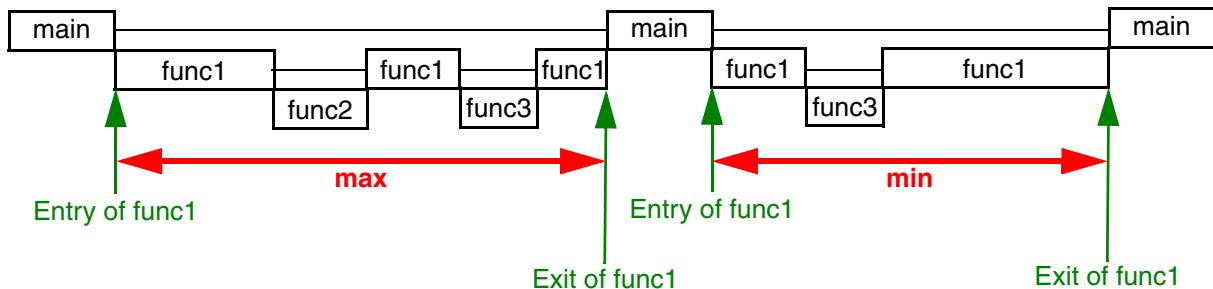
The function nesting analysis analyses only high-level language functions.





In order to display a nesting function run-time analysis TRACE32 analyzes the structure of the program execution by processing the trace information. The focus is put on the transition between functions (see picture above). The following events are of interest:

1. **Function entries**
2. **Function exits**
3. **Entries to interrupt service routines**
4. **Exits of interrupt service routines**
5. **Entries to TRAP handlers**
6. **Exits of TRAP handlers**



min	shortest time within the function including all subfunctions and traps
max	longest time within the function including all subfunctions and traps

The nesting analysis provides more details on the structure and the timing of the program run, but it is much more sensitive than the flat analysis. Missing or tricky function entries/exits may require additional setups before nesting analysis can be used.

Flat Function-Runtime Analysis

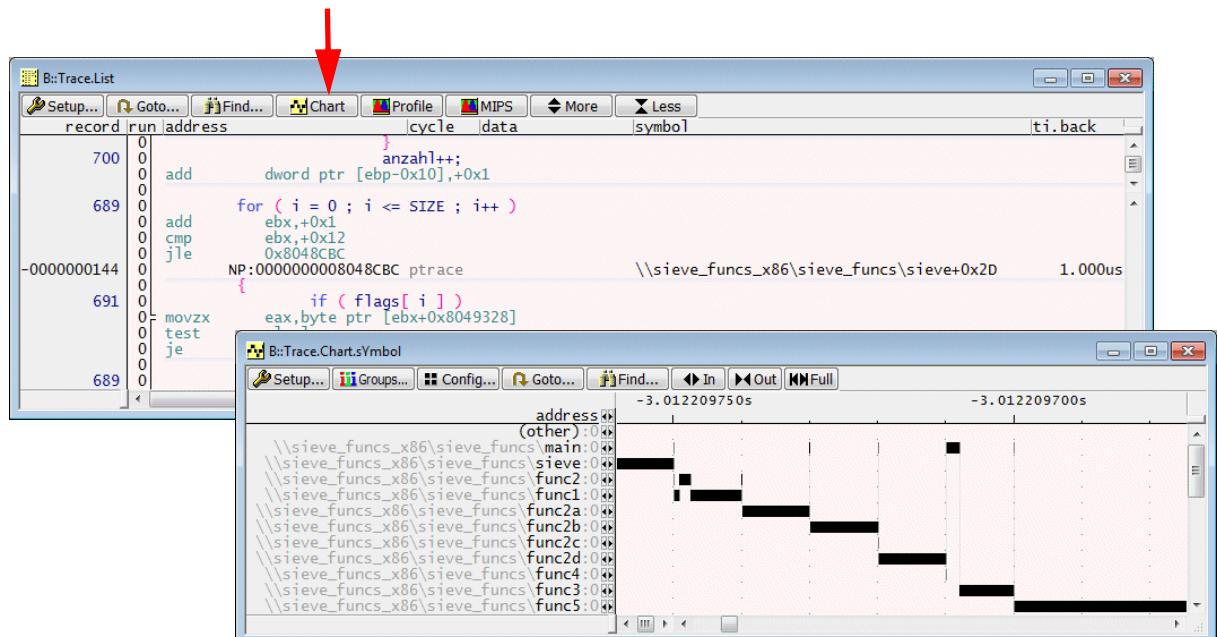
NOTE:

As long a TRACE32 does not support Synchronisation Time, cycle accurate tracing should be disabled for all kind of runtime measurement.

Function Time Chart

Default Time Chart

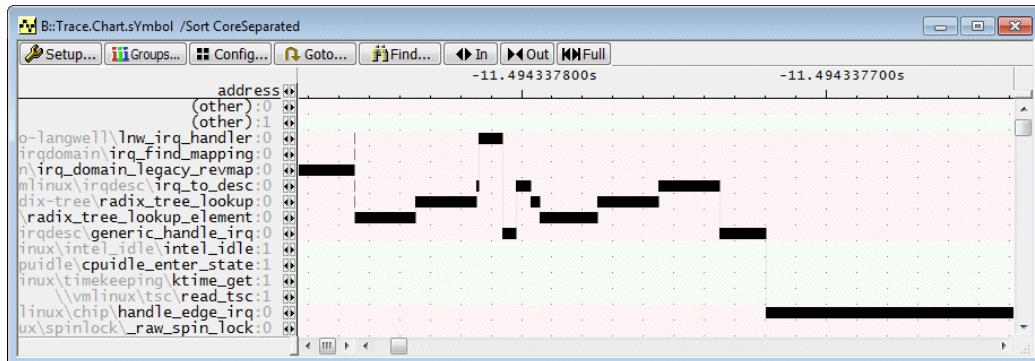
Pushing the **Chart** button in the **Trace.List** window
opens a **Trace.Chart.sYmbol** window



Trace.Chart.sYmbol [/SplitCore /Sort CoreTogether]

Flat function run-time analysis
- graphical display
- split the result per core
- sort results per core and then per recording order

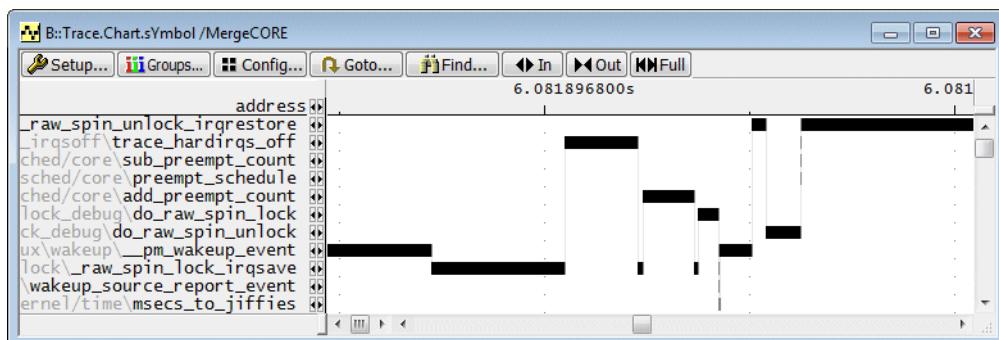
Core Options



Trace.Chart.sYmbol [/SplitCORE] /Sort CoreSeparated

Flat function run-time analysis

- graphical display
- split the result per core
- sort the results per recording order



Trace.Chart.sYmbol /MergeCORE

Flat function run-time analysis

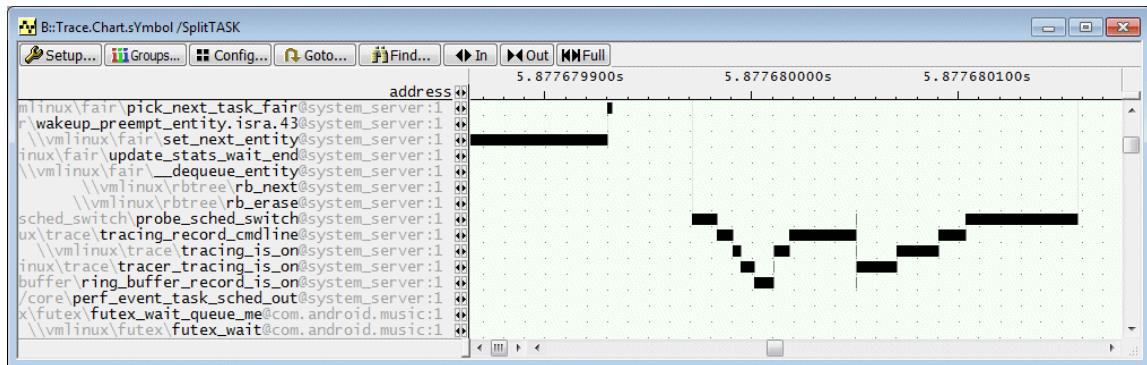
- graphical display
- merge the results of all cores

Trace information is analyzed independently for each core. The time chart summarizes these results to a single result.

TASK Options

Trace.Chart.sYmbol /SplitTASK

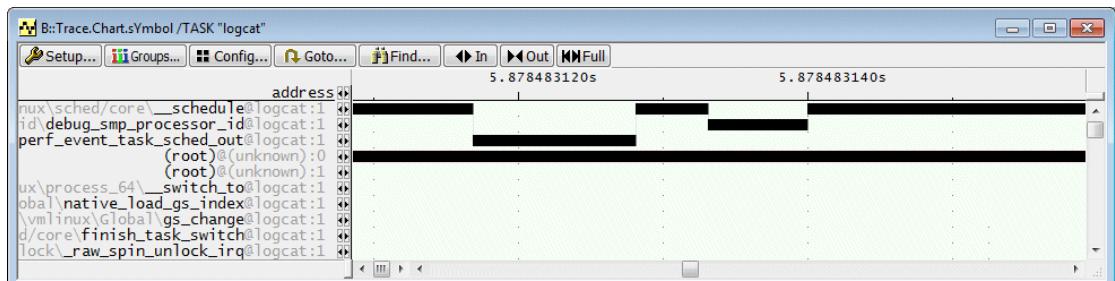
Display function time chart including process information (OS, OS+MMU only)



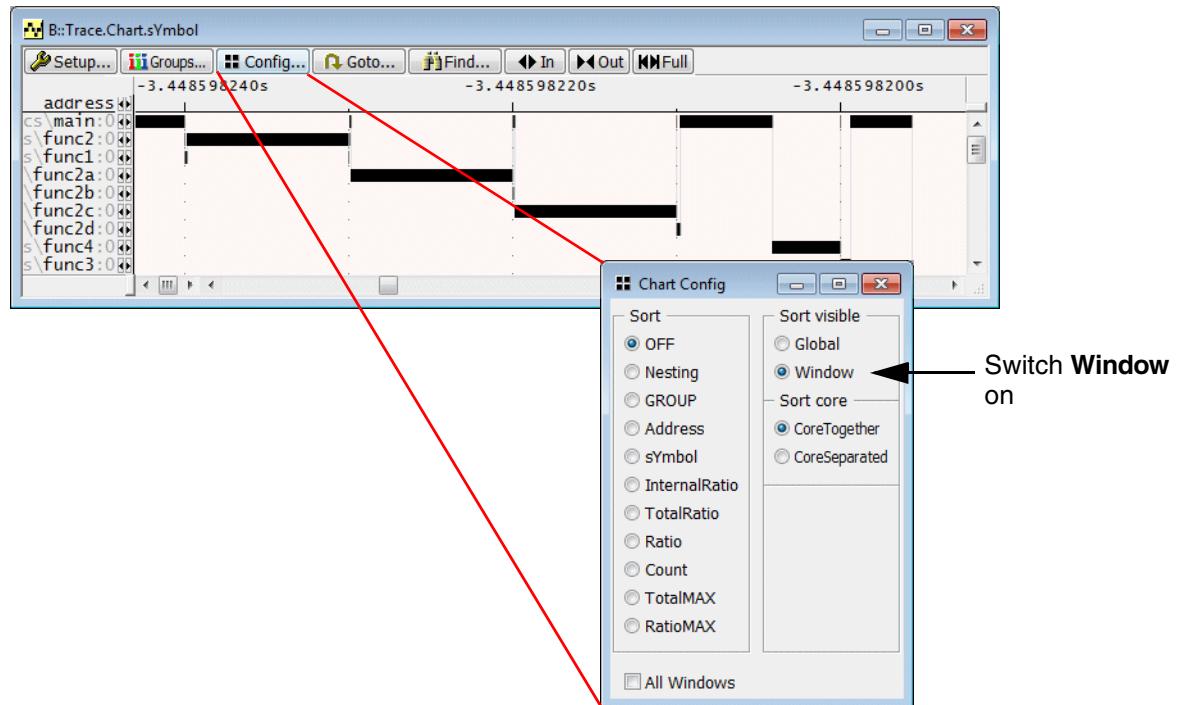
@<task_name>	Process name information
@(unknown)	Function was recorded before first process switch information was recorded

Trace.Chart.sYmbol /TASK <name>

Display function time chart for specified process (OS, OS+MMU only)



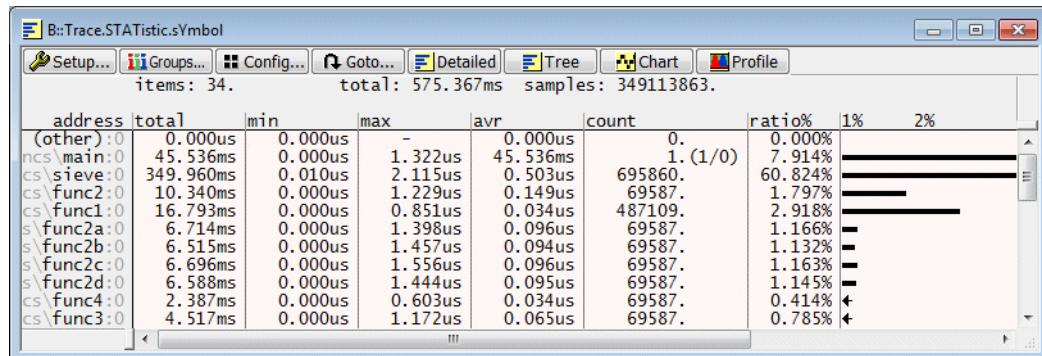
@<task_name>	Process name information
(root)@(unknown)	Everything outside of the specified process.



If **Window** in the **Sort visible** field is switched ON in the **Chart Config** window, the functions that are active at the selected point of time are visualized in the scope of the **Trace.Chart.sYmbol** window. This is helpful especially if you scroll horizontally.

Function Run-time Statistic

Analog to the timing diagram there is also a numerical analysis.

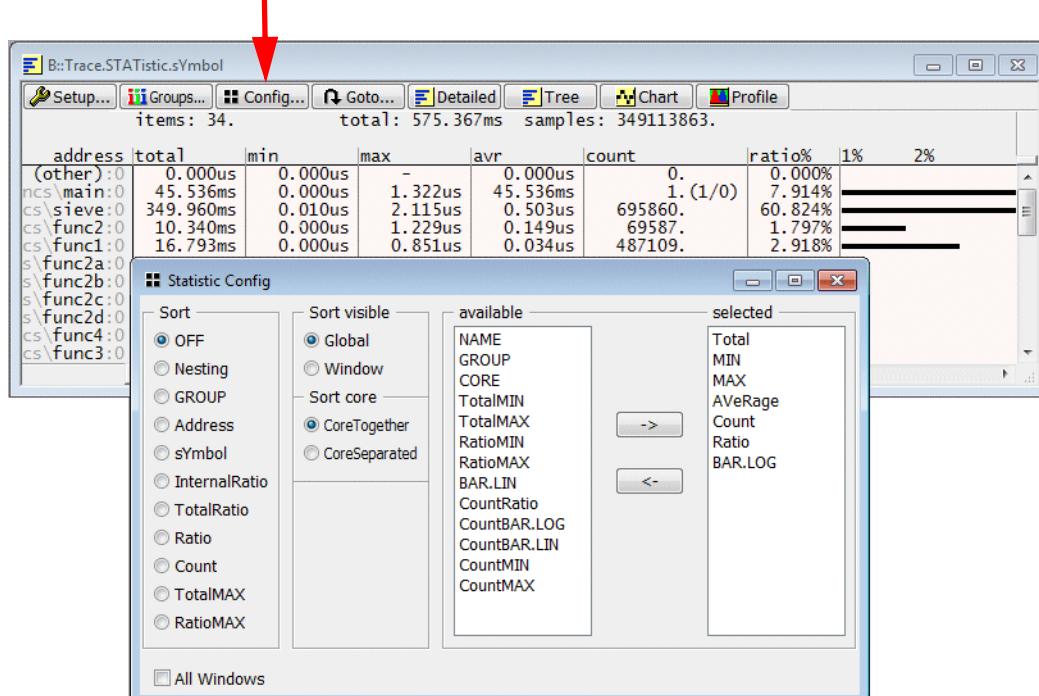


survey	
item	number of recorded functions/symbol regions
total	time period recorded by the trace
samples	total number of recorded changes of functions/symbol regions (program flow continuously in the address range of a function/symbol region)

function details	
address	function/symbol region name (here per core) (other) program sections that can not be assigned to a function/symbol region
total	time period in the function/symbol region during the recorded time period
min	shortest time continuously in the address range of the function/symbol region
max	longest time continuously in the address range of the function/symbol region
avr	average time continuously in the address range of the function/symbol region (calculated by total/count)

count	number of new entries (start address executed) into the address range of the function/symbol region
ratio	ratio of time in the function/symbol region with regards to the total time period recorded

Pushing the **Config** button provides the possibility to specify a different column layout and a different sorting criterion for the address column. By default the functions/symbol regions are sorted by their recording order.



Further Commands

[Trace.PROfileChart.sYmbol](#) Display dynamic program behavior graphically.

[MIPS.PROfileChart.sYmbol](#) Display MIPS for all program symbols graphically.

[MIPS.STATistic.sYmbol](#) Display MIPS for all program symbols numerically.

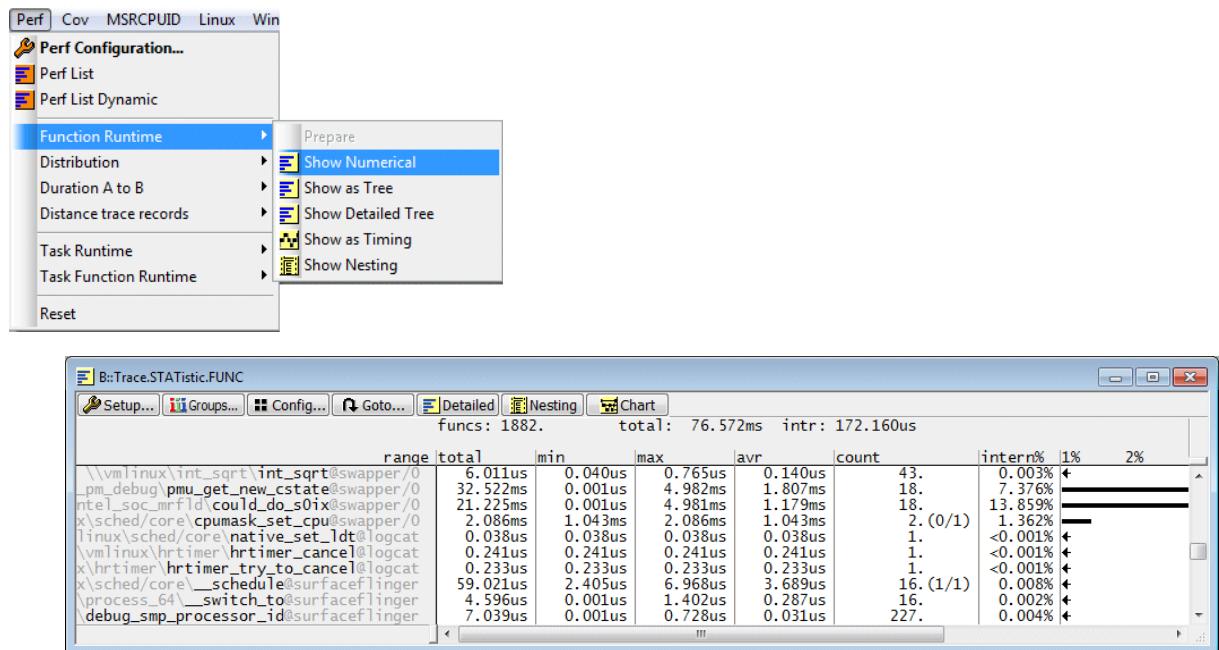
Nesting Function Analysis OS

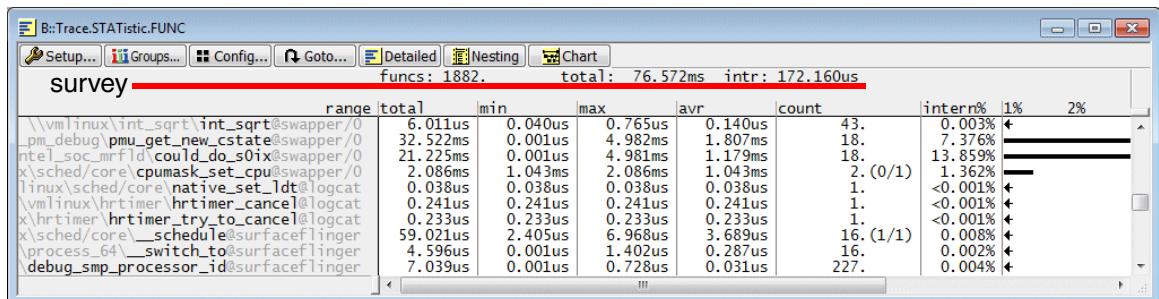
Function nesting analysis for OS requires that OS-aware debugging is configured. For more information refer to “[OS-aware Debugging](#)” (glossary.pdf).

Trace.STATistic.Func

Nesting function run-time analysis

- numeric display
- core information is discarded exceptions are the @ (unknown) task and the @ (interrupt) task



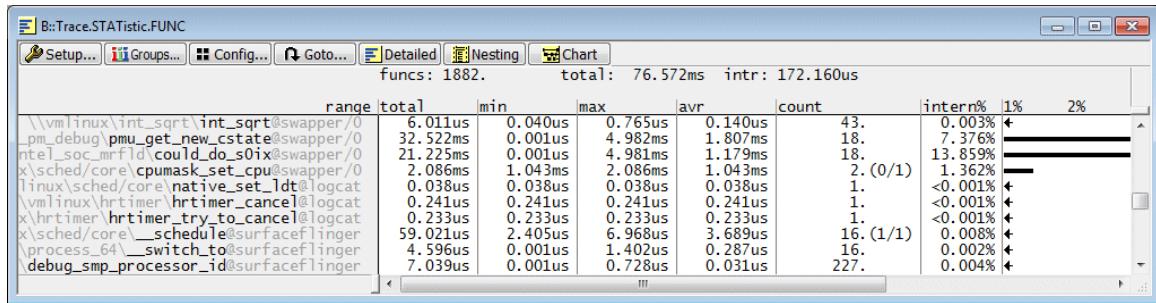


survey	
func	number of functions in the trace
total	total measurement time
intr	total time in interrupt service routines

OVERFLOW funcs: 174. total: 1.392s intr: 902.302us stack overflow at 186892464.

survey (issue indication)	
stopped: <time>	The analyzed trace recording contains program stops. <time> indicates the total time the program execution was stopped.
<number> problems	The nesting analysis contains problems. Please contact support@lauterbach.com .
<number> workarounds	The nesting analysis contains issues, but TRACE32 found solutions for them. It is recommended to perform a sanity check on the proposed solutions.
stack overflow at <record>	The nesting analysis exceeds the nesting level 200. It is highly likely that the function exit for an often called function is missing. The command Trace.STATistic.TREE can help you to identify the function. If you need further help please contact support@lauterbach.com .
stack underflow at <record>	The nesting analysis exceeds the nesting level 200. It is highly likely that the function entry for an often executed function is missing. The command Trace.STATistic.TREE can help you to identify the function. If you need further help please contact support@lauterbach.com .

range Column



columns

range (NAME)	function name, sorted by their recording order as default
--------------	---

\vmlinux\hrtimer\hrtimer_cancel@logcat

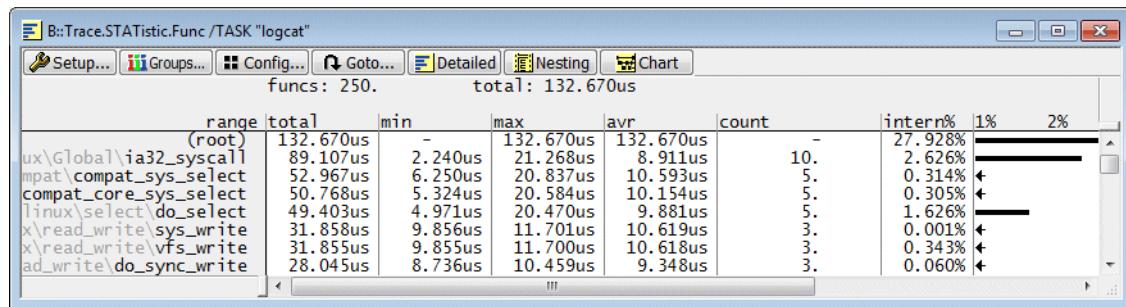
HLL function **hrtimer_cancel** running in process **@logcat**.

Please be aware that no core information is provided for processes and their functions.

Nesting function run-time analysis can also be performed per process.

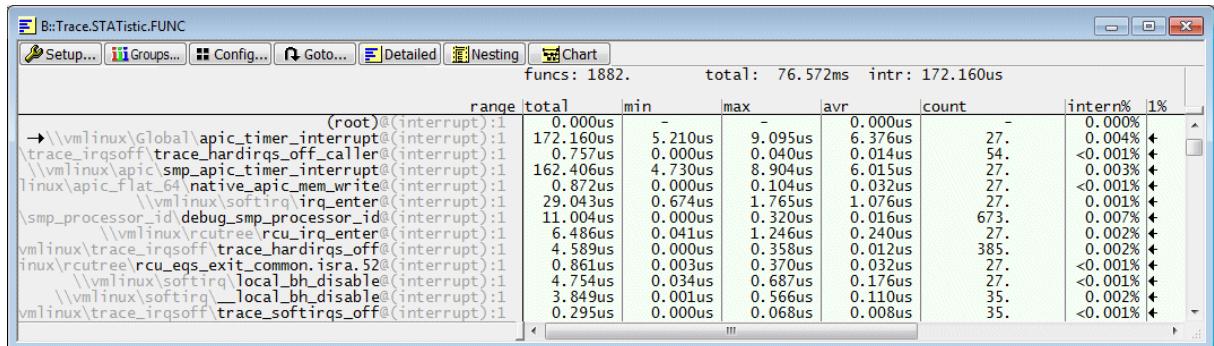
Trace.STATistic.Func /TASK <task_magic> | <task_name> | <task_id>

Trace.STATistic.Func /TASK "logcat"



Interrupt Functions

Interrupt service routines are assigned to the @interrupt task. Core information is provided for the @interrupt task.

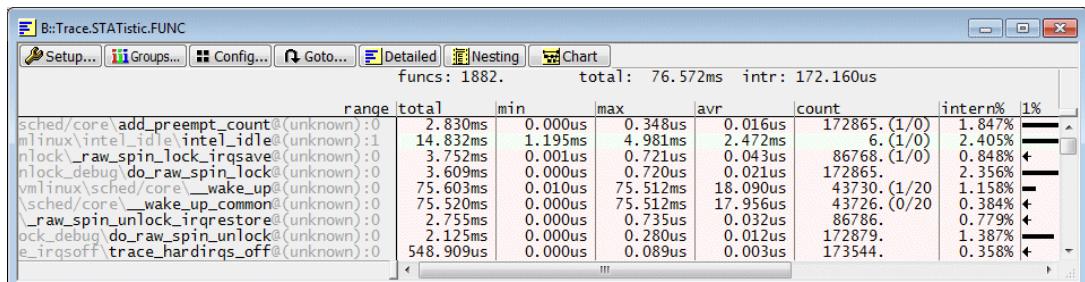


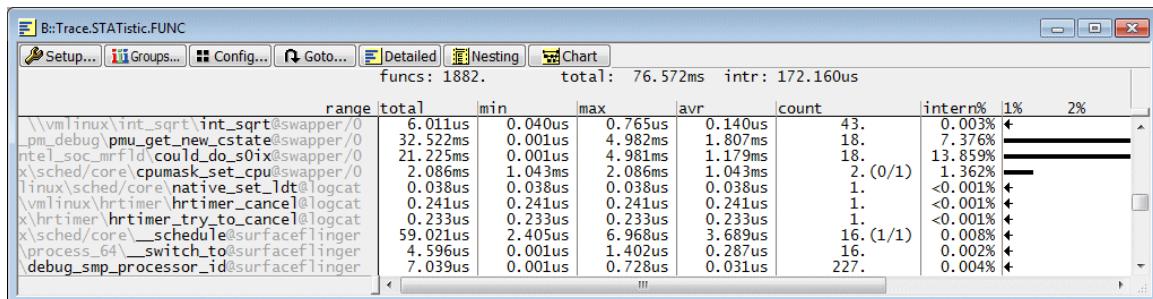
An arrow before the interrupt function indicates the function executed after the interrupt occurred:

→\\vmlinux\\Global\\apic_timer_interrupt@(@interrupt):1

The unknown Task

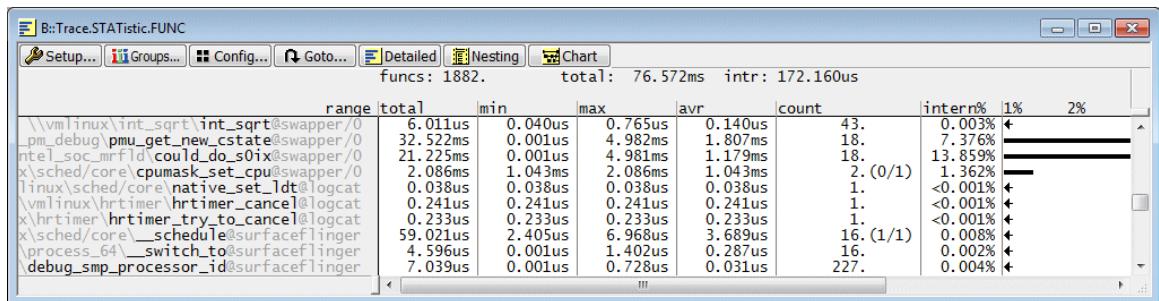
All function recorded before the first process switch is recorded are assigned to the @unknown task. Core information is provided for the @unknown task.





columns (cont.)

total	total time within the function
min	shortest time between function entry and exit, time spent in interrupt service routines is excluded No min time is displayed if a function exit was never executed.
max	longest time between function entry and exit, time spent in interrupt service routines is excluded
avr	average time between function entry and exit, time spent in interrupt service routines is excluded



columns (cont.)

count	number of times within the function
-------	-------------------------------------

If function entries or exits are missing, this is displayed in the following format:

<times within the function>. (<number of missing function entries>/<number of missing function exits>).

3671. (0/1)

Interpretation examples:

1. 2. (2/0): 2 times within the function, 2 function entries missing
2. 4. (0/3): 4 times within the function, 3 function exits missing
3. 11. (1/1): 11 times within the function, 1 function entry and 1 function exit is missing.



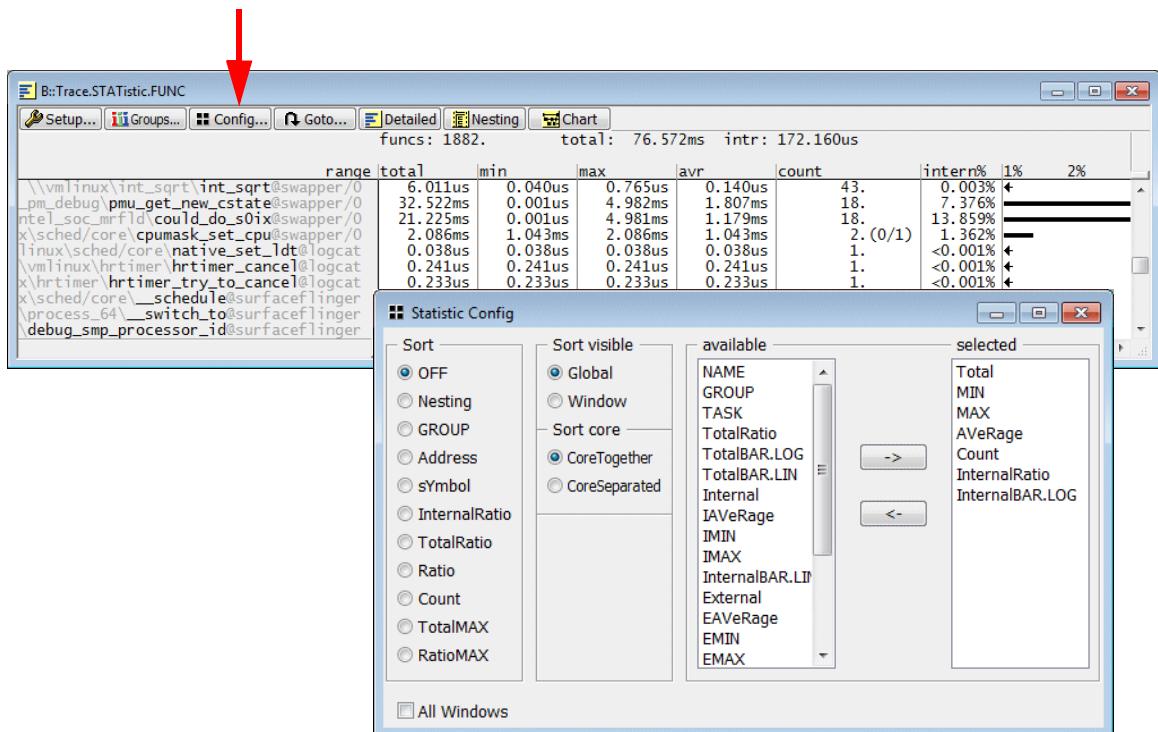
If the number of missing function entries or exits is higher than 1, the analysis performed by the command **Trace.STATistic.Func** might fail due to nesting problems. A detailed view to the trace contents is recommended.

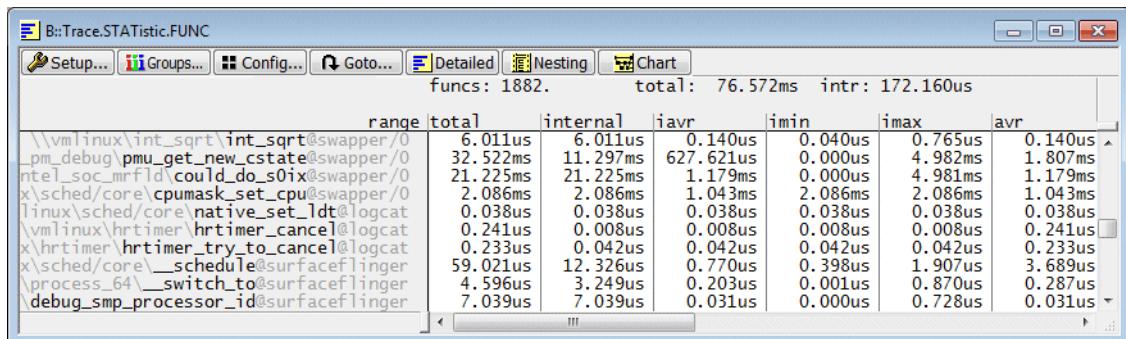
columns (cont.)

intern% (InternalRatio, InternalBAR.LOG)	ratio of time within the function without subfunctions, TRAP handlers, interrupts (net time)
--	--

Net Results

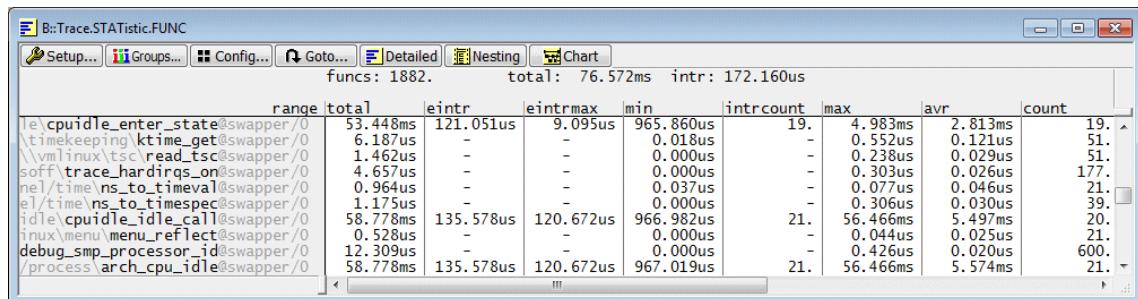
Pushing the **Config...** button allows to display additional columns





columns (cont.) - times only in function

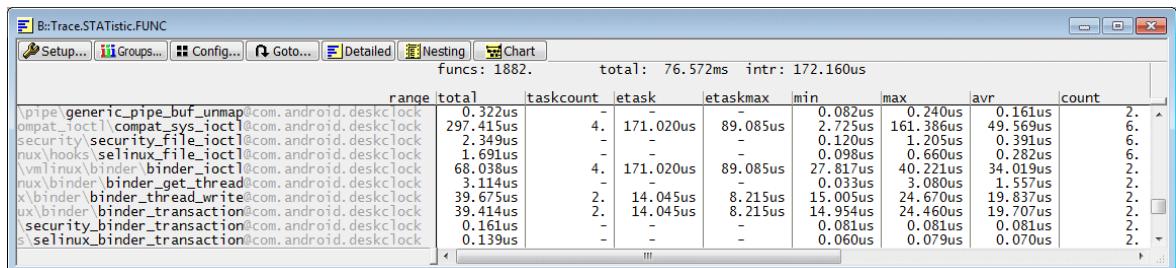
Internal	total time between function entry and exit without called sub-functions, TRAP handlers, interrupt service routines
IAVeRage	average time between function entry and exit without called sub-functions, TRAP handlers, interrupt service routines
IMIN	shortest time between function entry and exit without called sub-functions, TRAP handlers, interrupt service routines
IMAX	longest time spent in the function between function entry and exit without called sub-functions, TRAP handlers, interrupt service routines
InternalRatio	<i><Internal time of function>/<Total measurement time></i> as a numeric value.
InternalBAR	<i><Internal time of function>/<Total measurement time></i> graphically.



columns (cont.) - interrupt times

ExternalINTR	total time the function was interrupted
ExternalINTRMAX	max. time one function pass was interrupted
INTRCount	number of interrupts that occurred during the function run-time

Time in Other Tasks

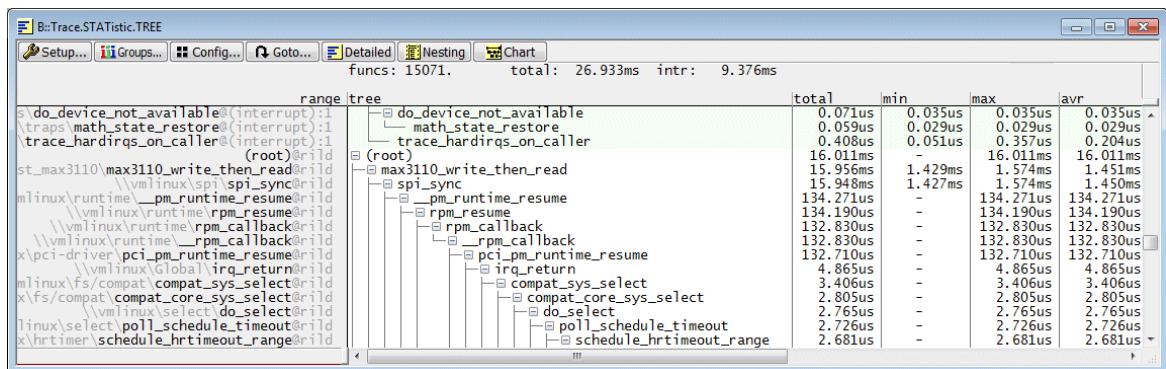
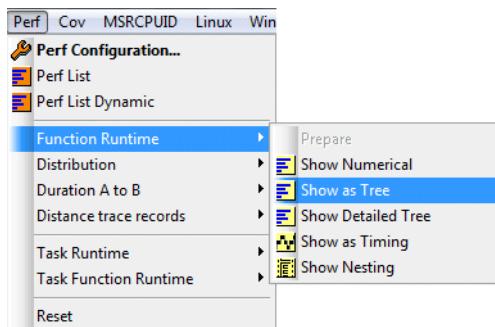


columns - process related information

TASKCount	number of tasks that interrupt the function/task
ExternalTASK	total time in other tasks
ExternalTASKMAX	max. time 1 function/task pass was interrupted by a task

Trace.STATistic.TREE

Nesting function run-time analysis
- tree display



It is also possible to get a task/process-specific tree.

```
Trace.STATistic.TREE /TASK "rild"
```

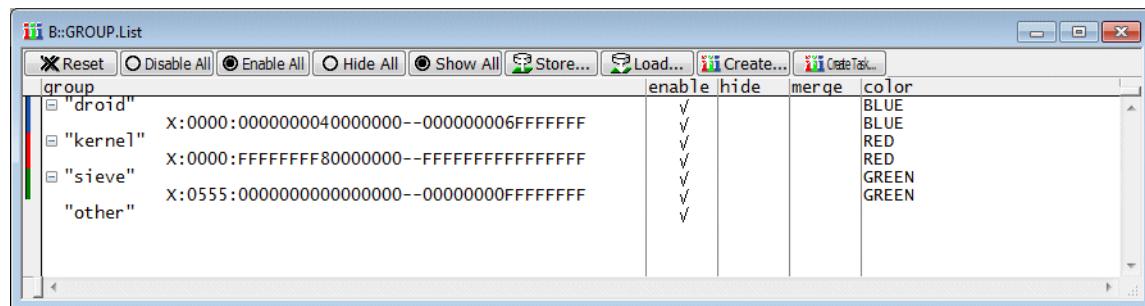
Structure your Trace Evaluation

GROUPs for OS-aware Tracing

TRACE32 PowerView provides the GROUP command to structure the trace evaluation.

If you use a target OS such a Linux, the following groups are created by the Lauterbach scripts and Lauterbach OS menus:

- A GROUP “kernel”, color RED, to mark the OS kernel.
- A GROUP “droid”, color BLUE, to mark virtual machine byte code e.g. Android/Dalvik.
- A GROUP *<process_name>* per process, color GREEN.
- A GROUPs *<module_name>* per kernel module, color YELLOW.

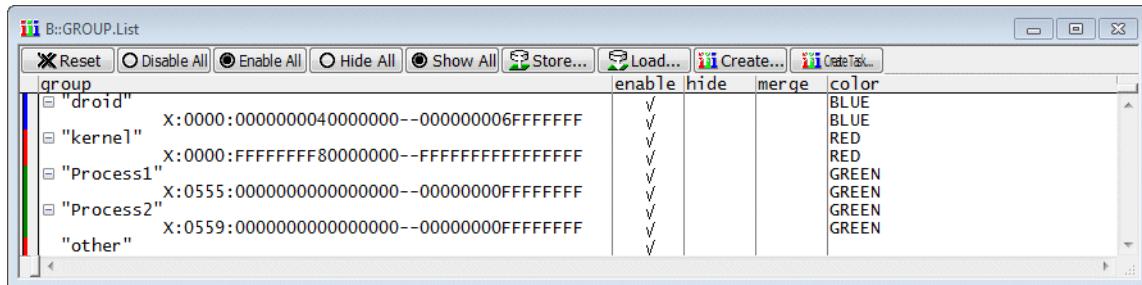


group	enable	hide	merge	color
“droid”	✓			BLUE
“kernel”	✓			BLUE
“sieve”	✓			RED
“other”	✓			RED
				GREEN
				GREEN

A group can have the following statuses:

- enable
- enable + merge
- enable + hide

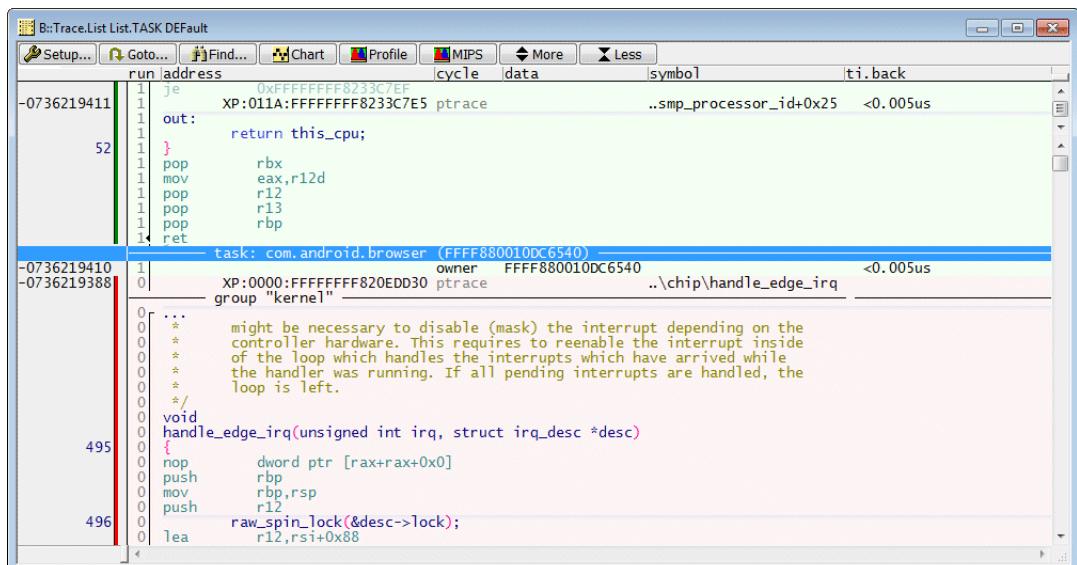
GROUP Status ENable



group	x	enable	hide	merge	color
"droid"	x:0000:000000040000000--00000006FFFFFF	✓			BLUE
"kernel"	x:0000:FFFFFFFFFF8000000--FFFFFFFFFFFFFFFF	✓			BLUE
"Process1"	X:0555:0000000000000000--00000000FFFFFF	✓			RED
"Process2"	X:0559:0000000000000000--00000000FFFFFF	✓			RED
"other"	X:0559:0000000000000000--00000000FFFFFF	✓	✓		GREEN

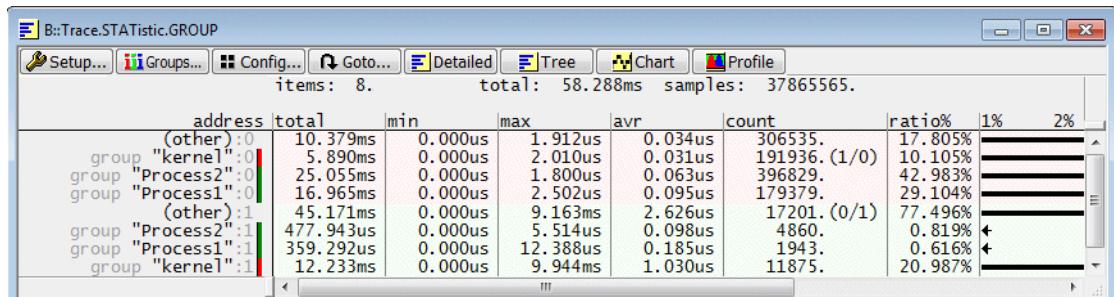
If a GROUP is enabled:

- The trace information recorded for the group members is marked with the color assigned to the group.



run	address	cycle	data	symbol	ti.back
-0736219411	je 0xFFFFFFF8233C7E5			..smp_processor_id+0x25	<0.005us
52	XP:011A:FFFFFFFFFF8233C7E5 ptrace				
	out:				
	return this_cpu;				
	}				
	pop rbx				
	mov eax,r12d				
	pop r12				
	pop r13				
	pop rbp				
	ret				
-0736219410	task: com.android.browser (FFFF880010DC6540) —				
-0736219388	0 owner FFFF880010DC6540				<0.005us
	XP:0000:FFFFFFFFFF820EDD30 ptrace			..\chip\handle_edge_irq	
	group "kernel"				
	...				
	* might be necessary to disable (mask) the interrupt depending on the				
	* controller hardware. This requires to reenable the interrupt inside				
	* of the loop which handles the interrupts which have arrived while				
	* the handler was running. If all pending interrupts are handled, the				
	* loop is left.				
	*/				
495	void handle_edge_irq(unsigned int irq, struct irq_desc *desc)				
	{				
	nop dword ptr [rax+rax+0x0]				
	push rbp				
	mov rbp,rsi				
	push r12				
	raw_spin_lock(&desc->lock);				
496	lea r12,rsi+0x88				

- Group-based trace analyses commands are provided e.g. [Trace.STATistic.GROUP](#).



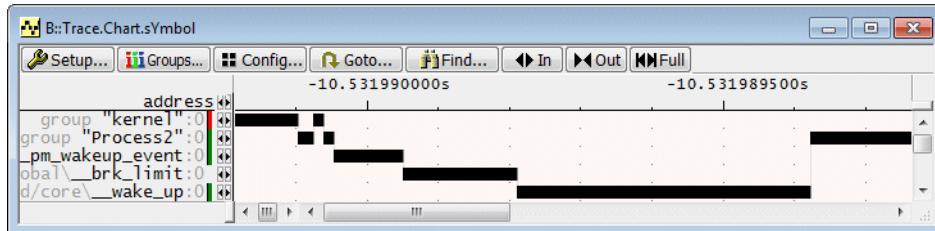
address	total	min	max	avr	count	ratio%	1%	2%
(other):0	10.379ms	0.000us	1.912us	0.034us	306535.	17.805%		
group "kernel":0	5.890ms	0.000us	2.010us	0.031us	191936. (1/0)	10.105%		
group "Process2":0	25.055ms	0.000us	1.800us	0.063us	396829.	42.983%		
group "Process1":0	16.965ms	0.000us	2.502us	0.095us	179379.	29.104%		
(other):1	45.171ms	0.000us	9.163ms	2.626us	17201. (0/1)	77.496%		
group "Process2":1	477.943us	0.000us	5.514us	0.098us	4860.	0.819%		
group "Process1":1	359.292us	0.000us	12.388us	0.185us	1943.	0.616%		
group "kernel":1	12.233ms	0.000us	9.944ms	1.030us	11875.	20.987%		

GROUP Status ENable+Merge

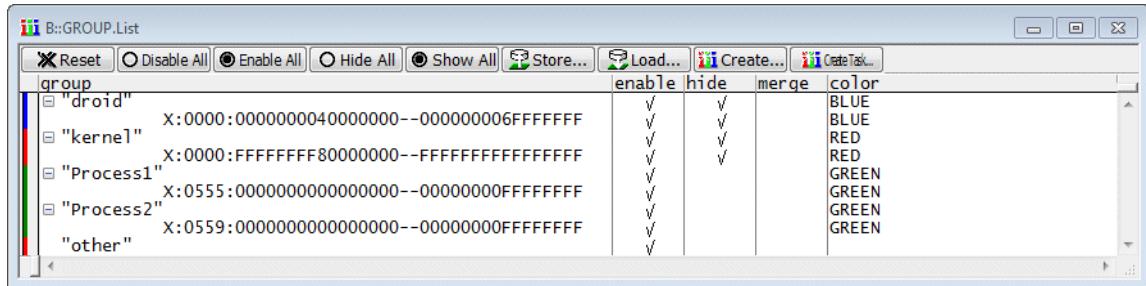
group	x:0000:00000040000000--00000006FFFFFF	enable	hide	merge	color
"droid"	x:0000:00000040000000--00000006FFFFFF	✓		✓	BLUE
"kernel"	x:0000:FFFFFFFF80000000--FFFFFFFFFFFFFFFFFF	✓		✓	RED
"Process1"	x:0555:0000000000000000--00000000FFFFFF	✓		✓	GREEN
"Process2"	x:0559:0000000000000000--00000000FFFFFF	✓		✓	GREEN
"other"	x:0559:0000000000000000--00000000FFFFFF	✓		✓	GREEN

If a GROUP is enabled and merge is checked:

- The group represents its members in all trace analysis windows. No details about group members are displayed.



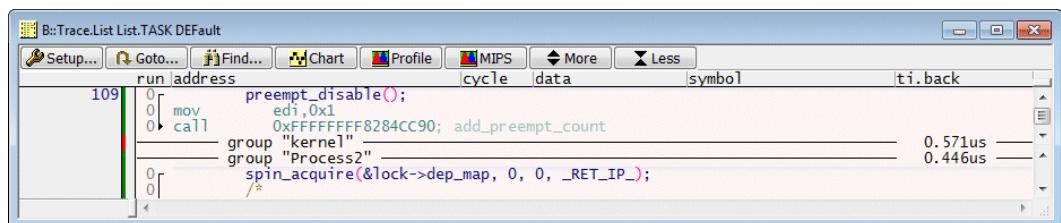
GROUP Status Enable+HIDE



group		enable	hide	merge	color
"droid"	X:0000:00000040000000--00000006FFFFFF	✓	✓		BLUE
"kernel"	X:0000:FFFFFFFF80000000--FFFFFFFFFFFFFF	✓	✓		RED
"Process1"	X:0555:0000000000000000--00000000FFFFFF	✓	✓		GREEN
"Process2"	X:0559:0000000000000000--00000000FFFFFF	✓	✓		GREEN
"other"		✓	✓		GREEN

If a GROUP is enabled and hide is checked:

- The group represents its members in all trace analysis windows. No details about group members are displayed (same as merge checked).
- The trace information recorded for the group members is hidden in the **Trace.List** window.



run	address	symbol	ti.back
109	0	preempt_disable();	
	0	mov	
	0	edi,0x1	
	0	call	0xFFFFFFFF8284CC90; add_preempt_count
	0	group "kernel"	
	0	group "Process2"	
	0	spin_acquire(&lock->dep_map, 0, 0, _RET_IP_);	0.571us
	0	/*	0.446us

GROUP Creation

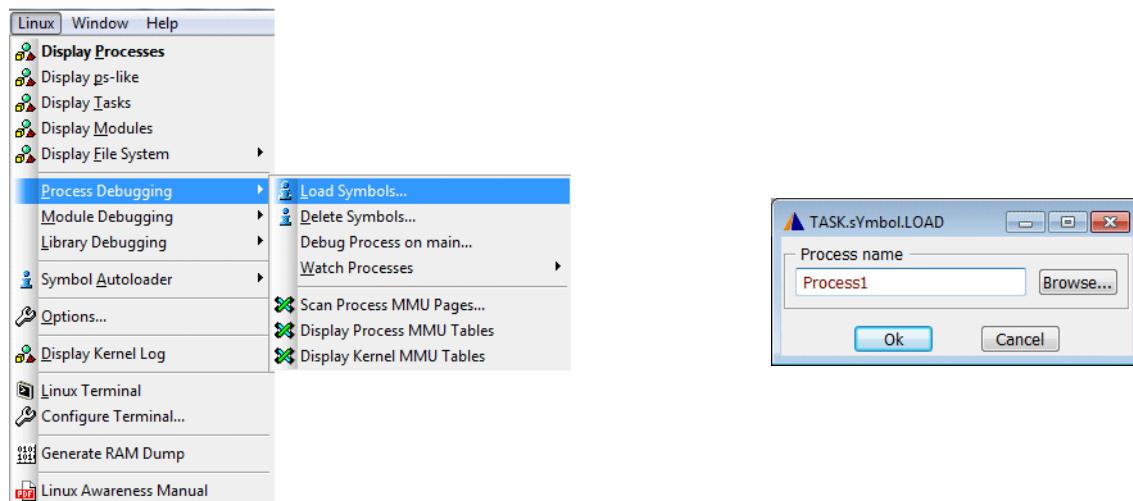
The GROUPs “kernel” and “droid” are typically created in the start-up script that sets up the OS-aware debugging.

GROUP.Create <group_name> <address_range> /<color>

```
GROUP.Create "kernel" XP:0xffffffff80000000--0xffffffffffff /RED
```

```
GROUP.Create "droid"  XP:0x0000000040000000--0x000000006FFFFFF /BLUE
```

<process> or <module> GROUPs are created when their symbol information is loaded.



For more details about GROUPs refer to the **GROUP** command group.