LAUTERBACH
DEVELOPMENT TOOLS

TRACE32 Terminology

MANUAL

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TRACE32 Terminology

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History

20-Jul-23	Initial version of this manual.

Term	Definition
deprecated	This command, function or parameter is old fashioned, but still works. It is important to Lauterbach that customer scripts work in the long term. Nevertheless, we recommend that you update scripts using the new command, function or parameter. Because in the long run, what is deprecated will be removed from the TRACE32 software.
not all core architectures supported	Certain TRACE32 features depend on the characteristics of the core architecture or the resources of the debug and trace logic. Therefore, they cannot be supported for all architectures.

Common Terms and Definitions

Term	Definition
Access class	For details, see **access classes**.
Branch coverage	Every point of entry and exit in the program has been invoked at least once and every branch in the program has been invoked at least once.
Build path	If a files with debug information is loaded (**Data.LOAD.<sub_cmd>**), this file also provides the paths for the high-level source files as they were on the build machine. For details, see **build path**.
Data memory class	For details, see **access classes**.
Debug path	If a files with debug information is loaded (**Data.LOAD.<sub_cmd>**), this file also provides the paths for the high-level source files as they were on the build machine. If TRACE32 is not running on the build machine, the build paths may not be valid and have to be adjusted for the debug host. The adjusted paths are called the debug paths. For details, see **build path**.
Decision coverage	Every point of entry and exit in the program has been invoked at least once and every decision in the program has taken all possible outcomes at least once.
Kernel **Subject area**: OS Awareness	The operating system itself, without the tasks.
MCDS	MCDS (Multi Core Debug Solution) is a peripheral block that implements trace and trigger functions for the Infineon TriCore and C166/XC2000 devices. For more details refer to **MCDS in Infineon TriCore AURIX MCUs**.
OS-aware debugging	The debugger is aware of an operating system in the target, allowing additional views (like tasks) and capabilities (like task aware breakpoints). For details, see **OS-aware debugging**.
OS-aware tracing	The trace can be evaluated with respect to tasks, e.g. calculating task run times or function nesting of tasks. For details, see **OS-aware tracing**.

Term	Definition
Program memory class	For details, see **access classes**.
Statement coverage	Every statement in the program has been invoked at least once.

Abbreviations

The following is a list of abbreviations that occur in the context of debugging and tracing embedded systems.TRACE32 specific abbreviations are indicated by (TRACE32).

AGBT	Aurora Gigabit Trace (Infineon TriCore AURIX TC2xx, TC3xx)
AMP	Asymmetric Multi-Processing
BSDL	Boundary Scan Description Language
CADI	Component Architecture Debug Interface
cJTAG	Compact JTAG
DAP	CoreSight Debug Access Port (Arm)
DAP	Device Access Port (infineon)
DXCM	DAP over CAN Messages (Infineon)
DXCPL	DAP over CAN Physical Layer
ETB	Embedded Trace Buffer
ETF	Embedded Trace Fifo
ETM	Embedded Trace Macrocell
ETR	Embedded Trace Router
GDB	GNU Debugger
GTL	Generic Transactor Library
HLL (TRACE32)	High Level Language
HSM	Hardware Security Module (Infineon)
HSSTP	High Speed Serial Trace Port
ITM	Instrumentation Trace Macrocell
JTAG	Joint Test Action Group
MCD (TRACE32)	Multi-Core Debug
MC/DC	Modified Condition/Decision Coverage

MCDS	Multi-Core Debug Solution (Infineon)
MMU	Memory Management Unit
SGBT	Serial Gigabit Trace (Infineon TriCore AURIX TC4x)
SMP	Symmetric Multi-Processing
SoC	System-on-Chip
STP	System Trace Protocol
STM	System Trace Macrocell
SWD	Serial Wire Debug
SWO	Serial Wire Output
SWV	Serial Wire Viewer
TAP	Test Access Port
TPIU	Trace Port Interface Unit
XCP	Universal Measurement and Calibration Protocol

Power Debug Modules

PowerDebug Module with USB

- PowerDebug E40, deliverable since 06/2022
  Featuring 64 MiB trace memory for the first time.
- PowerDebug Module USB 3.0, deliverable from 05/2013 to 03/2023
- PowerDebug Module USB 2.0, deliverable from 04/206 to 04/2013

PowerDebug Module with USB and Ethernet

- PowerDebug X50, deliverable since 03/2023
  Featuring 64 MiB trace memory
- PowerDebug PRO Ethernet, deliverable from 12/2014 to 06/2023
  Featuring 64 MiB trace memory for the first time.
- PowerDebug Module Ethernet, deliverable from 02/2003 to 12/2014

Trace Modules

- PowerTrace III, deliverable since 08/2022

  Connect to the target via
  - *TRACE32 AutoFocus II Preprocessor* (parallel trace port) or other parallel preprocessor pre-licensed for a core trace protocol at delivery
  - *TRACE32 Serial Preprocessor* pre-licensed for a core trace protocol at delivery

  featuring up to 8 GigaByte of trace memory, trace streaming up to 400 MByte/s and *TRACE32 Mixed-Signal Probe*

- PowerTrace II, deliverable from 06/2007 to 07/2022

  Connect to the target via
  - *TRACE32 AutoFocus II Preprocessor* (parallel trace port) or other parallel preprocessor pre-licensed for a core trace protocol at delivery
  - *TRACE32 Serial Preprocessor* pre-licensed for a core trace protocol at delivery

  featuring up to 4 GigaByte of trace memory, trace streaming up to 200 MByte/s and *TRACE32 Standard Probe*

- PowerTrace Serial 2, deliverable since 06/2023

  Connected directly to the target, pre-licensed for a core trace protocol at delivery, featuring up to 8 GigaByte of trace memory, trace streaming up to 400 MByte/s and *TRACE32 Mixed-Signal Probe*

  Connected to target via *Aurora 2 Preprocessor for PowerTrace Serial* to reach higher speeds

- PowerTrace Serial, deliverable from 11/2016 to 05/2023

  Connected directly to the target, pre-licensed for a core trace protocol at delivery, featuring up to 4 GigaByte of trace memory, trace streaming up to 200 MByte/s and*TRACE32 Standard Probe*

  Connected to target via *Aurora 2 Preprocessor for PowerTrace Serial* to reach higher speeds