CONFIDENTIAL

User's Guide

R-Car V4M
FCBGA 19.0sq

PCB verification guide for LPDDR4X

RENESAS
SoCs for Automotive

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The purpose of this guide

This guide helps PCB design engineers to verify their design and arrive to their design goal.

The timing budget for DDR interface (DDR-IF) is composed of controller chip, DRAM and interconnect (PKG and PCB). Therefore, it is important to manage interconnect (PKG and PCB) timing. This guide describes a) PCB design restrictions, b) verification items and c) how to measure them.

It is indispensable to satisfy PCB restrictions described in this guide to enable LPDDR4X function in user's system. Renesas recommends the customer to confirm satisfying restrictions in this guide and to check signal quality based on JEDEC standard.

All information shown in this guide, including product specifications, represents the information at the time of publication and is subject to change by Renesas Electronics Corp. without notice. Please review the latest information published by Renesas Electronics Corp.

SOC means R-Car V4M (FCBGA) in this document.

R-Car V4M

DDR PCB Verification Guide

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1 Introduction

1.1 Overview

This document provides PCB verification guide on DDR-IF. The purpose of this guide is to help PCB design engineers to design signals and power supplies of DDR-IF in their PCB design. DDR-IF design needs to satisfy the waveform quality specification defined in JEDEC. To achieve this, intensive signal and power integrity verification are necessary with the use of SOC, PCB and DDR model (connected system level simulation of these models).

The chapters of this guide are organized as follows:

- Chapter 1 describes operating conditions, signal and power name list of DDR-IF, and verification method and items.
- Chapter 2 describes simulation setup for the signal and power integrity verification in the system level. Deliverables provided by Renesas are SOC model and information. System level simulation can be performed using PCB model to be prepared by customer and DRAM model provided by DRAM vender.
- Chapter 3 describes recommended IO setting and PCB configuration for all DDR-IF signal and power.
- Chapter 4 describes verification items and method of signal line: verification item list, its target value, and measurement method for simulated waveform.
- Chapter 5 describes verification items and method of IO Power Distribution Network (PDN): verification item list, its target value (target impedance), and measurement method for PDN impedance.

1.2 Operating conditions

(1) Data transfer rate
- 1rank: 4267Mbps
- 2rank: 4267Mbps

*) Data transfer rate depends on DRAM the customer uses.

(2) DRAM and its connection

Table 1-1 DRAMs to be used and connections *1)

DRAM type	Bit count	Number of Rank *2)	Number of connected DRAMs	DRAM grade	DRAM package
LPDDR4X	X32	1 or 2	1	LPDDR4X-4267	200-ball x32 Discrete Package, 0.80 mm x 0.65 mm using MO-311

*1) Please refer to the SOC User's Manual for the supported DRAM densities.

*2) Please note the "(1) Data transfer rate".

(3) DRAM specification
- JEDEC standard : JESD209-4C(LPDDR4)
  JESD209-4-1A (LPDDR4X)

(4) Training function (must be used)

Table 1-2 Training function

Training		Initialization	Periodic	Note
IO ZQ Calibration	SOC	Yes	Yes (Except for CK)	*1, *2
	DRAM	Yes	Yes	*1, *3
CA/CS	Timing	Yes	-	
	Vref	Yes	-	
Write Leveling		Yes	-	
Read Gate Training		Yes	Yes	*4
Read Data Eye Training	Timing	Yes	Yes	
	Vref	Yes	-	
Write Data Eye Training	Timing	Yes	Yes	*5
	Vref	Yes	-	

*1: Driver/Receiver impedance calibration across process, temperature, and voltage.
*2: Driver impedance of CK signals are not calibrated periodically after the initialization, but its degradation is already taken into account in the spec of restrictions.
*3: For multi-rank DRAM, IO ZQ Calibration cannot be performed at the same time. Please see section 3.2.1.
*4: To compensate tDQSCK and tDQSCK_temp/volt.
*5: To compensate tDQS2DQ and tDQS2DQ_temp/volt.

(5) The function to keep the signal quality (must be used)
- Turn on On Die Termination (ODT).
- Use DBI in WRITE and READ mode.

(6) Supported topology for CA
- Point to Point (P2P) topology

1.3 Signal and power name of DDR-IF

Descriptions and abbreviations of signal name are defined as Table 1-3, Table 1-4, Table 1-5, and Table 1-6. “p” is from 0 to 1 in these tables.
DDR power supply pins are shown in Table 1-7.

Table 1-3 Signal line (DQS/DQS#, DQ, DM)

Pin name	Description	Abbreviation
Mp_WCK[1:0]_T/Mp_WCK[1:0]_C	Data strobe	DQS/DQS#
Mp_DQ[15:00]	Data Input/Output	DQ
Mp_DMI[1:0]	Data Mask Inversion	DM

Table 1-4 Signal line (CK/CK#, ADD/CMD)

Pin name	Description	Abbreviation
Mp_CK_T/Mp_CK_C	Clock	CK/CK#
Mp_CA[6:2], Mp_CA0 *1)	Command/Address	CA
Mp_LP4XCS[1:0]	Chip select	CS
Mp_LP5CS[1:0]_LP4XCKE[1:0]	Clock enable	CKE
M1_RESET_N	Reset	RESET

*1) Mp_CA1 cannot be used for LPDDR4X. Please use Mp_CA6 instead of Mp_CA1.

Table 1-5 Other signal line

Pin name	Description	Abbreviation
Mp_ZQ	Calibration reference	ZQ
M01_BKUP	Backup control	-

Table 1-6 Signal line (unused)

Pin name	Description	Abbreviation
Mp_RDQS[1:0]_T/Mp_RDQS[1:0]_C	Open	-
Mp_CA1 *1)	Open	-
Mp_ATB[1:0]	Open	-
M1_PLLTEST	Open	-

*1) Mp_CA1 cannot be used for LPDDR4X. Please use Mp_CA6 instead of Mp_CA1.

Table 1-7 Power supply

Pin name	Description	Abbreviation
VDDQVA_DDRp	Power supply for DDR-IF IO	-
VDDQX_DDRp	Power supply for DDR-IF IO	
VDD_DDRPLL01	Power supply for DDR PLL	-
VSS	Ground pin (common with other power supplies)	-

1.4 Verification items and method

Figure 1-1 shows the interconnect between SOC and DRAM in DDR system. In transmitting and receiving data, drivers on SOC/DRAM transmit the data to DRAM/SOC via SOC PKG and PCB during Write/Read access (Figure 1-1 shows Write image).

Therefore, in designing DDR-IF, there are verification items on signal line and IO PDN shown in Table 1-8 and next page. Verification items are summarized from Table 4-1 to Table 4-12, and Table 5-1.

All restrictions must be satisfied in your PCB design. Please refer to chapter 4 and 5 about each verification items and method in detail.

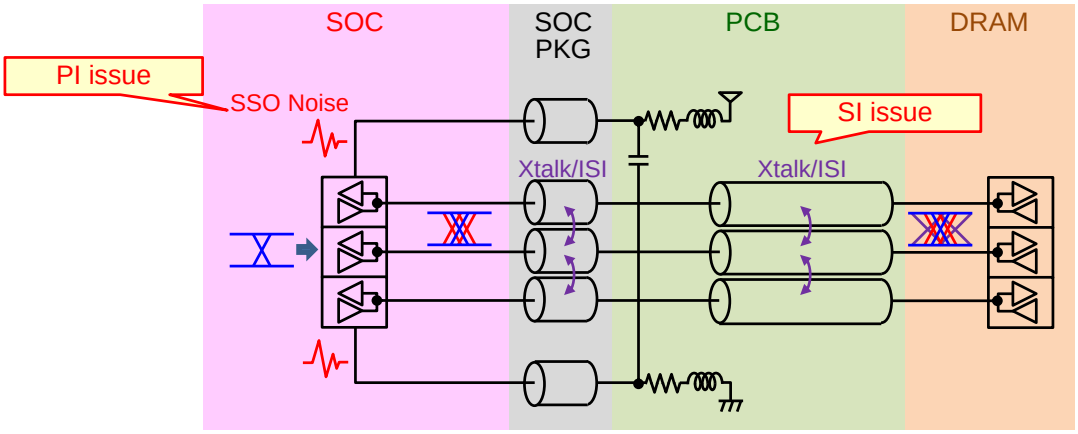


Figure 1-1 Interconnect in DDR System

Table 1-8 Verification items of LPDDR4X DDR-IF

Verification target	Category	Verification items	reference
Signal line	Skew restrictions	Intra-pair skew, data-strobe skew, data-data skew and so on.	Section 4.1.1
	Flight-time restrictions	Flight-time	Section 4.1.2
	Timing restrictions	Eye, pulse width, jitter	Section 4.1.3
	Waveform restrictions	Amplitude, slew rate, cross point, overshoot, undershoot and so on	Section 4.1.4
IO power distribution network	IO power distribution network restrictions	Power supply impedance	Section 5.1

(1) Signal line restrictions

i) Skew restrictions

Some kind of de-skew trainings need to be performed in order to realize high speed data transfer. It leads to the decrease of excessive serpentine routing and the relaxation of restrictions for PCB skew.

However, PCB skew and delay between DDR-IF signals must be managed within adjustable range for SOC because that range is finite.

In the verification of skew restrictions, only path mismatch which is not physical length but electrical length should be measured.

ii) Flight-time restrictions

As well as skew restrictions, the flight-time restrictions must be satisfied in your PCB design.

iii) Timing restrictions

Timing at DRAM and SOC receiver is degraded because PKG and PCB have some impedance mismatch, loss, inter-signal coupling and ground bounce which cause the reflection, Inter-Symbol Interference (ISI) and Cross talk (Xtalk). It's called Signal Integrity (SI) issue. In order to transmit the data correctly, these degradation components should be controlled so that all DDR signals satisfy JEDEC and SOC specification. In the verification of timing restrictions, signal timing should be verified taking these ISI and Xtalk into account.

iv) Waveform restrictions

Waveform (amplitude, slew rate and so on) at DRAM receiver is also degraded due to Xtalk, ISI and reflection.

In the verification of waveform restrictions, signal waveform should be verified taking these degradations into account.

(2) IO power distribution network restrictions

Output waveform of SOC is degraded because non-ideal power supply causes Simultaneous Switching Output/Input (SSO/SSI) noise. It is called Power Integrity (PI) issue. In the verification of IO power distribution network restrictions, target impedance for IO PDN must be satisfied.

For SI and PI issue, PCB design for DDR-IF need to satisfy the timing and waveform restrictions as SI verification and the target impedance of IO PDN as PI verification. Target values of timing and waveform restrictions in this guide are more severe than JEDEC standard because we need to consider the influence of power noise. Then, PI degradation for timing and waveform restriction is estimated by PI simulation based on the target impedance and is included in its target values.

2 Deliverables and simulation setup

This section shows necessary materials for DDR-IF verification. SOC models are provided by Renesas. Customer need to prepare PCB models and get DRAM models from DRAM vender.

2.1 Information and models provided by Renesas

1) BGA pin assignments

2) IO buffer Model

IO buffer model (IBIS Ver.5.0): r8a779h0.ibs (Rev1.00)

The package models in the IBIS model ([Package], [PIN]) are not valid for Xtalk/ISI simulation because of its accuracy, therefore using the dedicated package model must be used (see below). This IBIS model has the components for power aware simulations, but these components are not supported.

3) PKG model of DDR-IF signal

PKG model of DDR-IF signal:

RCV4M_FCBGA19p0sq_DDR_Mp.s78p (Rev1.00)

These PKG models can simulate interaction only within signal block which correspond to model name. “p” is from 0 to 1 in each model name.

4) SOC model of IO PDN for target impedance confirmation

SOC PDN model of DDR IO power supply for

VDDQVA_DDRp :

RCV4M_FCBGA19p0sq_VDDQVA_DDRp.s9p (Rev1.00)

VDDQX_DDRp :

RCV4M_FCBGA19p0sq_VDDQX_DDRp.s4p (Rev1.00)

“p” is from 0 to 1 in model name.

5) SOC User’s Manual

2.2 Models to be prepared by customer

1) PCB model of DDR-IF signal between SOC and DRAM
(Xtalk and impedance mismatch of PCB trace should be included in this model.)

2) PCB model of IO PDN for target impedance verification

2.3 Models provided by DRAM vendor

DRAM model (IO model, PKG model and so on)

2.4 Simulation setup

Figure 2-1 shows a circuit diagram image in verification of signal line. Renesas provides IO buffer model and PKG model. Customer need to prepare PCB model. DRAM model is provided by DRAM vendor.

Figure 2-2 shows a circuit diagram image in verification of DDR IO PDN. Customer need to prepare PCB model, connect it with SOC model provided by Renesas and verify the impedance of DDR IO power supply which is shown as Z_{PDN} in Figure 2-2.

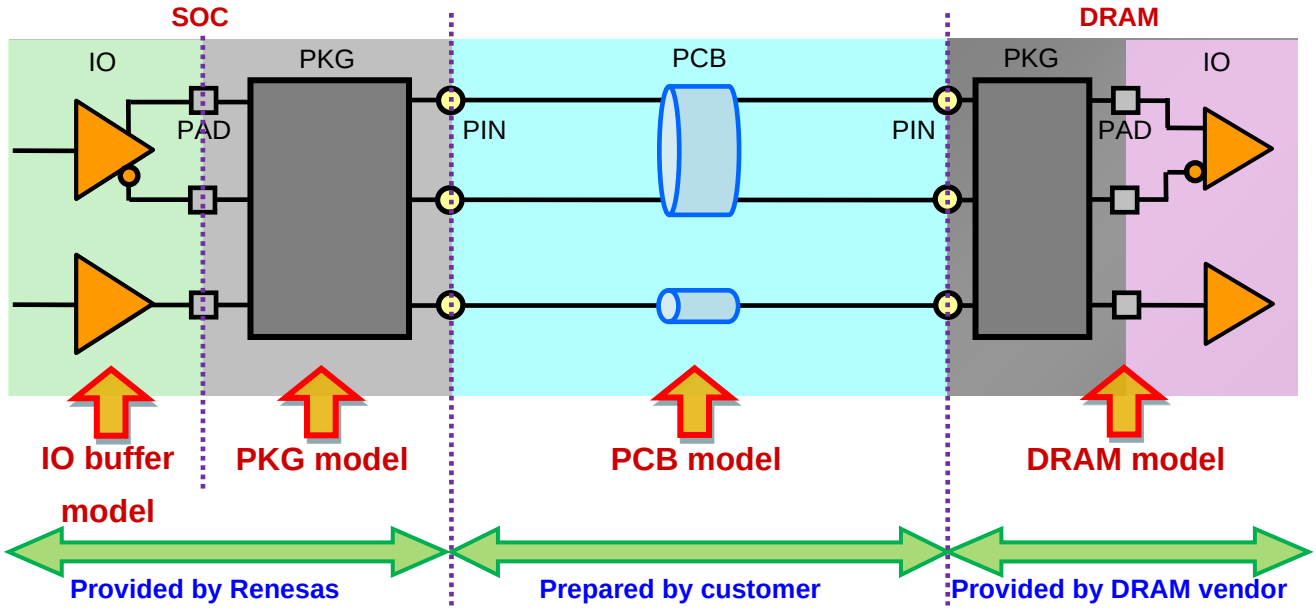


Figure 2-1 Measurement circuit connection image in verification of signal line

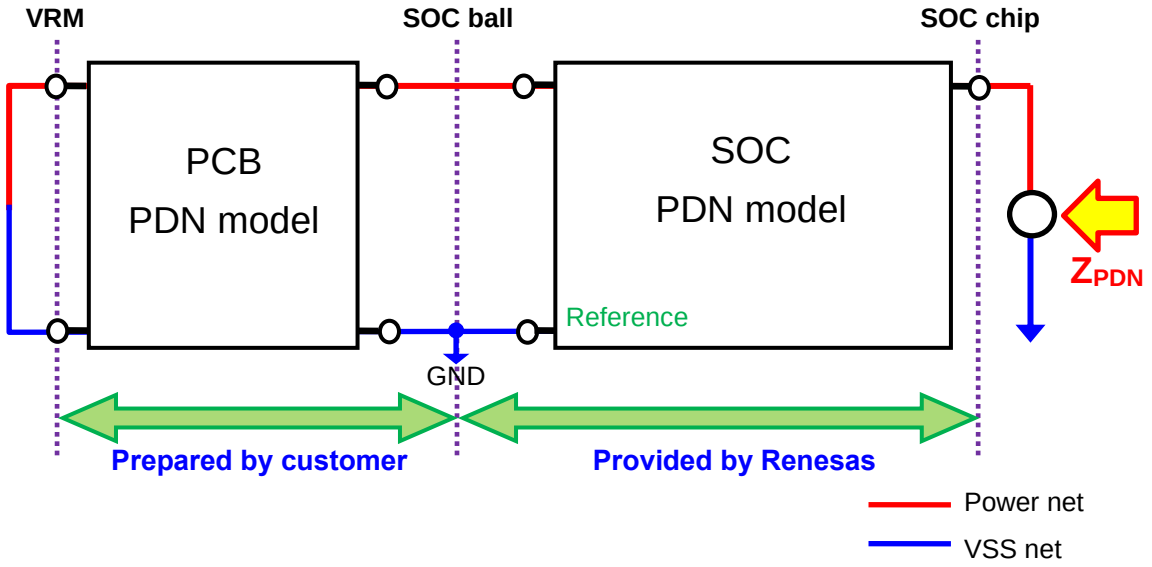


Figure 2-2 Measurement circuit connection image in verification of DDR IO PDN

3 IO setting and PCB configuration

3.1 Signal lines of high-speed DDR IF signals

PCB topology of each signal group is shown in Section 3.1.1 - 3.1.8. Each Table shows IO and ODT setting recommendation. Customer should evaluate all restrictions described in section 4 based on these recommendations. IO setting and IBIS model to be used in each signal are summarized in section 3.1.9.

3.1.1 DQS/DQS#

Table 3-1 DQS/DQS# setting

Command	SOC		DRAM		SOC IBIS model
	Driver setting	ODT	Driver setting	ODT	
Write	PU : 34ohm PD : 34ohm	OFF	OFF	60ohm	DQS, DQS# : lpddr4x_ocd_34p_34n_diff
Read	OFF	40ohm	VOH=VDDQ*0.5 SOC ODT=RZQ/6 PDDS=RZQ/6	OFF	DQS, DQS# : lpddr4x_odt_40_diff

Figure 3-1 DQS/DQS# PCB topology

3.1.2 DQ, DM

Table 3-2 DQ, DM setting

Command	SOC		DRAM		SOC IBIS model
	Driver setting	ODT	Driver setting	ODT	
Write	PU : 34ohm PD : 34ohm	OFF	OFF	60ohm	lpddr4x_ocd_34p_34n
Read	OFF	40ohm	VOH=VDDQ*0.5 SOC ODT=RZQ/6 PDDS=RZQ/6	OFF	lpddr4x_odt_40

Figure 3-2 DQ, DM PCB topology

3.1.3 CK/CK#

Table 3-3 CK/CK# setting

Command	SOC		DRAM		SOC IBIS model
	Driver setting	ODT	Driver setting	ODT	
Write	PU : 34ohm PD : 34ohm	OFF	OFF	60ohm *1)	CK, CK# : lpddr4x_ocd_34p_34n_diff

*1) We recommend CK ODT is set to 60ohm to satisfy the JEDEC specification because CK IO calibration is only occurred in initial sequence and VT drift after that is not adjusted.

Figure 3-3 CK/CK# PCB topology

3.1.4 CA

Table 3-4 CA setting

Command	SOC		DRAM		SOC IBIS model
	Driver setting	ODT	Driver setting	ODT	
Write	PU : 40ohm PD : 40ohm	OFF	OFF	60ohm *1)	lpddr4x_ocd_40p_40n

*1) CA ODT setting of DRAM is referred to the same MR with CK. Therefore, CA ODT value should be the same one with CK.

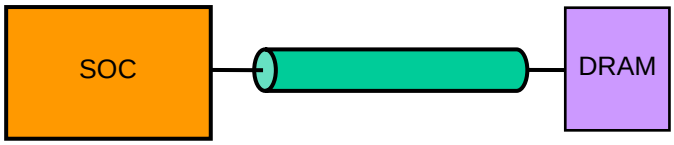


Figure 3-4 CA PCB topology

3.1.5 CS

Table 3-5 CS setting

Command	SOC		DRAM		SOC IBIS model
	Driver setting	ODT	Driver setting	ODT	
Write	PU : 40ohm PD : 40ohm	OFF	OFF	60ohm *1)	lpddr4x_ocd_40p_40n

*1) CS ODT setting of DRAM is referred to the same MR with CK. Therefore, CS ODT value should be the same one with CK.

Figure 3-5 CS PCB topology

3.1.6 CKE

Table 3-6 CKE setting

Command	SOC		DRAM		SOC IBIS model
	Driver setting	ODT	Driver setting	ODT	
Write	PU : 640ohm *1) PD : 240ohm	OFF	-	- *2)	lpddr4x_cke_240p_240n

*1) The model name is “lpddr4x_cke_240p_240n”, but only the drivability on PU side is about 640ohm.

*2) There is no ODT function for CKE.

Figure 3-6 CKE PCB topology

3.1.7 RESET

Table 3-7 RESET setting

Command	SOC		DRAM		SOC IBIS model
	Driver setting	ODT	Driver setting	ODT	
Write	PU : 50ohm PD : 50ohm	OFF	-	- *1)	lpddr4x_ocd_50p_50n

*1) There is no ODT function for RESET.

Figure 3-7 RESET PCB topology

3.1.8 ODT

LPDDR4X DRAM ignores ODT_CA_A and ODT_CA_B. Please contact DRAM vendor about those connection.

3.1.9 Summary of recommended IO settings

SOC IBIS models for recommended IO setting described before are listed in the following tables: Table 3-8, Table 3-9 and Table 3-10. Proper DRAM model must be selected based on materials provided by DRAM vender.

Table 3-8 Recommended settings of SOC IBIS and DRAM IO model in CA

Pin name	Recommended setting	
	SOC IBIS model	DRAM IO model setting*1)
CK, CK#	lpddr4x_ocd_34p_34n_diff	ODT = 60ohm
CA	lpddr4x_ocd_40p_40n	ODT = 60ohm
CS	lpddr4x_ocd_40p_40n	ODT = 60ohm
CKE	lpddr4x_cke_240p_240n	ODT=Off
RESET	lpddr4x_ocd_50p_50n	ODT=Off
ODT	-	-

Table 3-9 Recommended settings of SOC IBIS and DRAM IO model in DQ WRITE mode

Pin name	Recommended setting	
	SOC IBIS model	DRAM IO model setting*1)
DQS, DQS#	lpddr4x_ocd_34p_34n_diff	ODT = 60ohm
DQ, DM	lpddr4x_ocd_34p_34n	ODT = 60ohm

Table 3-10 Recommended settings of SOC IBIS and DRAM IO model in DQ READ mode

Pin name	Recommended setting	
	SOC IBIS model	DRAM IO model setting*1)
DQS, DQS#	lpddr4x_odt_40_diff	VOH=VDDQ*0.5, SOC ODT = RZQ/6, PDDS = RZQ/6
DQ, DM	lpddr4x_odt_40	VOH=VDDQ*0.5, SOC ODT = RZQ/6, PDDS = RZQ/6

*1) ODT is the setting of on-die-termination of each signal bus receiver in Table 3-8, Table 3-9 and Table 3-10. Similarly, SOC ODT is the setting of controller ODT value for VOH calibration of DRAM.

3.2 Other signal lines

3.2.1 ZQ

Figure 3-8 and Figure 3-9 show a circuit diagram of external parts for ZQ on SOC and DRAM side. “p” is from 0 to 1 in these figures.

External resistance is connected between ZQ and GND on SOC side. Otherwise, that of DRAM is connected to VDDQ as specified in JEDEC standard. Please be careful of the difference between SOC and DRAM resistance connection of ZQ.

Noise to ZQ must be managed because ZQ is analog signal.

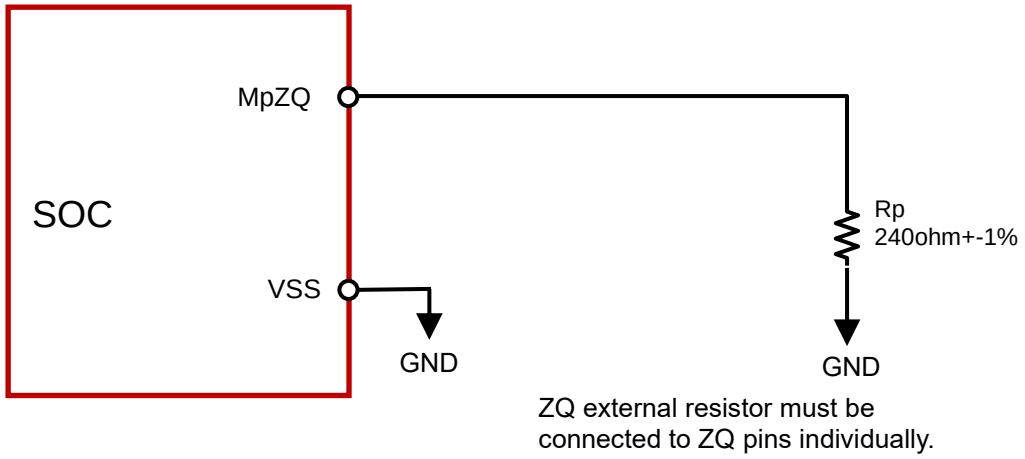


Figure 3-8 Circuit diagram of external parts for ZQ on SOC side

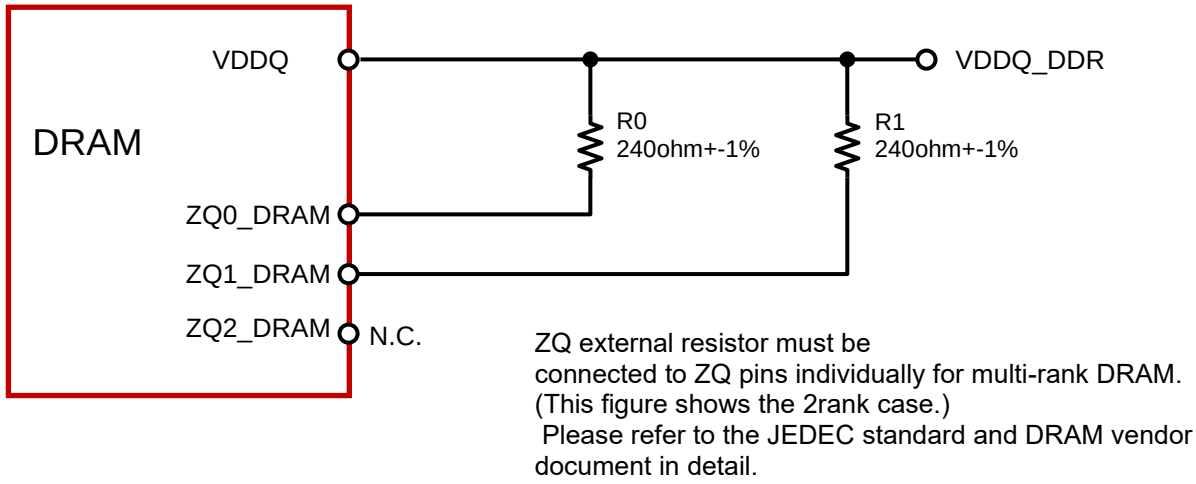


Figure 3-9 Circuit diagram of external parts for ZQ on DRAM side

3.3 Power supply configuration

3.3.1 IO power supply (VDDQVA_DDRp and VDDQX_DDRp)

Figure 3-10 shows a circuit diagram of IO power supply and external parts.

Power supply impedance of your PCB must be lower than target impedance for DDR IO power supply (VDDQVA_DDRp and VDDQX_DDRp). Please refer to section 5 about target impedance and verification method. Some of power domain in PCB can be merged, and it is also explained.

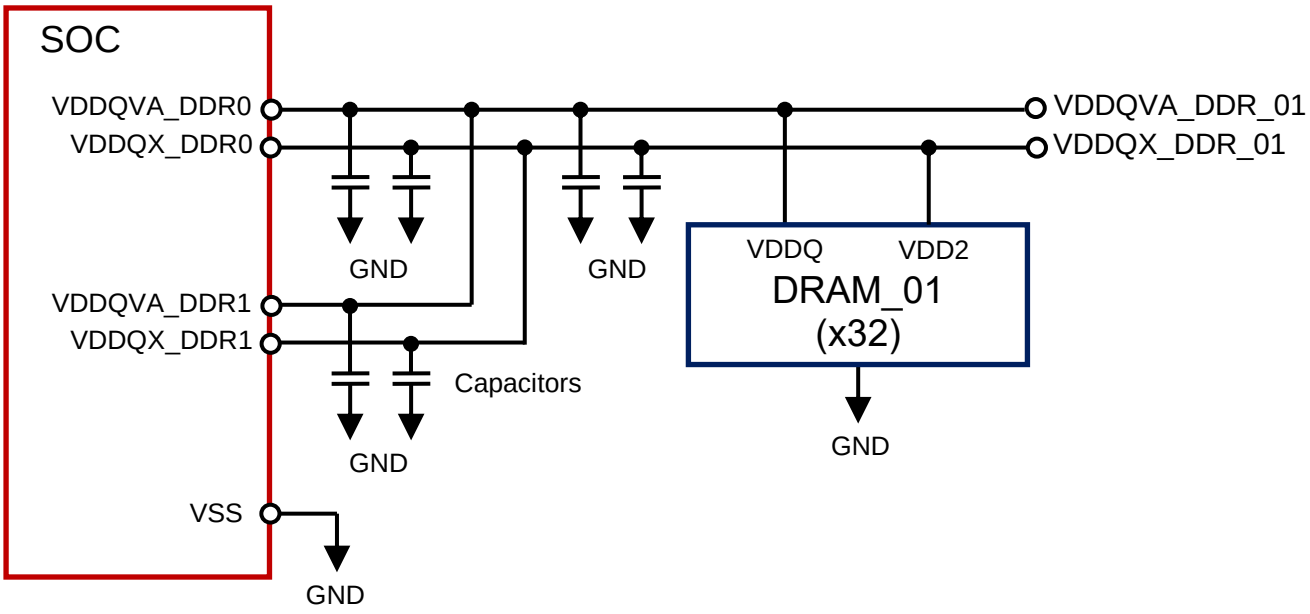


Figure 3-10 Circuit diagram of IO power supply and external parts

3.3.2 PLL power supply (VDD_DDRPLL01)

Figure 3-11 shows a circuit diagram image of PLL power supply (VDD_DDRPLL01) and external parts that compose a low pass filter. The external parts must be placed near SOC pin. Please refer to Figure 3-11 to determine Lp and Cp value. LC-filter is strongly recommended because PLL is very sensitive for power noise. Each PLL power supply group (VDD_DDRPLL01) consumes 46mA on maximum condition. The inductance Lp must be able to flow this maximum current, and DC drop caused by DC resistance of Lp must be less than or equal to 4.6mV (namely, DC resistance of Lp must be less than or equal to 100mohm max).

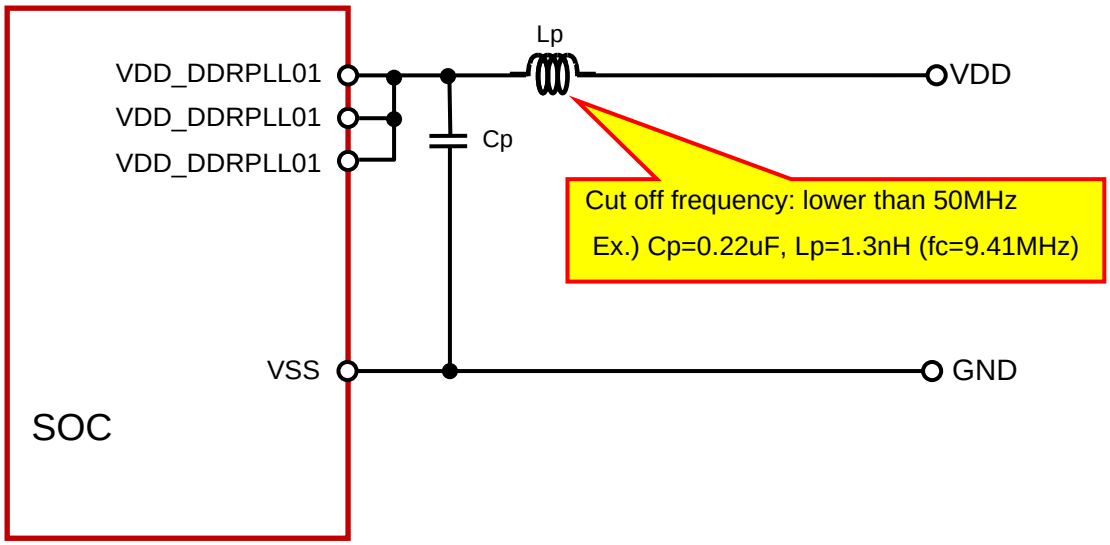


Figure 3-11 Circuit diagram of PLL power supply and external parts

4 Verification items and method of signal line

The verification of signal line includes skew, flight-time, timing, and waveform restrictions. Items and method of these restrictions are described in this section.

Simulation condition for skew restriction and flight-time restriction are only in typical condition whereas the others are simulated in typical and corner conditions.

4.1 Verification items

4.1.1 Skew restrictions

Table 4-1 shows skew restrictions. Measurement method of each restriction is described in section 4.2.1. Each item in Table 4-1 needs to be verified in accordance with section 4.2.1. These skew restrictions should be applied in the case using either LPDDR4 or LPDDR4X.

Table 4-1 Skew restrictions

Mode	Target signal group	Reference signal group	Skew restrictions value		note
			Min	Max	
Write	DQS/DQS#	CK/CK#	-1404ps	100ps	*1
Write	CK#	CK	-1ps	1ps	*1, *4
Write	CA	CK/CK#	-150ps	150ps	*1
Write	CAz / CS	CAw / CS	-	150ps	*1, *2
Write	CS	CK/CK#	-150ps	150ps	*1
Write	DQS#	DQS	-1ps	1ps	*1, *4
Write	DQ/DM	DQS/DQS#	-75ps	75ps	*1, *5
Write	DQx	DQy	-	150ps	*1, *3
Read	DQS#	DQS	-1ps	1ps	*1, *4
Read	DQ/DM	DQS/DQS#	-75ps	75ps	*1, *5
Read	DQx	DQy	-	150ps	*1, *3

*1: Skew restriction value do not include ISI and Xtalk jitter.
*2: This restriction is applied to the skew between two CAs and/or CSs in same channel of DRAM.
*3: Allowable delay variation within single byte group, i.e. maximum delay – minimum delay in a byte group. DM is included in these DQs.
*4: These restrictions are not mandatory but recommendation to design good differential signal. For example, about 3.5ps intra-pair skew might be allowable range. Please note that, of course, the other mandatory restrictions (VIX etc.) must be met.
*5: Allowable delay variation within single byte group.

4.1.1.1 Combination of measurement signals

Following tables show combination of measurement signals for skew restrictions. “p” is from 0 to 1 in these tables. In the tables, “x” and “y” mean from 0 to 15, and “z” and “w” mean from 0 to 5.

It is assumed that byte and bit swap functions are not used. If used, these combinations are modified based on SOC User’s Manual.

Table 4-2 Skew between DQS and CK (tDQSS)

Target signal	Reference signal
Mp_WCK[1:0]_T/Mp_WCK[1:0]_C	Mp_CK_T/Mp_CK_C

Table 4-3 Skew between CK and CK#

Target signal	Reference signal
Mp_CK_C	Mp_CK_T

Table 4-4 Skew between CA/CS and CK

Signal group	Target signal	Reference signal
CA	Mp_CA[6:2], p_CA0	Mp_CK_T/Mp_CK_C
CS	Mp_LP4XCS[1:0]	Mp_CK_T/Mp_CK_C

Table 4-5 Skew between CAz, CAw and CS

Target signal	Reference signal
Mp_CA[6:2], Mp_CA0 Mp_LP4XCS[1:0]	Mp_CA[6:2], Mp_CA0 Mp_LP4XCS[1:0]

Table 4-6 Skew between DQS and DQS# (Write/Read)

Target signal	Reference signal
Mp_WCK0_C	Mp_WCK0_T
Mp_WCK1_C	Mp_WCK1_T

Table 4-7 Skew between DQ/DM and DQS (Write/Read)

Target signal	Reference signal
Mp_DQ[7:0], Mp_DMI0	Mp_WCK0_T/Mp_WCK0_C
Mp_DQ[15:8], Mp_DMI1	Mp_WCK1_T/Mp_WCK1_C

Table 4-8 Skew between DQx and DQy (Write/Read)

Target signal	Reference signal
Mp_DQ[7:0], Mp_DMI0	Mp_DQ[7:0], Mp_DMI0
Mp_DQ[15:8], Mp_DMI1	Mp_DQ[15:8], Mp_DMI1

4.1.2 Flight-time restrictions

Table 4-9 shows flight-time restrictions. Measurement method of the restriction is described in section 4.2.2. The item in Table 4-9 needs to be verified in accordance with section 4.2.2. This restriction is necessary to keep through put of DDR-IF.

Table 4-9 Flight-time restriction

Restriction item	Restriction value	Unit
Flight-time	~ 1.0	ns

4.1.2.1 Combination of measurement signals

The following table shows combination of measurement signals for skew restrictions. “p” is from 0 to 1 in these tables.

Table 4-10 Flight-time

CK_delay	DQS_delay
Mp_CK_T/Mp_CK_C	Mp_WCK0_T/Mp_WCK0_C
	Mp_WCK1_T/Mp_WCK1_C

4.1.3 Timing restrictions

Table 4-11 shows timing restrictions based on SOC timing budget. Measurement method of each item is described in section 4.2.3. Each item in Table 4-11 needs to be verified in accordance with section 4.2.3.

Table 4-11 Timing restrictions

Category	Verification Item *1)	JEDEC Standard to be referred	JEDEC Spec. *2)		Timing Restriction		Unit
			Min	Max	Min	Max	
DQ	Write DQ eye (degradation)	tdIVW_total	-	58.5	-	88	ps
	Read DQ eye (degradation)	-	-	-	-	95	ps
	DQ input pulse width (At Vcent_DQ) (degradation)	tdIPW DQ	105.3	-	-	28	ps
DQS	DQS input low/high pulse width (degradation)	tDQSL/tDQSH	46.8	-	-12.0	12.0	ps
	Read DQS input low/high pulse width (degradation)	-	-	-	-12.0	12.0	ps
CA	CA eye (degradation)	tcIVW	-	140.4	-	217	ps
	CA input pulse width (degradation)	tcIPW	280.8	-	-	88.1	ps
CK	Average clock period *3)	tCK(avg)	0.468	100	-	-	ns
	Average High/Low pulse width (degradation)	tCH(avg)/tCL(avg)	-18.72	18.72	-5.0	5.0	ps
	Clock High/Low pulse width (degradation)	tCH(abs)/tCL(abs)	-32.76	32.76	-9.4	9.4	ps
	Clock period and cycle-cycle jitter *4)	tJIT(per)	-30	30	-9.4	9.4	ps
		tJIT(cc)	-	60	-	18.8	ps
	Jitter of DQS referred to CK rise edge	tDQSS	351	585	-9.5	9.5	ps

*1) Please note that some of these names do not correspond to JEDEC standard because these are calculated as degradation of corresponding spec.
*2) These values are JEDEC standard of LPDDR4X-4267 for corresponding timing restriction.
*3) This item shows the input data, trigger and clock period. Signaling rate in the verifications show in this table should be matched with actual data rate in your system.
*4) The restriction for tCK(abs) isn't specified in this table because tCK(abs) is calculated from tCK(avg)MIN and tJIT(per)MIN as described in JEDEC standard.

4.1.4 Waveform restrictions

Table 4-12 shows waveform restrictions. Measurement method of these items are described in JEDEC standard. Each item in Table 4-12 needs to be verified in accordance with JEDEC standard. Only those of Rx Mask voltage p-p (for DQ and CA) is described in section 4.2.4.

Table 4-12 Waveform restrictions

Category	Verification Item	JEDEC Standard to be referred	JEDEC Spec.		Waveform Restriction		Unit
			Min	Max	Min	Max	
WRITE DQ	DQ AC input pulse amplitude pk-pk	VIHL_AC	170	-	190	-	mV
	Rx Mask voltage p-p total	VdIVW_total	-	120	140	-	mV
	Input Slew Rate over VdIVW_total	SRIN_dIVW	1	7	1.4	6.6	V/ns
WRITE DQS	DQS Differential input crosspoint voltage ratio	Vix_DQS_ratio	-	20	-	12	%
	DQS differential input	Vindiff_DQS	340	-	390	-	mV
	DQS Single-Ended input voltage High from VrefDQ	Vinse_DQS_High	85	-	102	-	mV
	DQS Single-Ended input voltage Low from VrefDQ	Vinse_DQS_Low	85	-	102	-	mV
	Different Input Slew Rate	SRIdiff	2	14	3.7	12.3	V/ns
READ DQ	DQ AC input pulse amplitude pk-pk	VIHL_AC	-	-	190	-	mV
	Rx Mask voltage p-p total	VdIVW_total	-	-	140	-	mV
	Input Slew Rate over VdIVW_total	SRIN_dIVW	-	-	1.4	6.4	V/ns
READ DQS	DQS Differential input crosspoint voltage ratio	Vix_DQS_ratio	-	-	-	12	%
	DQS differential input	Vindiff_DQS	-	-	360	-	mV
	DQS Single-Ended input voltage High from VrefDQ	Vinse_DQS_High	-	-	102	-	mV

Table 4-12 Waveform restrictions (Continued)

Category	Verification Item	JEDEC Standard to be referred	JEDEC Spec.		Waveform Restriction		Unit
			Min	Max	Min	Max	
READ DQS	DQS Single-Ended input voltage Low from VrefDQ	Vinse_DQS_Low	-	-	102	-	mV
	Different Input Slew Rate	SRIdiff	-	-	3.7	12.3	V/ns
CA	CA AC input pulse amplitude pk-pk	VIHL_AC	180	-	210	-	mV
	Rx Mask voltage p-p	VcIVW	-	145	170	-	mV
	Input Slew Rate over VcIVW	SRIN_cIVW	1	7	1.4	6.7	V/ns
CK	CK Differential input crosspoint voltage ratio	Vix_CK_ratio	-	25	-	11	%
	CK differential input voltage	Vindiff_CK	360	-	520	-	mV
	CK Single-Ended input voltage High from VrefCA	Vinse_CK_High	90	-	153	-	mV
	CK Single-Ended input voltage Low from VrefCA	Vinse_CK_Low	90	-	153	-	mV
	Different Input Slew Rate	SRIdiff	2	14	3.0	12.4	V/ns
LVSTL Signal Common	Maximum peak amplitude allowed for overshoot area	Maximum peak amplitude for overshoot area	-	0.3	-	0.26	V
	Maximum peak amplitude allowed for undershoot area	Maximum peak amplitude for undershoot area	-	0.3	-	0.26	V
	Maximum overshoot area above VDD/VDDQ	Maximum overshoot area above VDD/VDDQ	-	0.1	-	0.087	V-ns
	Maximum undershoot area below VSS/VSSQ	Maximum undershoot area below VSS/VSSQ	-	0.1	-	0.087	V-ns

Table 4-12 Waveform restrictions (Continued)

Category	Verification Item	JEDEC Standard to be referred	JEDEC Spec.		Waveform Restriction		Unit
			Min	Max	Min	Max	
LVCMOS Signal Common	Input high level (AC)	VIH(AC)	0.75* VDDQ	VDDQ +0.2	0.75* VDDQ	VDDQ +0.2	V
	Input low level (AC)	VIL(AC)	-0.2	0.25 *VDDQ	-0.2	0.25 *VDDQ	V
	Input high level (DC)	VIH(DC)	0.65* VDDQ	VDDQ +0.2	0.65* VDDQ	VDDQ +0.2	V
	Input low level (DC)	VIL(DC)	-0.2	0.35 *VDDQ	-0.2	0.35 *VDDQ	V
LVCMOS Signal Common	Maximum peak Amplitude allowed for overshoot area	Maximum peak Amplitude allowed for overshoot area	-	0.35	-	0.35	V
	Maximum peak Amplitude allowed for undershoot area	Maximum peak Amplitude allowed for undershoot area	-	0.35	-	0.35	V
	Maximum overshoot area above VDD/VDDQ	Maximum overshoot area above VDD/VDDQ	-	0.8	-	0.8	V-ns
	Maximum undershoot area below VSS/VSSQ	Maximum undershoot area below VSS/VSSQ	-	0.8	-	0.8	V-ns

4.2 Verification method

4.2.1 Skew restrictions

Skew restrictions shown in Table 4-1 are confirmed at DRAM PAD and SOC PAD. Delay from SOC PAD to DRAM PAD must be confirmed to satisfy skew restrictions described in Figure 4-1, which compensate the skew of PKG by adjusting PCB delay.

In verifying skew between differential and single-ended signal, it is necessary to remove IO buffer delay (named “basic delay”) to measure only interconnect skew.

Measurement method of basic delay is shown in Figure 4-2 and Figure 4-3.

Skew factors are assumed the following three items as described in section 1.4.

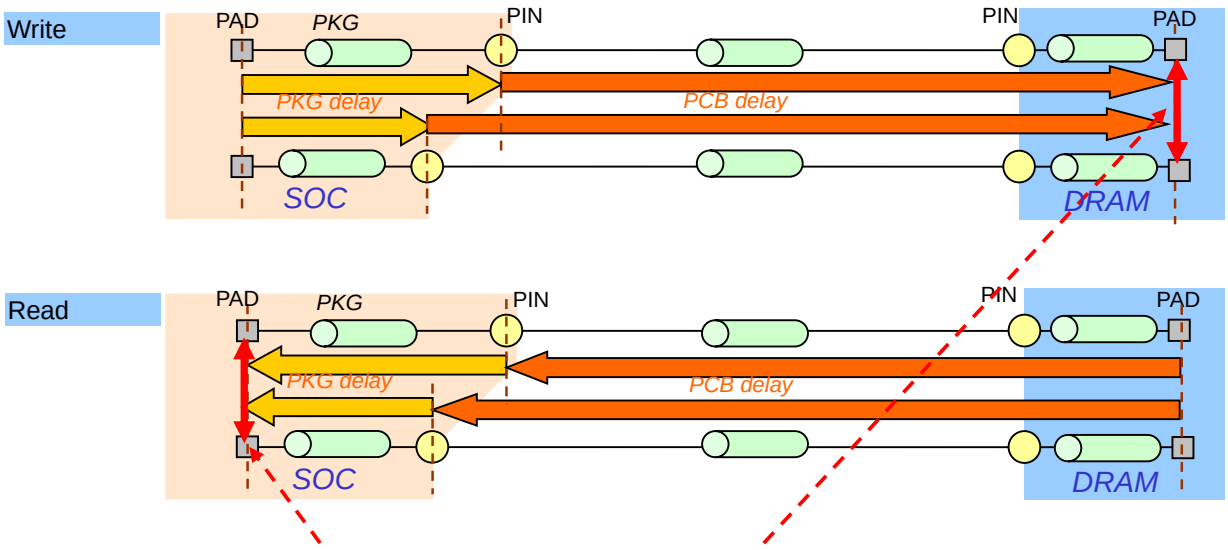
(1). Path mismatch

Delay time deviation caused by the SOC PKG and PCB trace length difference among signals.

(2). Inter-Symbol Interference (ISI)

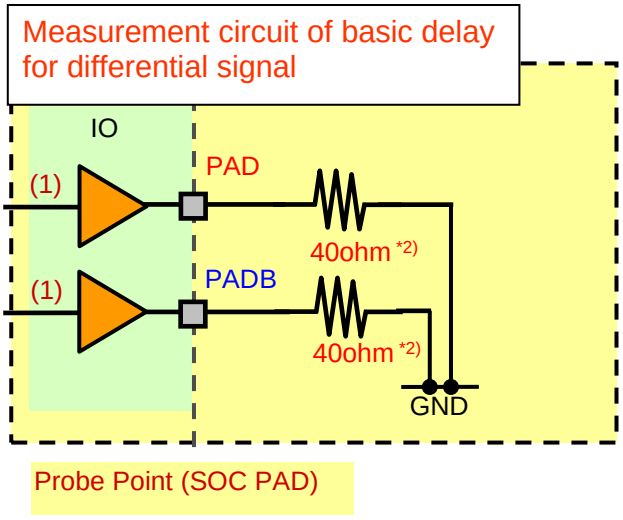
(3). Xtalk jitter

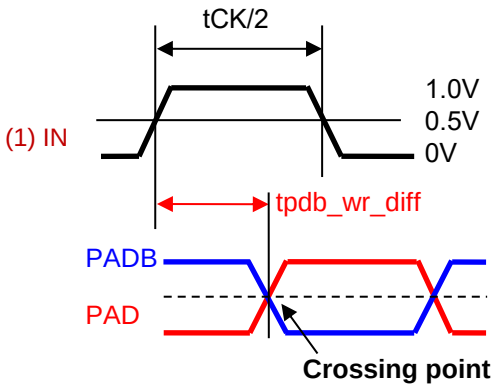
Table 4-1 shows restrictions for (1) path mismatch. PCB design should be verified by using data pattern which causes no ISI and no Xtalk jitter. (2) and (3) are verified in timing restriction by using data pattern with ISI and Xtalk (refer to section 4.2.3). To eliminate the influence of ISI to the result of skew simulation, DQ/CA data frequency should be slow, for example 100MHz (10ns). On the other hand, the frequency for CK and DQS should be real operating frequency, for example the operating frequency 2.133GHz (468ps).

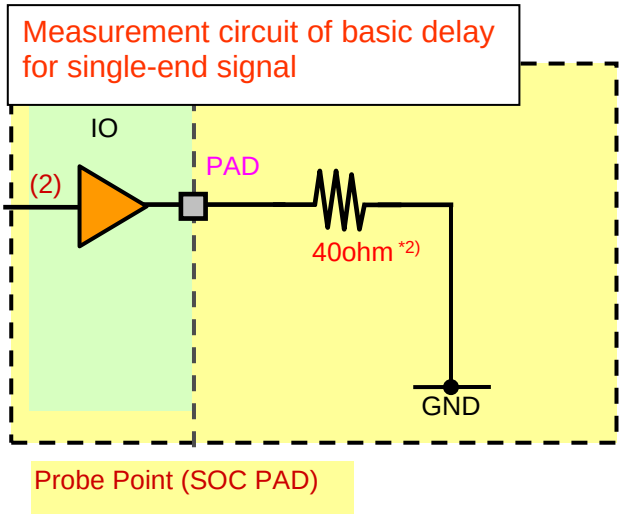


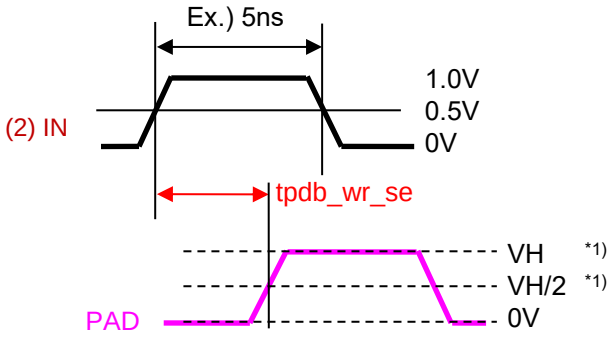
It should be confirmed that path mismatch is less than restrictions at DRAM PAD and SOC PAD.

Figure 4-1 How to adjust path mismatch





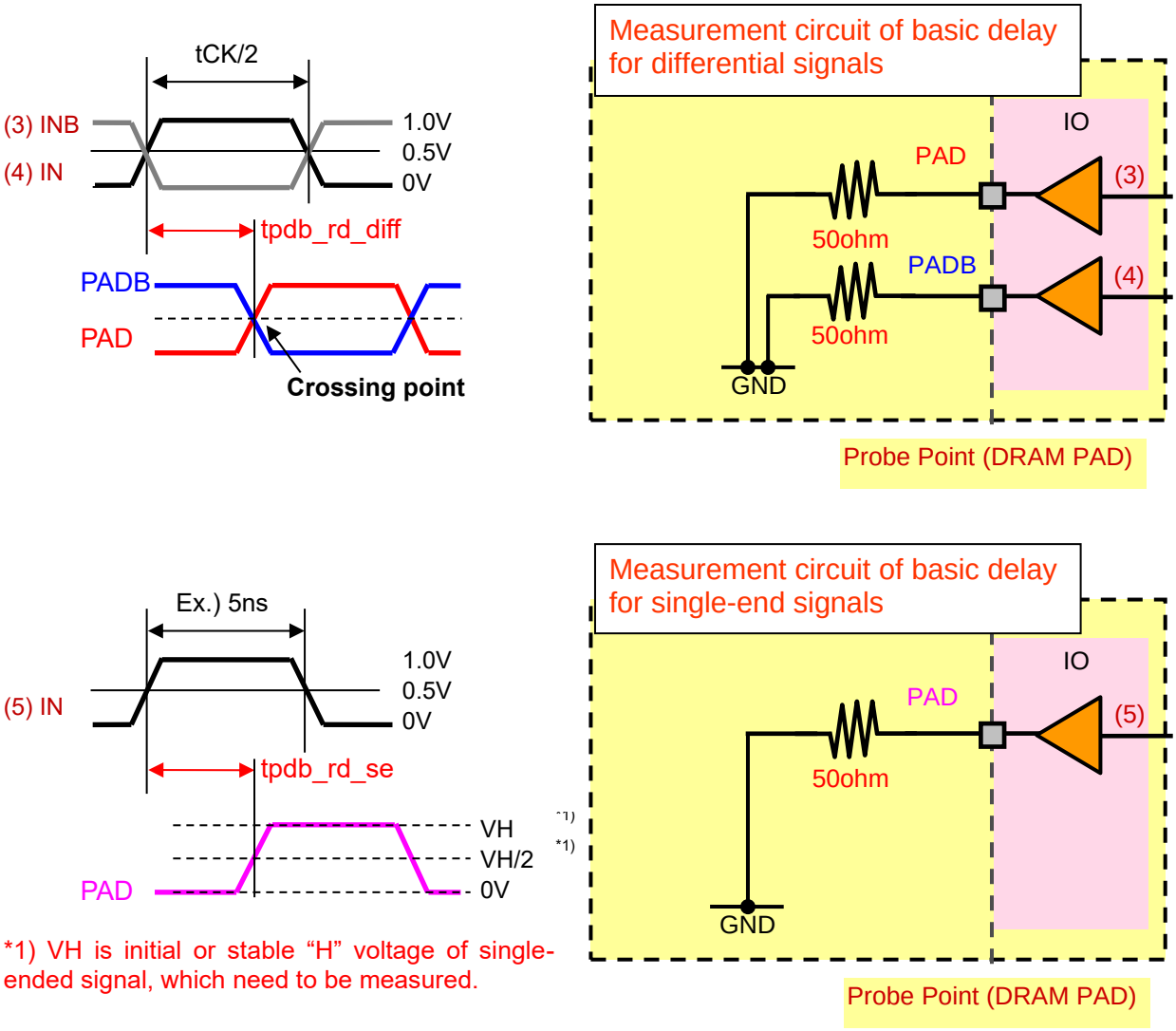




*1) VH is initial or stable “H” voltage of single-ended signal, which need to be measured.

*2) The termination resistance value should be set to the one of each signal group setting in this basic delay simulation of IBIS model.

Figure 4-2 Measurement method of basic delay (Write)

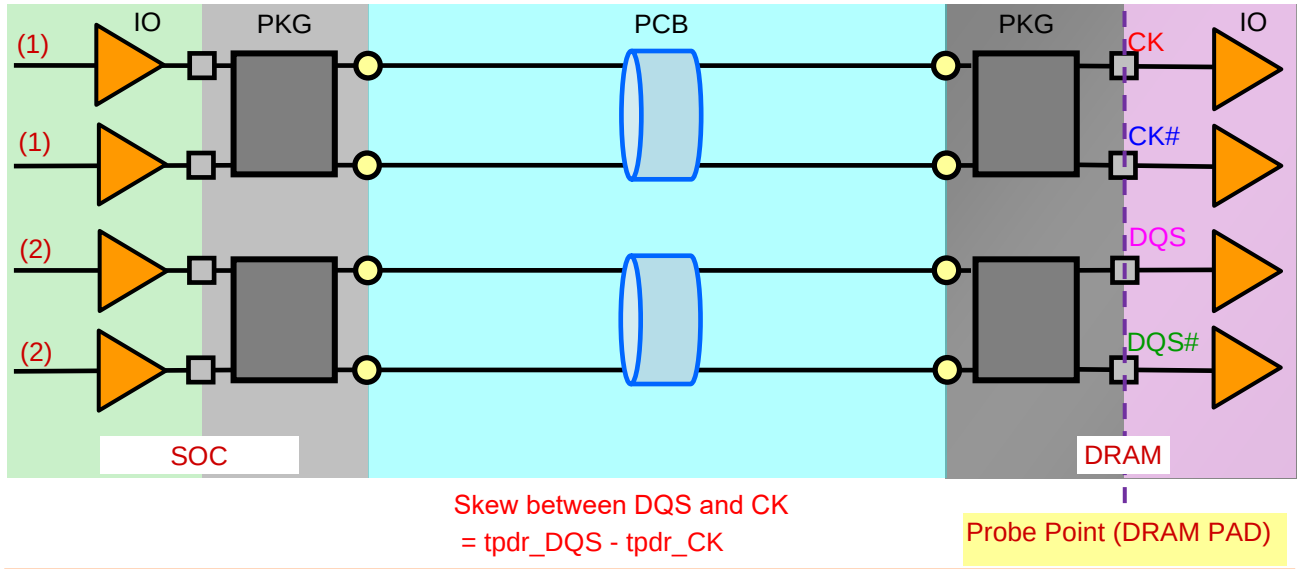


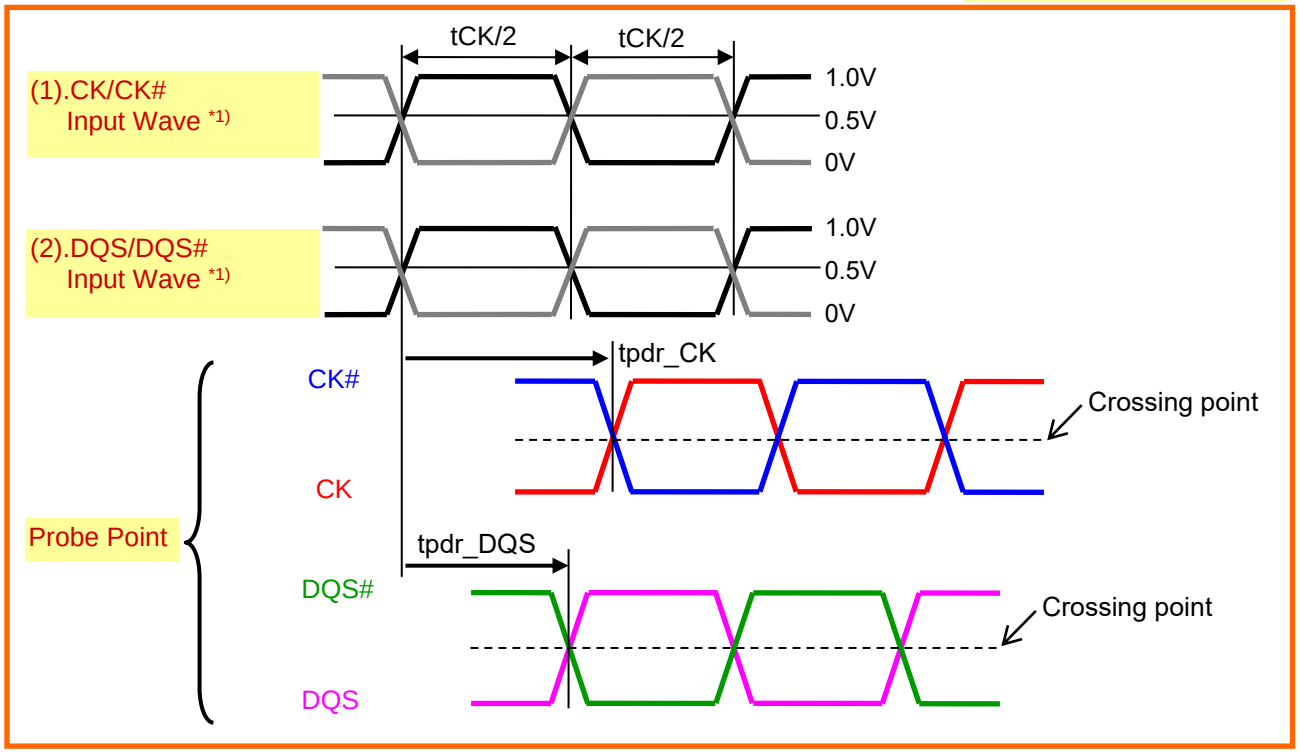
*1) VH is initial or stable “H” voltage of single-ended signal, which need to be measured.

Figure 4-3 Measurement method of basic delay (Read)

4.2.1.1 Skew between DQS and CK (tDQSS)

Figure 4-4 shows the measurement circuit, input waveform to SOC IO buffer model, and measured waveform at DRAM PAD. Skew between DQS and CK should be smaller than the target specification shown in Table 4-1.



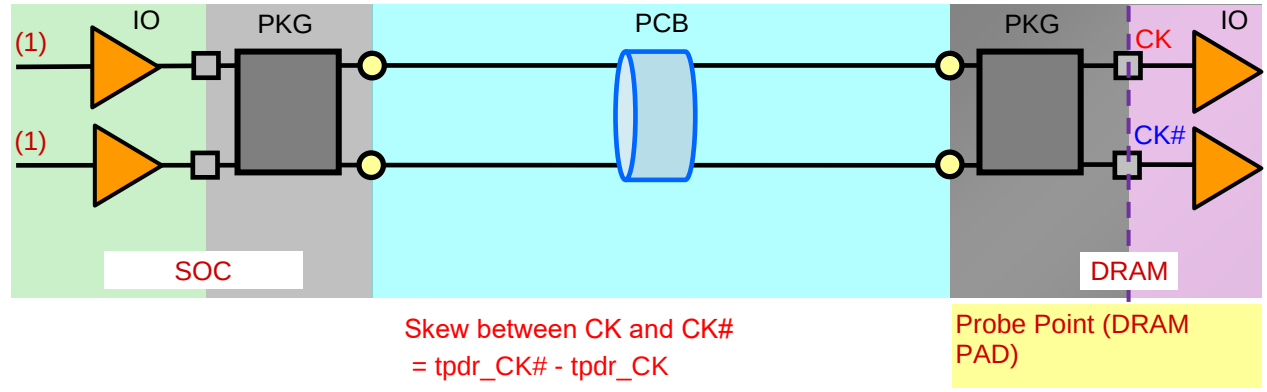


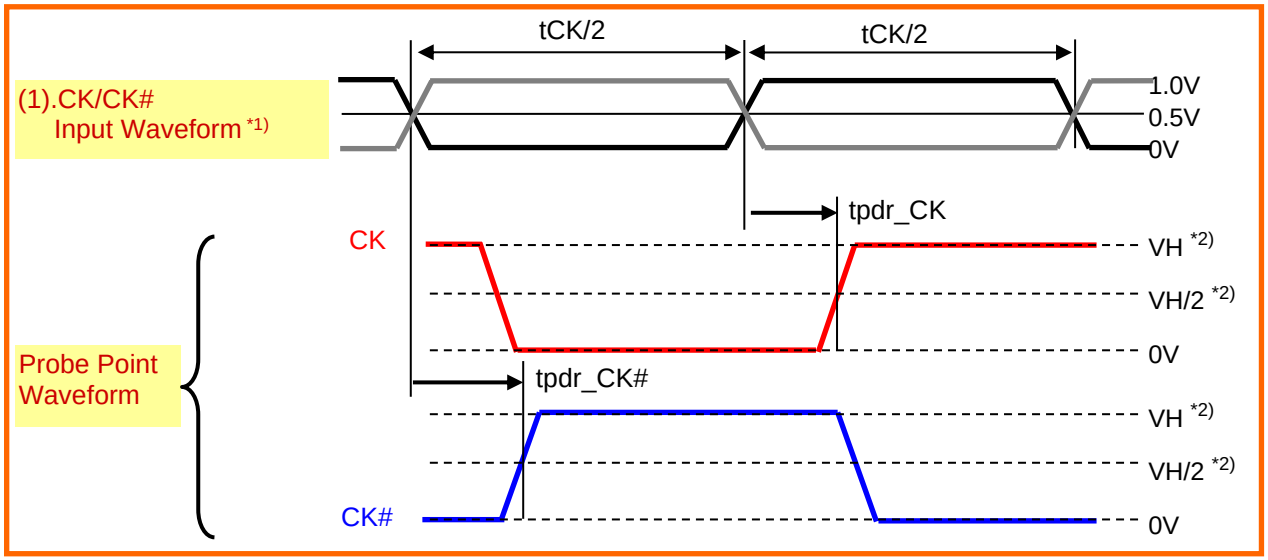
*1) Input wave form of complementary side (# side) is same as true one because of the polarity of the IBIS model.

Figure 4-4 Measurement method of skew between DQS and CK

4.2.1.2 Skew between CK and CK#

Figure 4-5 shows the measurement circuit, input waveform to SOC IO buffer model, and measured waveform at DRAM PAD. Skew between CK and CK# should be smaller than the target specification shown in Table 4-1.



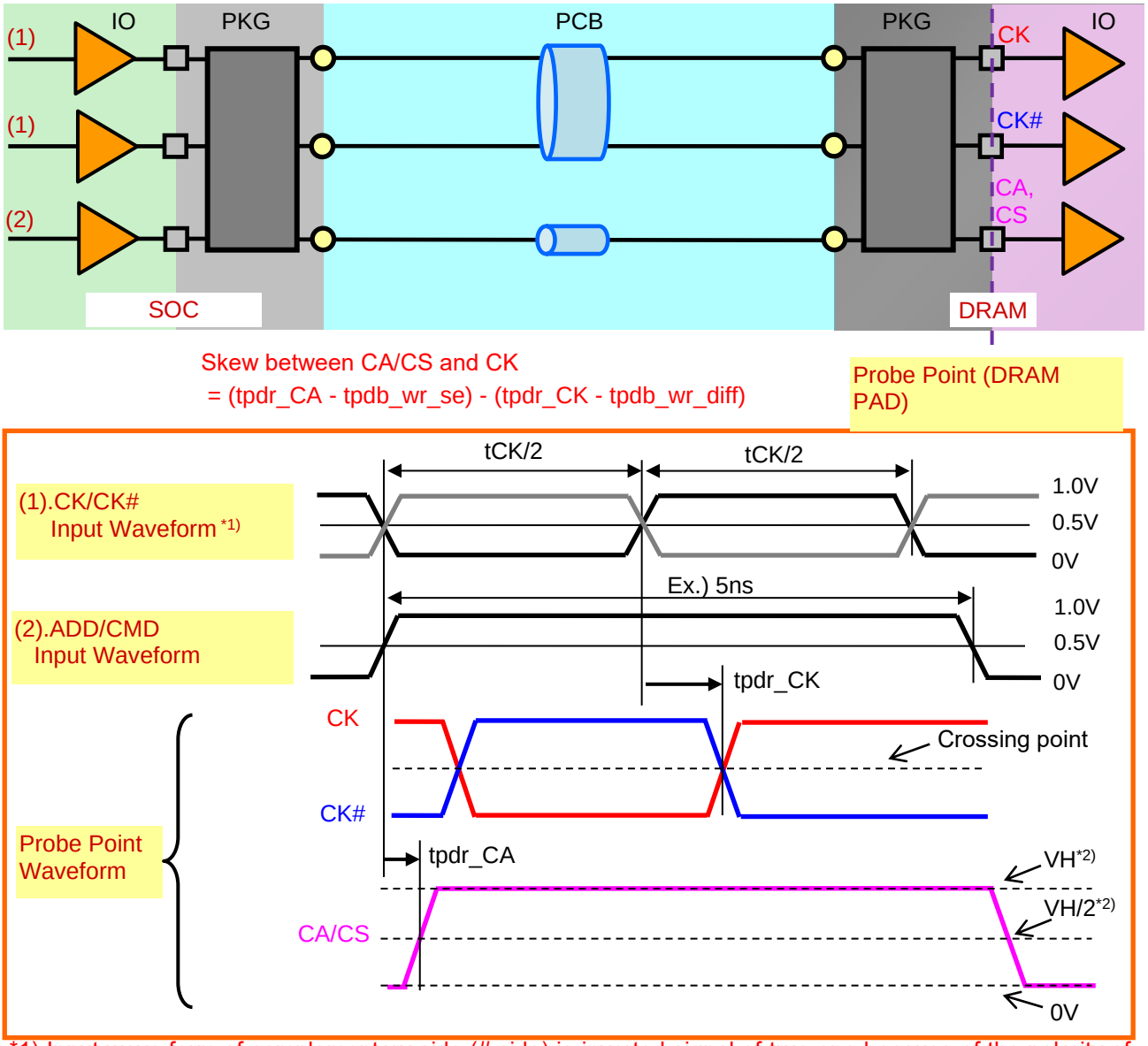


*1) Input wave form of complementary side (# side) is inverted signal of true one because of the polarity of the IBIS model.
*2) VH is initial voltage of CK or CK#, which need to be measured.

Figure 4-5 Measurement method of skew between CK and CK#

4.2.1.3 Skew between CA/CS and CK

Figure 4-6 shows the measurement circuit, input waveform to SOC IO model, and measured waveform at DRAM PAD. Skew between CA/CS and CK should be smaller than the target specification shown in Table 4-1.

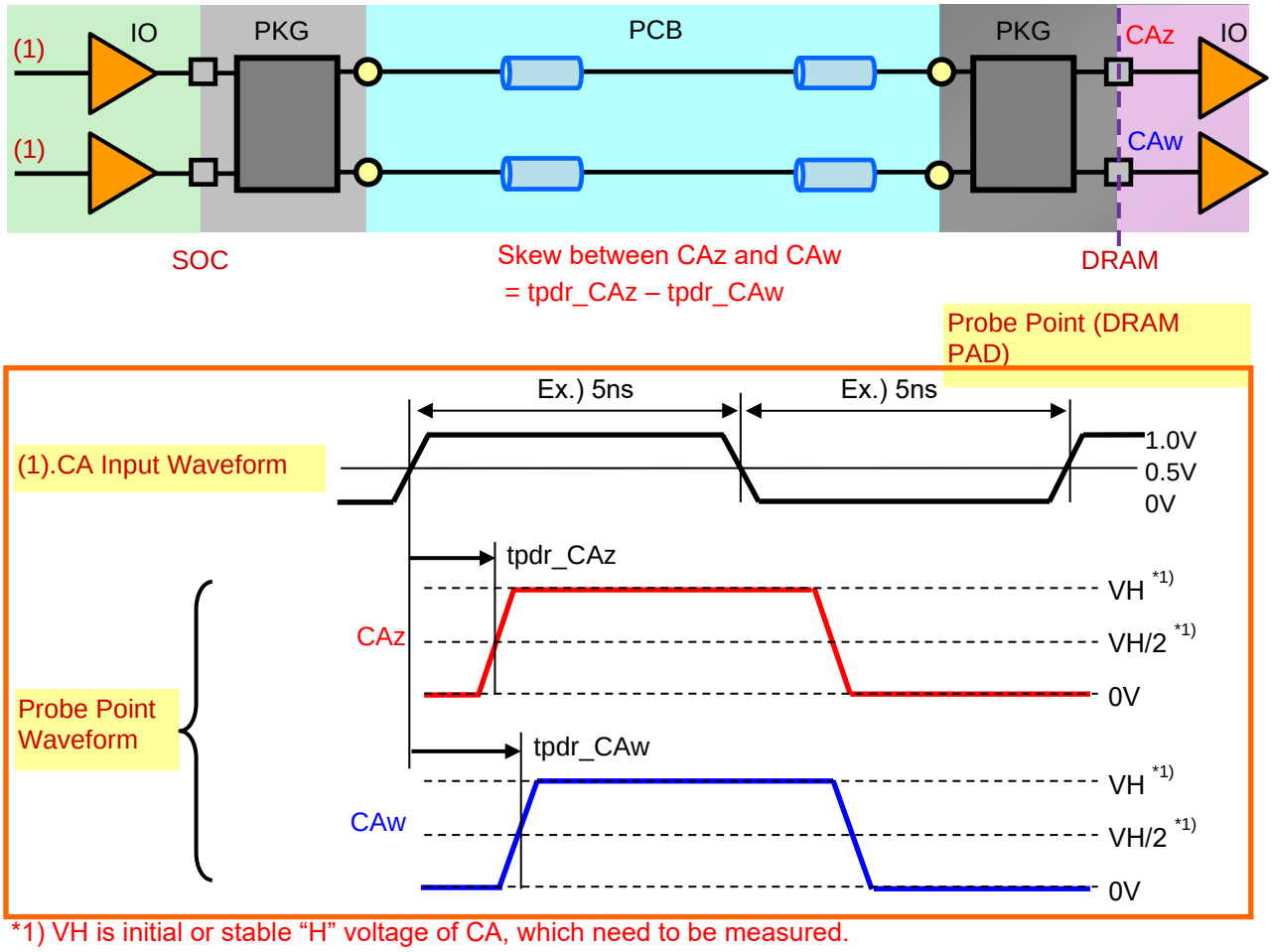


*1) Input wave form of complementary side (# side) is inverted signal of true one because of the polarity of the IBIS model.
*2) VH is initial or stable “H” voltage of CA, which need to be measured.

Figure 4-6 Measurement method of skew between CA/CS and CK

4.2.1.4 Skew between CAz and CAw

Figure 4-7 shows the measurement circuit, input waveform to SOC IO buffer model, and measured waveform at DRAM PAD. Skew between CAz and CAw should be smaller than the target specification shown in Table 4-1. CAz and CAw are the combination of each two CA signals which are connected to same DRAM channel and same DRAM rank. “Z” and “w” mean from 0 to 5 and “z” is not equal to “w”.



*1) VH is initial or stable “H” voltage of CA, which need to be measured.

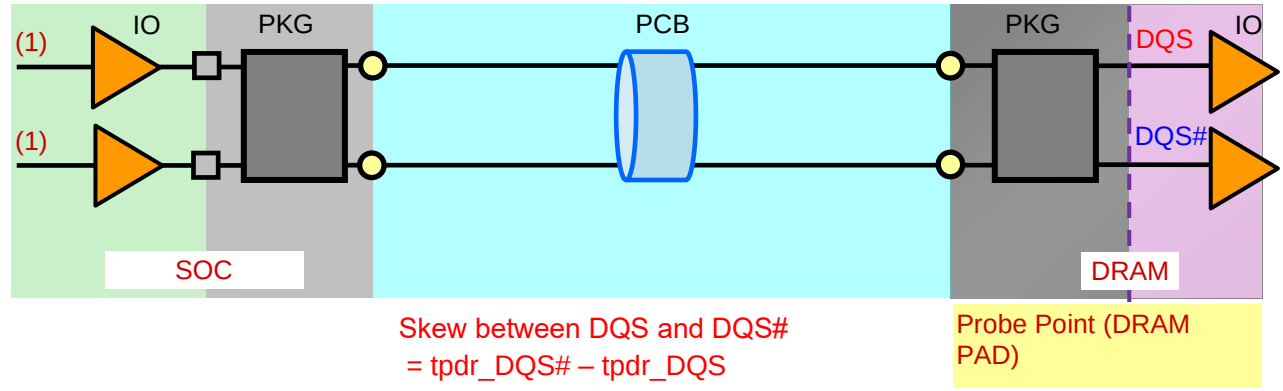
Figure 4-7 Measurement method of skew between CAz and CAw

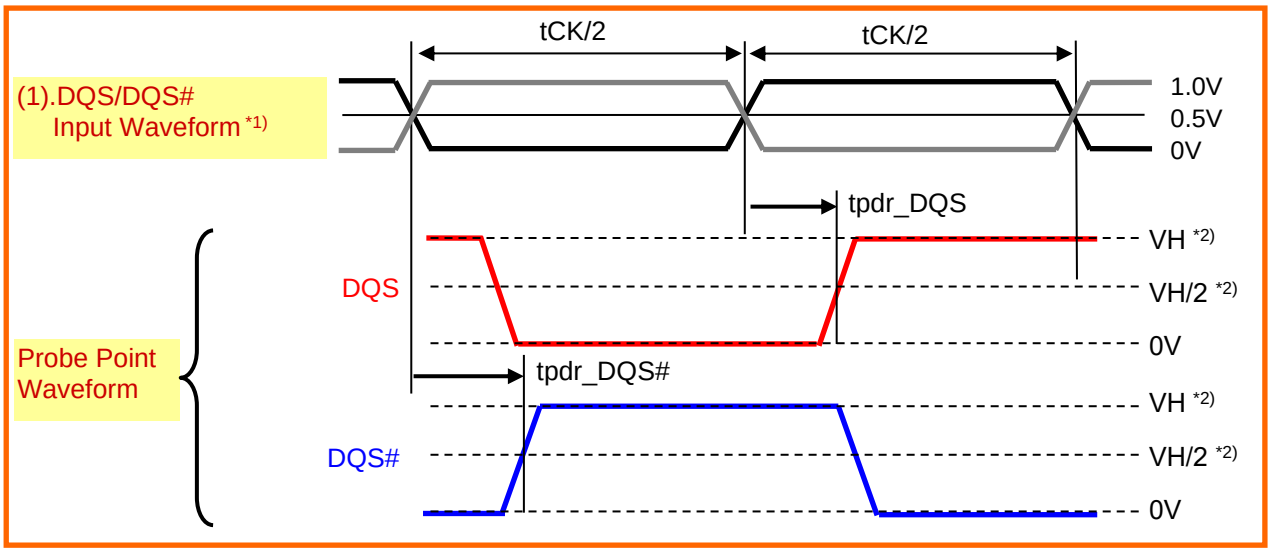
4.2.1.5 Skew between CKE and CK

No restriction because JEDEC has no tight timing restriction for CKE and CK.

4.2.1.6 Skew between DQS and DQS# (Write)

Figure 4-8 shows the measurement circuit, input waveform to SOC IO buffer model, and measured waveform at DRAM PAD in write mode. Skew between DQS and DQS# in write mode should be smaller than the target specification shown in Table 4-1.



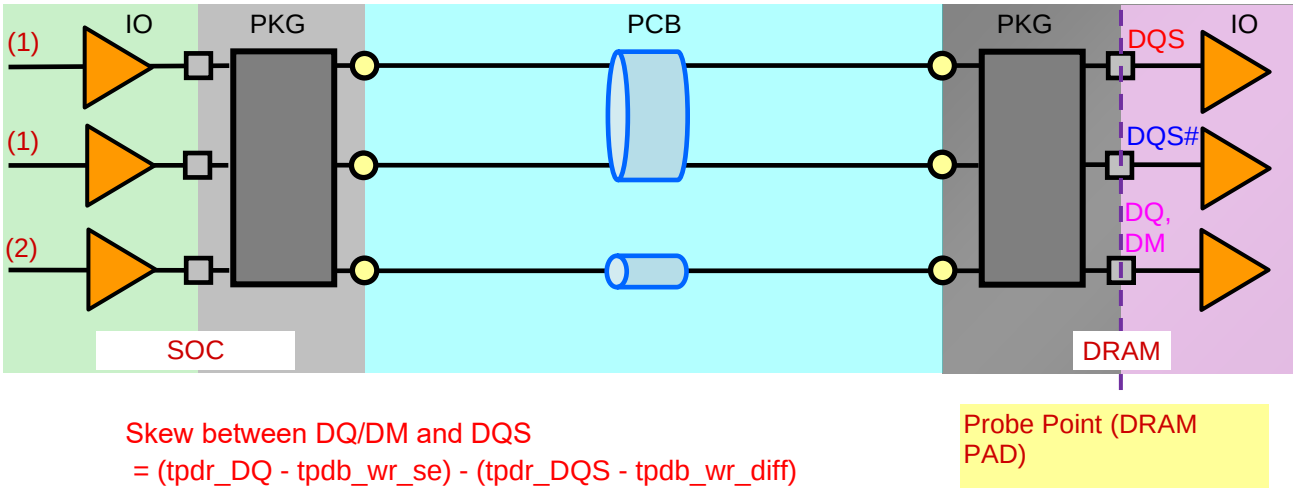


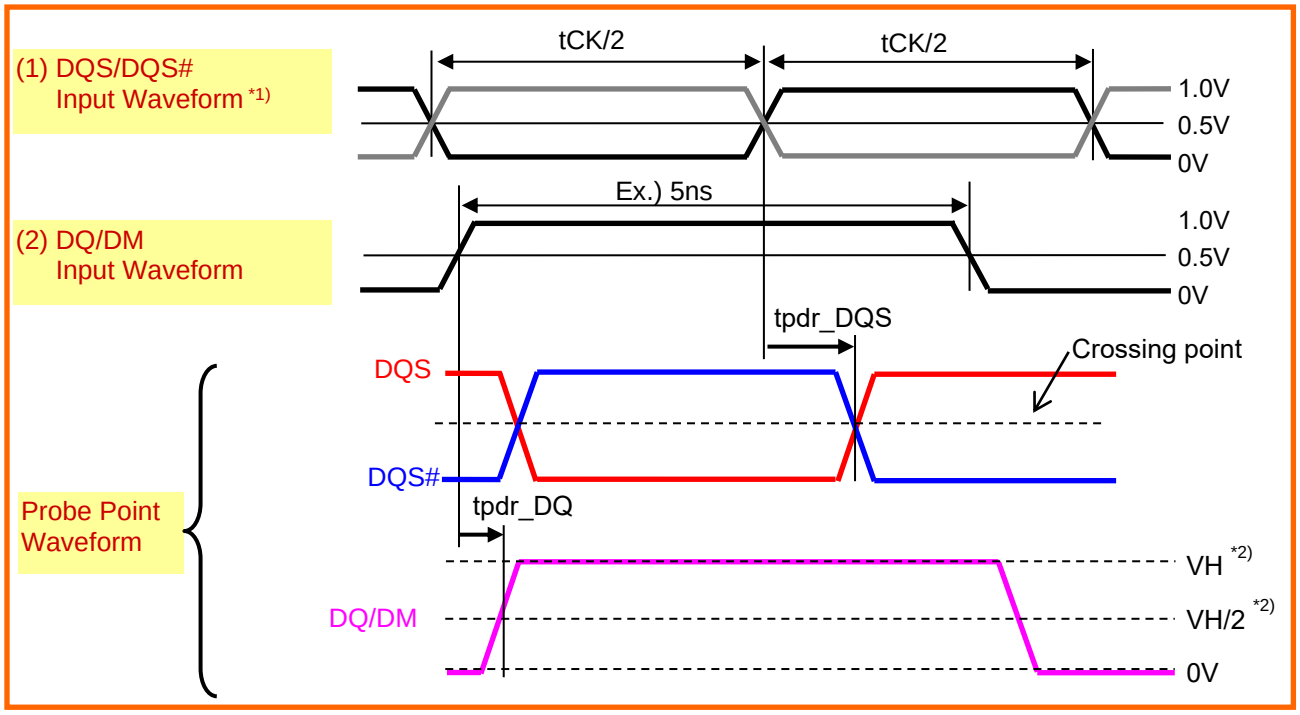
*1) Input wave form of complementary side (# side) is inverted signal of true one because of the polarity of the IBIS model.
*2) VH is initial voltage of DQS or DQS#, which need to be measured.

Figure 4-8 Measurement method of skew between DQS and DQS# (Write)

4.2.1.7 Skew between DQ/DM and DQS (Write)

Figure 4-9 shows the measurement circuit, input waveform to SOC IO model, and measured waveform at DRAM PAD in write mode. Skew between DQ/DM and DQS in write mode should be smaller than the target specification shown in Table 4-1.



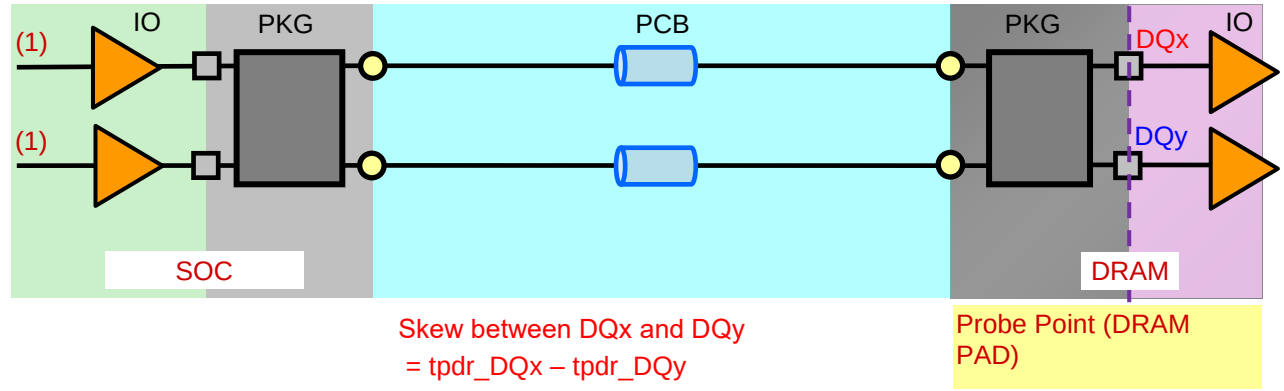


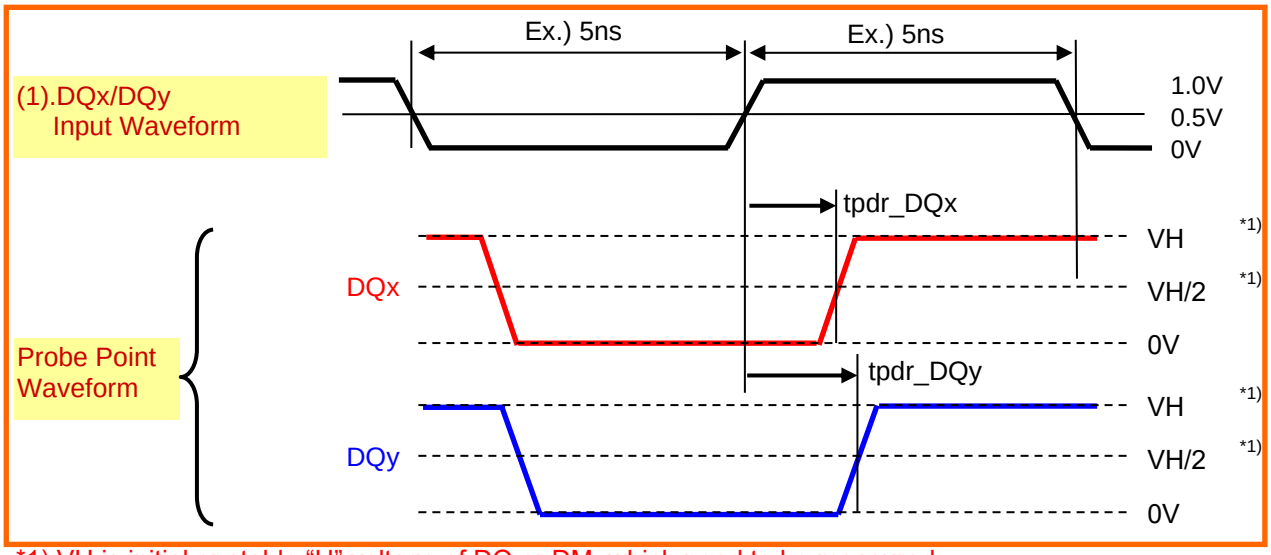
*1) Input wave form of complementary side (# side) is inverted signal of true one because of the polarity of the IBIS model.
*2) VH is initial or stable “H” voltage of DQ or DM, which need to be measured.

Figure 4-9 Measurement method of skew between DQ/DM and DQS (Write)

4.2.1.8 Skew between DQx and DQy (Write)

Figure 4-10 shows the measurement circuit, input waveform to SOC IO model and measured waveform at DRAM PAD in write mode. Skew between DQx and DQy in write mode should be smaller than the target specification shown in Table 4-1.



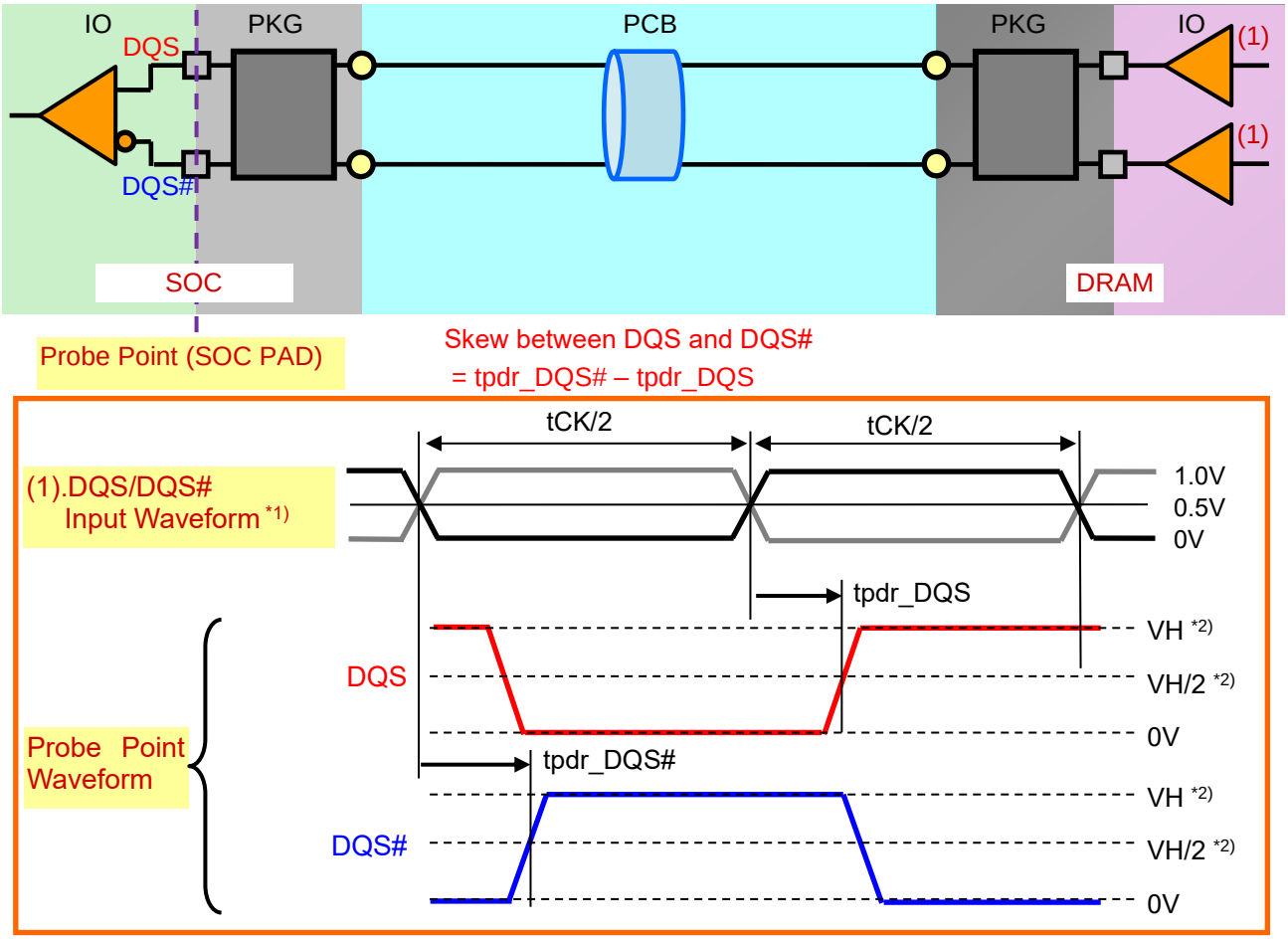


*1) VH is initial or stable “H” voltage of DQ or DM, which need to be measured.

Figure 4-10 Measurement method of skew between DQx and DQy (Write)

4.2.1.9 Skew between DQS and DQS# (Read)

Figure 4-11 shows the measurement circuit, input waveform to DRAM IO model, and measured waveform at SOC PAD in read mode. Skew between DQS and DQS# in read mode should be smaller than the target specification shown in Table 4-1.

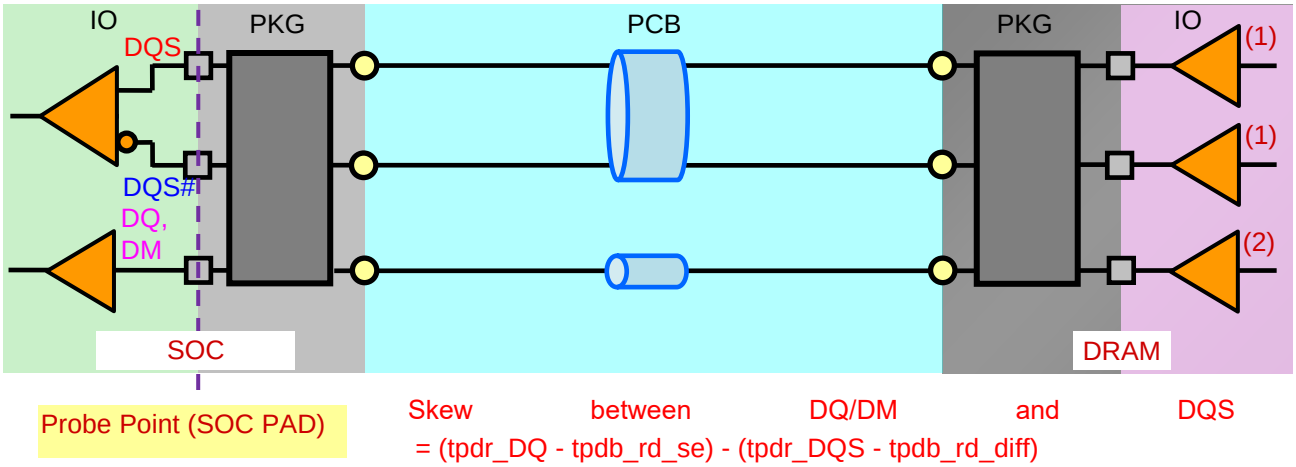


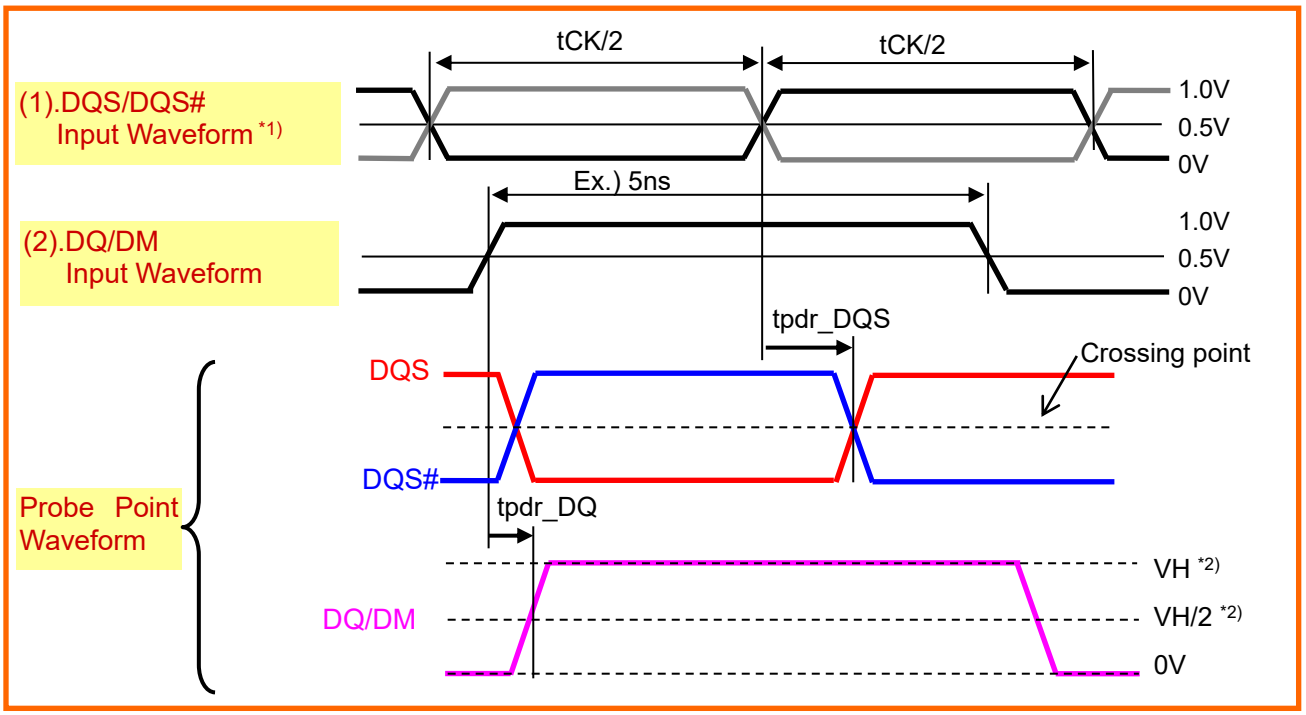
*1) Input wave form of complementary side (# side) is inverted signal of true one because of the polarity of the IBIS model.
*2) VH is initial voltage of DQS or DQS#, which need to be measured.

Figure 4-11 Measurement method of skew between DQS and DQS# (Read)

4.2.1.10 Skew between DQ/DM and DQS (Read)

Figure 4-12 shows the measurement circuit, input waveform of DRAM IO model and measured waveform at SOC PAD in read mode. Skew between DQ/DM and DQS in read mode should be smaller than the target specification shown in Table 4-1.



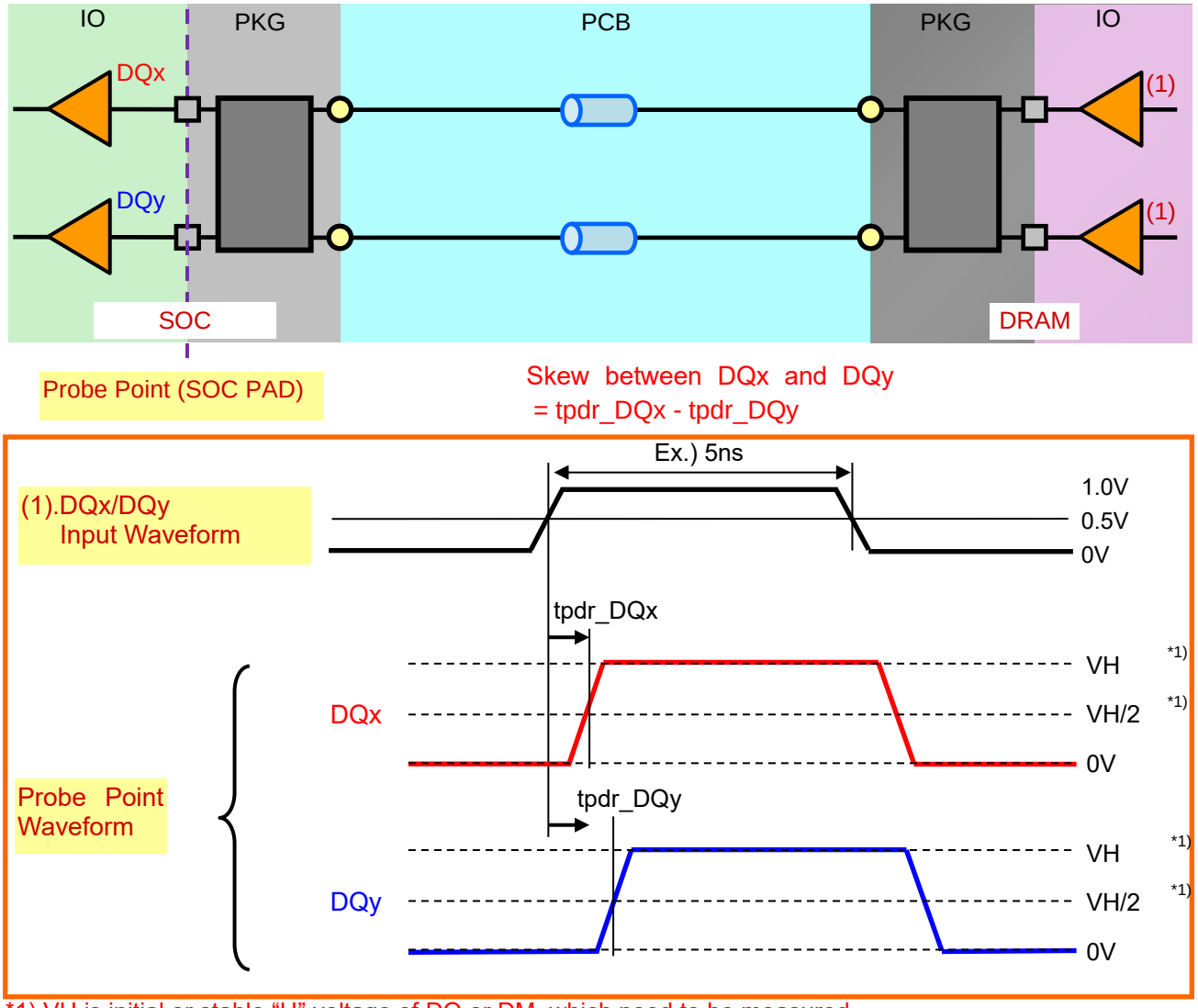


*1) Input wave form of complementary side (# side) is inverted signal of true one because of the polarity of the IBIS model.
*2) VH is initial or stable “H” voltage of DQ or DM, which need to be measured.

Figure 4-12 Measurement method of skew between DQ/DM and DQS (Read)

4.2.1.11 Skew between DQx and DQy (Read)

Figure 4-13 shows the measurement circuit, input waveform of DRAM IO model and measured waveform at SOC PAD in read mode. Skew between DQx and DQy in read mode should be smaller than the target specification shown in Table 4-1.



*1) VH is initial or stable “H” voltage of DQ or DM, which need to be measured.

Figure 4-13 Measurement method of skew between DQx and DQy (Read)

4.2.2 Flight-time restrictions

Flight-time is defined as sum of a) CK delay from SOC PAD to DRAM PIN (CK_delay) and b) DQS delay from DRAM pin to SOC PAD (DQS_delay), shown in below equation.

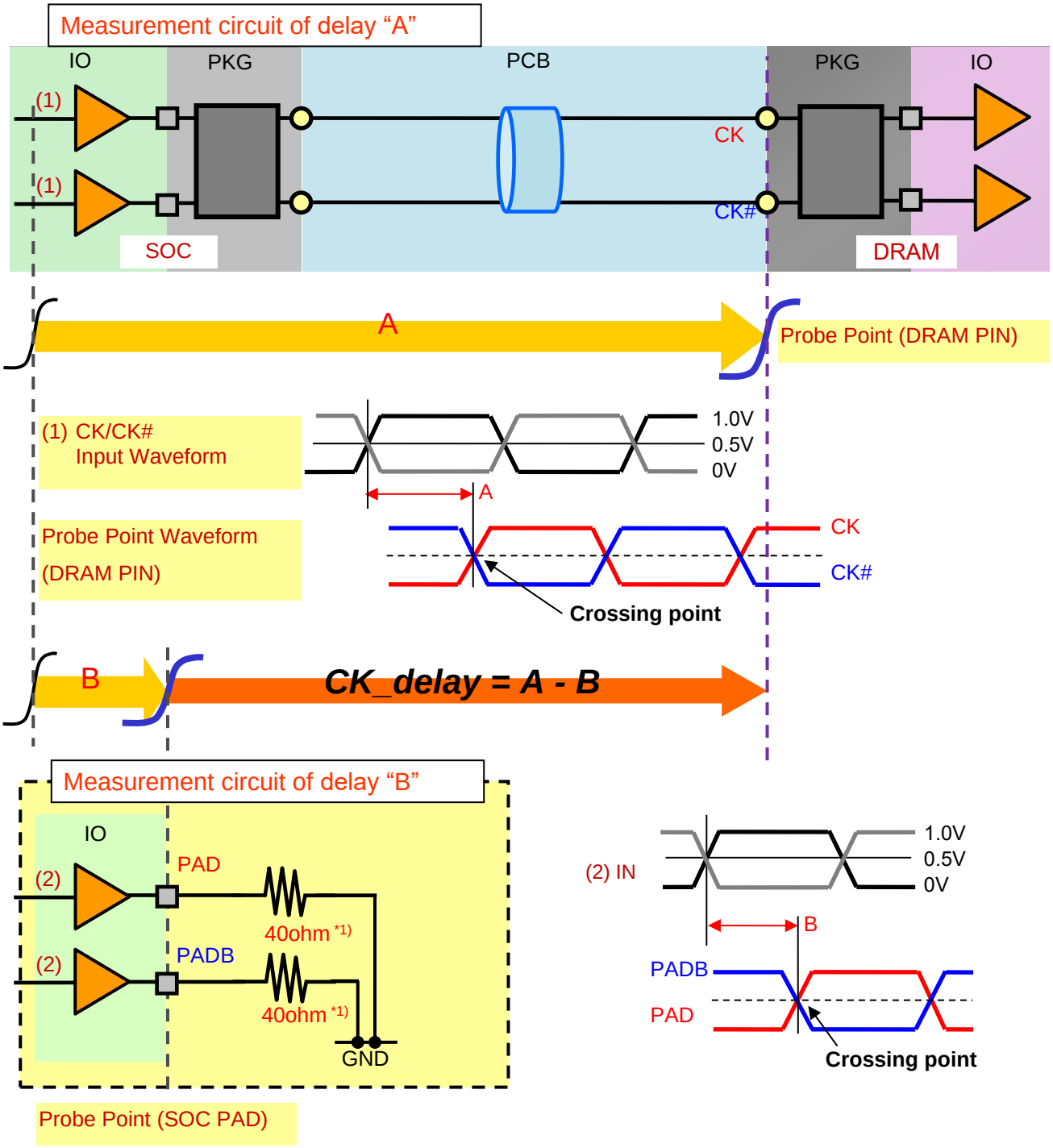
Flight-time = CK_delay + DQS_delay

4.2.2.1 Flight-time

Figure 4-14 and Figure 4-15 show measurement method of CK and DQS delay which compose the flight-time.

(1) Measurement method of CK_delay

Both delay “A” from PHY input to DRAM PIN and SOC IO delay “B” are measured in accordance with Figure 4-14. Then, CK_delay = A - B.



*1) The termination resistance value should be set to the one of each signal group setting in this basic delay simulation of IBIS model.

Figure 4-14 Measurement method of CK_delay

(2) Measurement method of DQS_delay

Both delay “C” from DRAM PIN to SOC PAD and DRAM delay “D” are measured in accordance with Figure 4-15. Then, DQS_delay = C - D.

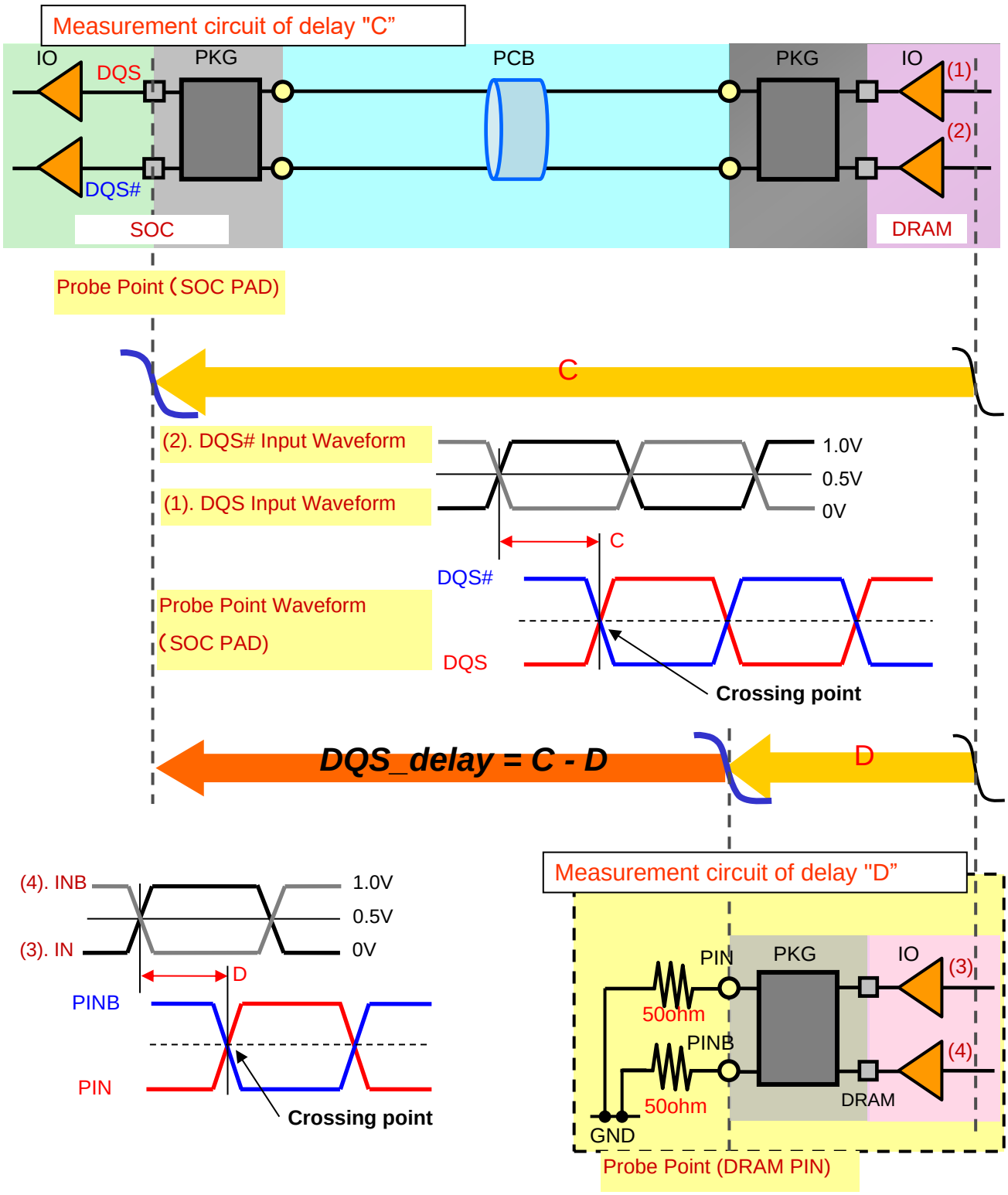


Figure 4-15 Measurement method of DQS_delay

4.2.3 Timing restrictions

Measurement methods for timing restriction are described in this section.

Timing restrictions shown in Table 4-11 must be confirmed at DRAM PAD / SOC PAD in Write/Read mode respectively. ISI and Xtalk effects of interconnect are evaluated in this measurement.

4.2.3.1 WRITE/READ DQ eye (degradation) (tdIVW_total)

Figure 4-16 shows a measurement example of DQ eye pattern. Vcent_DQ(pin_mid) is determined based on JEDEC standard. Maximum eye opening around Vcent_DQ(pin_mid) is measured as tdIVW_total(measured). The difference between UI and tdIVW_total(measured) is the degradation of WRITE (READ) DQ eye.

PCB design need to satisfy the target value of the DQ Eye degradation. Each target value is defined for both Write mode and Read mode. The all signals of DQ/DM need to be checked in both modes.

The trigger signal of DQ eye pattern is the differential signal of DQS and DQS#. Trigger level is differential zero volt.

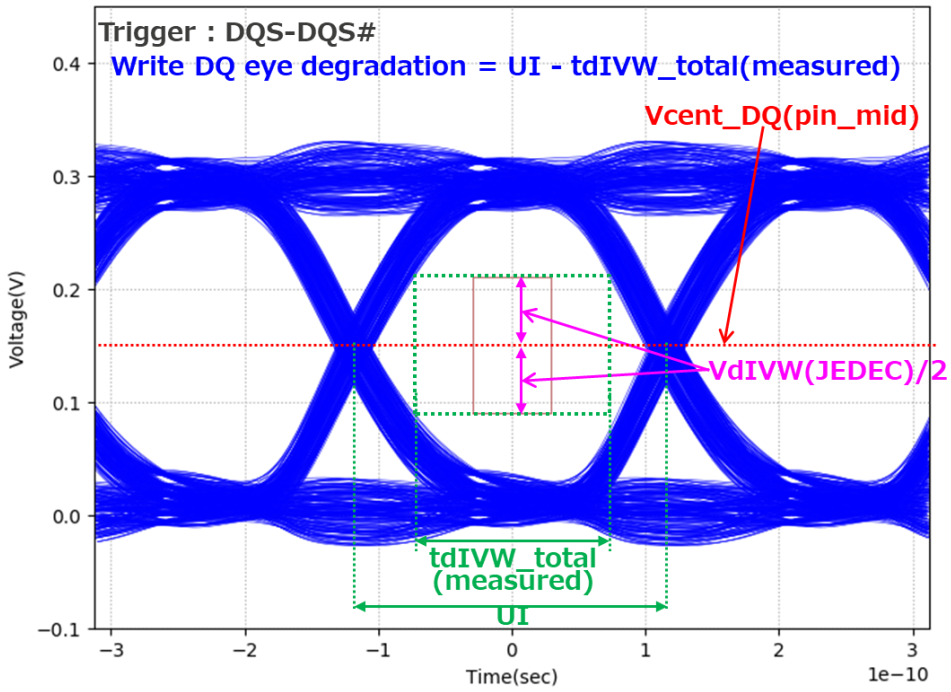


Figure 4-16 Measurement example of DQ Eye pattern

4.2.3.2 DQ Input pulse width (At Vcent_DQ) (degradation) (tdIPW_DQ)

This is the restriction for the pulse width of DQ. Each pulse width should be measured for all DQs and DMs. Input pulse width degradation is calculated as the difference between tCK(avg)/2 and measured minimum input pulse width. Input pulse width should be measured at Vcent_DQ(pin_mid) shown in JEDEC standard.

4.2.3.3 DQS input low/high pulse width (degradation) (tDQSL/tDQSH)

tDQSL/tDQSH should be checked in the same manner of clock low/high pulse width degradation (tCL/tCH). Please see section 4.2.3.6.

4.2.3.4 CA eye (degradation) (tcIVW)

Figure 4-17 shows a measurement example of CA eye pattern. Vcent_CA(pin_mid) is determined based on JEDEC standard. Maximum eye opening around Vcent_CA(pin_mid) is measured as tcIVW_total(measured). The difference between UI and tcIVW_total(measured) is the degradation of Write CA eye.

PCB design need to satisfy the target value of the CA Eye degradation. The all signals of CA/CS need to be checked.

The trigger signal of CA eye pattern is the differential signal of CK and CK#. Trigger level is differential zero volt.

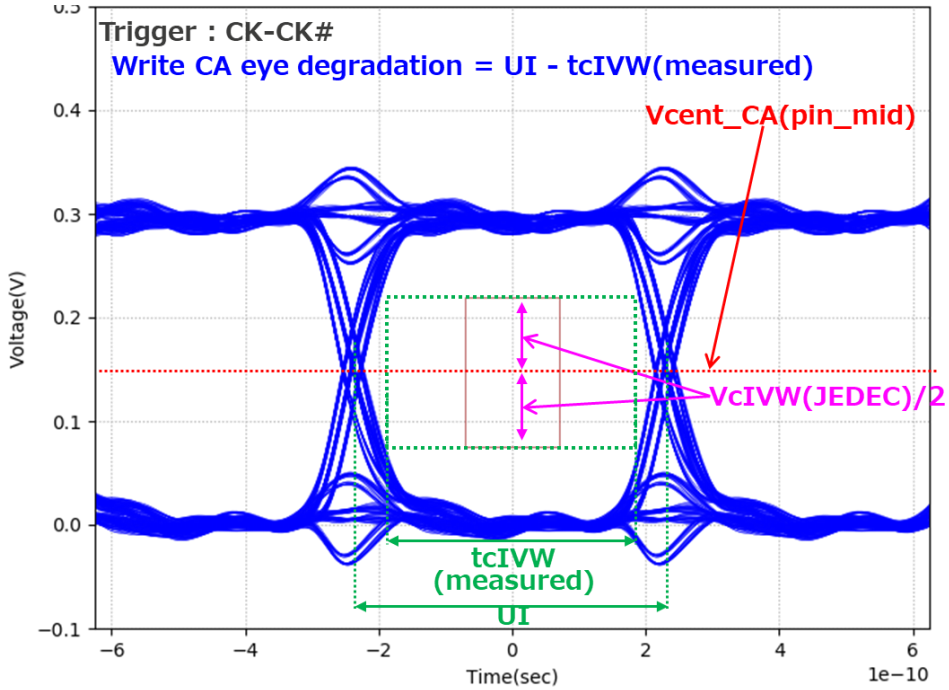


Figure 4-17 Measurement example of CA Eye pattern

4.2.3.5 CA input pulse width (degradation) (tcIPW)

This is the restriction for the pulse width of CA. Each pulse width should be measured for all CAs and CSs. Input pulse width degradation is calculated as the difference between tCK(avg) and measured minimum input pulse width. Input pulse width should be measured at Vcent_CA(pin_mid) shown in JEDEC standard.

4.2.3.6 Clock High/Low pulse width (degradation) (tCH(avg)/tCL(avg) and tCH(abs)/tCL(abs))

Figure 4-18 shows a measurement example of tCH/tCL. tCH(min) and tCL(min) are determined based on JEDEC standard. The difference between tCK(avg) and each measured value is the tCH/tCL degradation. tCK(avg) means the average of CK period. tCH(max) and tCL(max) need to be checked in the same manner. PCB design need to satisfy the target value of the clock high/low pulse width degradation.

Average value of tCH and tCL degradation should also satisfy the restriction for tCH(avg) and tCK(avg).

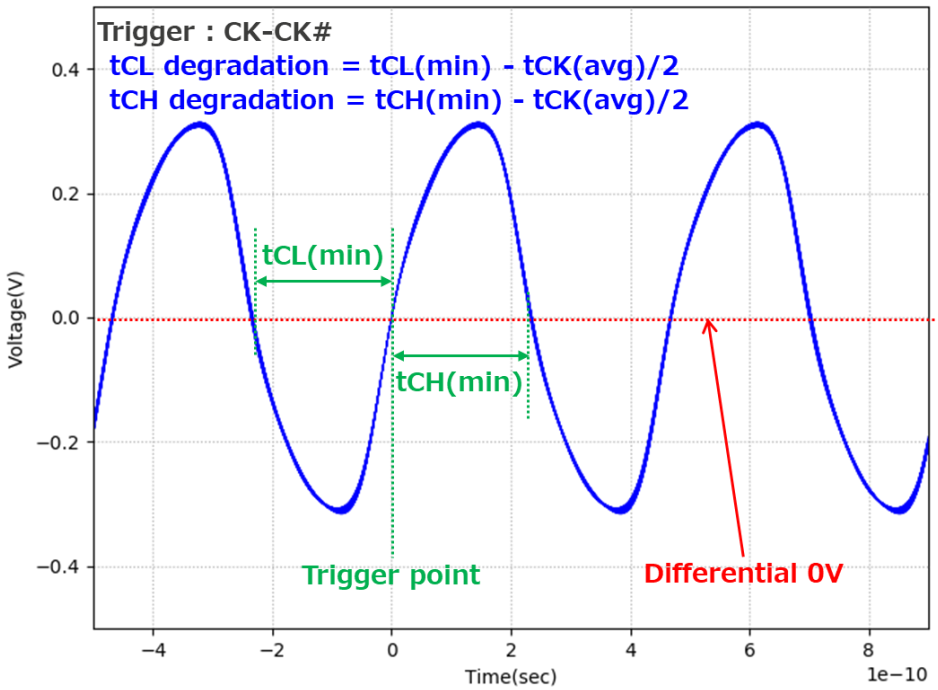


Figure 4-18 Measurement example of tCL/tCH

4.2.3.7 Clock period and cycle-cycle jitter (tJIT(per)/tJIT(cc))

Figure 4-19 shows a measurement example of tJIT(per). tCK(max) and tCK(min) are determined based on JEDEC standard. The difference between tCK(avg) and each measured value is the tJIT(per). tCK(avg) means the average of CK period.

PCB design need to satisfy the target value of the clock period jitter.

Similarly, tJIT(cc) need to be measured based on JEDEC standard and confirmed that the measured value satisfies the target value of the cycle-cycle jitter.

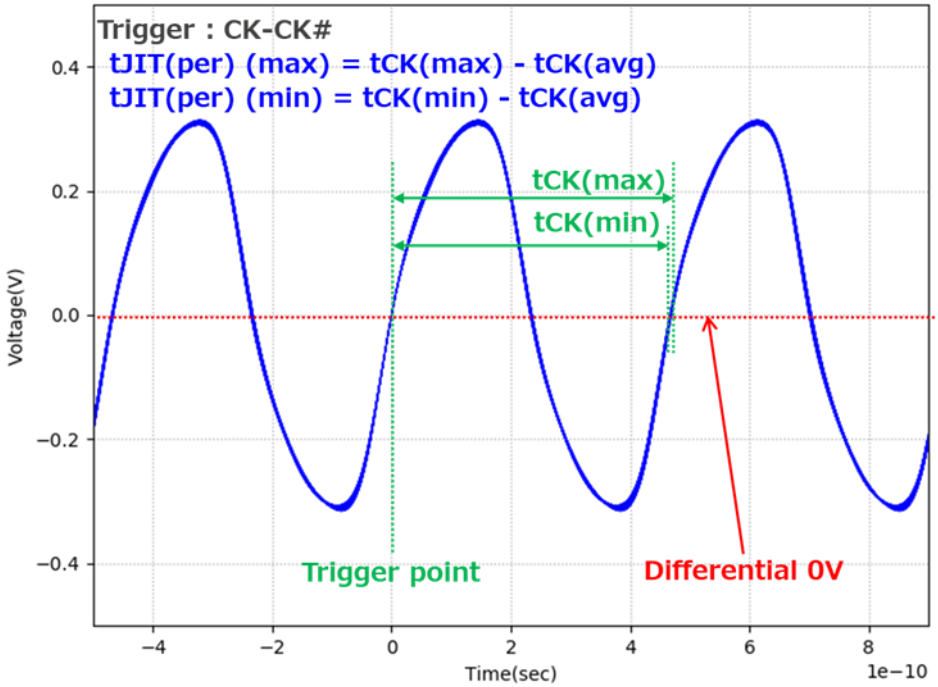
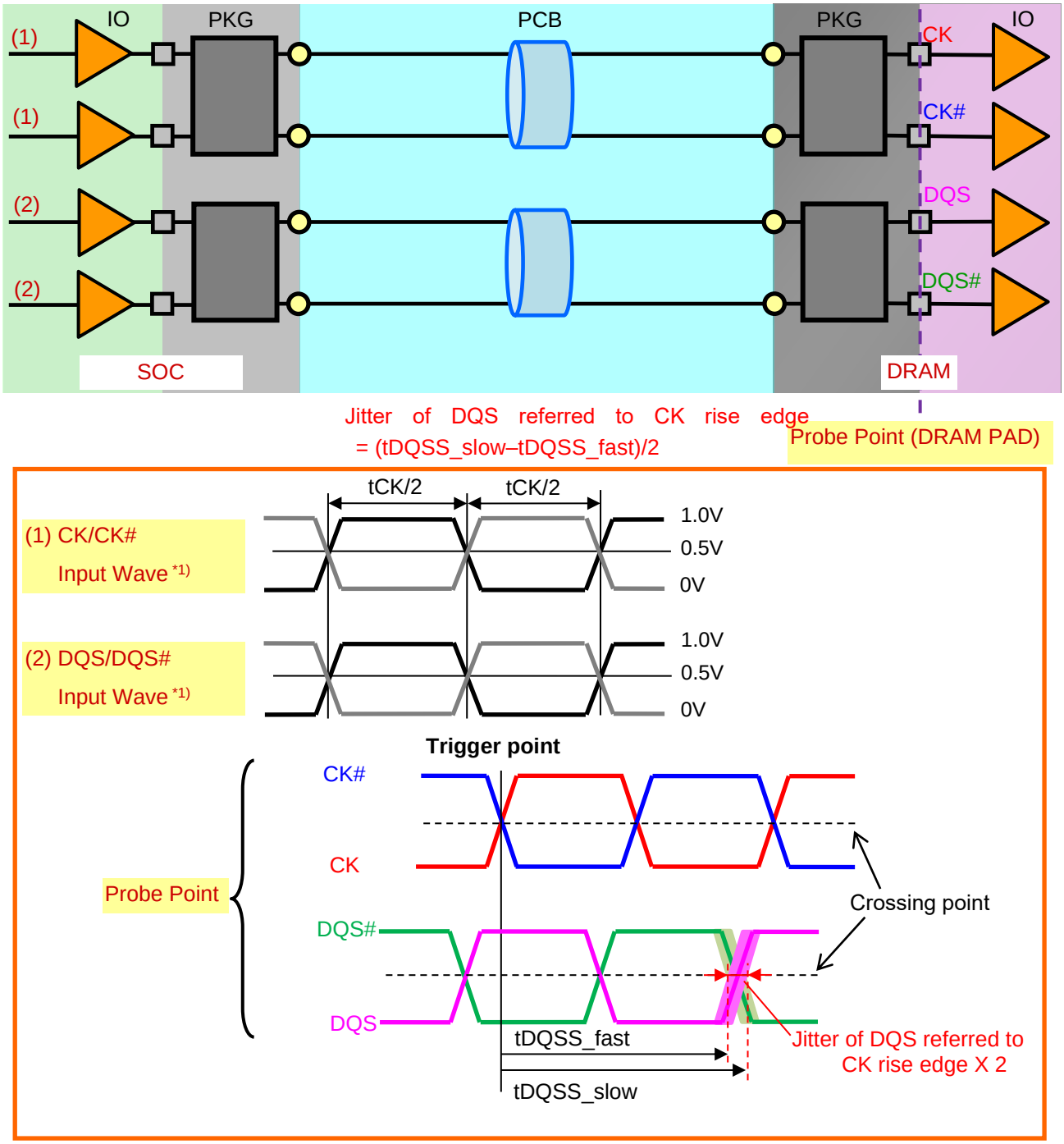


Figure 4-19 Measurement example of tJIT(per)

4.2.3.8 Jitter of DQS referred to CK rise edge (tDQSS)

Figure 4-20 shows the measurement method of DQS jitter referred to CK rise edge. Please measure difference between minimum and maximum time from CK rise edge to next DQS rise edge (shown as tDQSS_fast and tDQSS_slow). The jitter of DQS referred to CK rise edge in Table 4-11 is half of this difference (=(tDQSS_slow-tDQSS_fast)/2). PCB design need to satisfy the target value of the jitter.



*1) Input wave form of complementary side (# side) is inverted signal of true one because of the polarity of the IBIS model.

Figure 4-20 Measurement method of DQS jitter referred to CK rise edge

4.2.4 Waveform restrictions

Measurement method for waveform restrictions are described in JEDEC standard. Waveform restrictions shown in Table 4-12 must be confirmed at DRAM PAD / SOC PAD in Write/Read mode respectively. ISI and Xtalk effects of interconnect are evaluated in this measurement.

As an example of waveform restriction, Rx Mask voltage p-p is described in this section.

4.2.4.1 Rx Mask voltage p-p (for DQ and CA)

Figure 4-21 shows a measurement example of Rx Mask voltage p-p (for CA).

Minimum amplitude within the time range of eye mask (tcIVW in CA case) is measured as VcIVW_H(measured) and VcIVW_L(measured).

PCB design need to satisfy the target value of VcIVW/2.

The trigger signal of CA eye pattern is the differential signal of CK and CK#. Trigger level is differential zero volt.

Rx Mask voltage p-p (for DQ) need to be checked in the same manner.

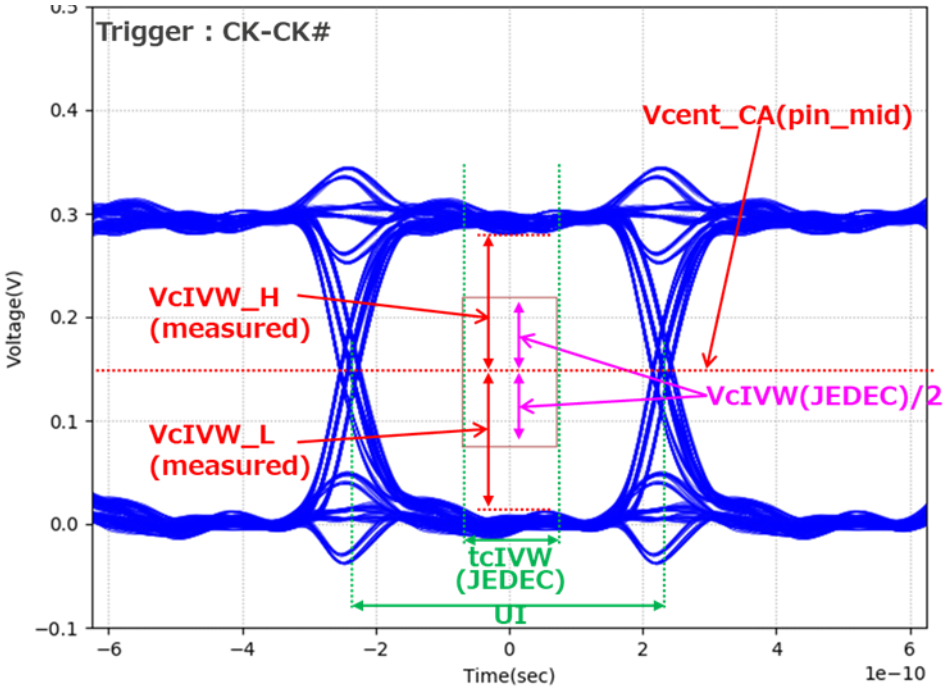


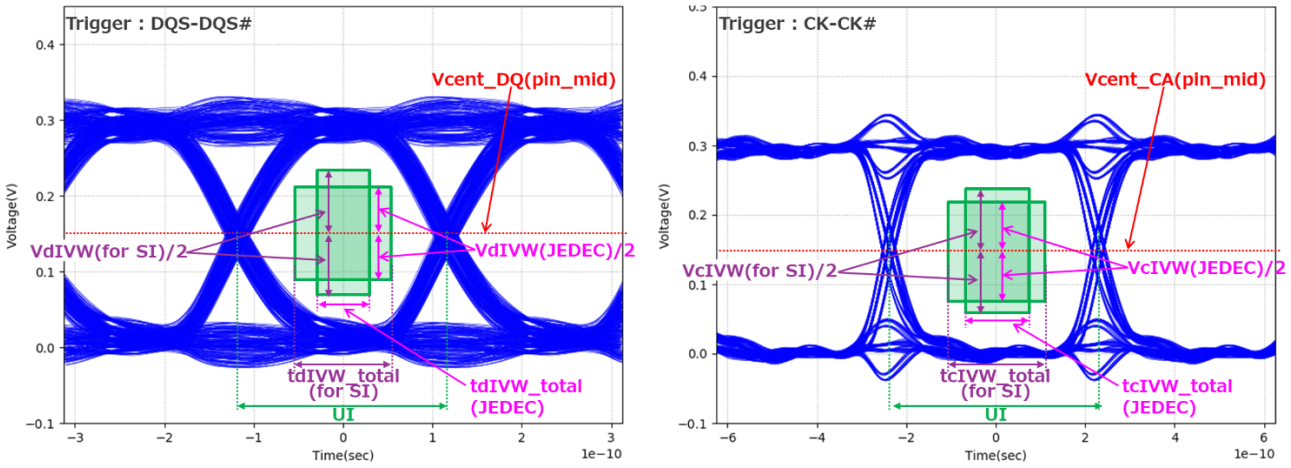
Figure 4-21 Measurement example of Rx Mask voltage p-p (for CA)

4.2.5 Eye mask definitions

Eye mask definitions for WRITE DQ, READ DQ and CA are shown in this section based on timing and waveform restrictions in 4.1.3 and 4.1.4. You can verify your PCB design using these eye mask specifications.

Figure 4-22 defines the eye masks for WRITE DQ, READ DQ and CA. Table 4-13 shows their eye mask specifications. The difference between JEDEC and SI specification mean the voltage noise and timing consumption of SOC.

These eye mask specifications include each eye degradation in timing restrictions and RX mask voltage p-p in waveform restrictions. The other restrictions shown in 4.1 should be checked in PCB design verification.



(a) WRITE / READ DQ (b) CA

Figure 4-22 Eye mask for WRITE / READ DQ and CA

Table 4-13 Eye mask specification

Category	VdIVW / VcIVW (JEDEC)	VdIVW / VcIVW (for SI)	tdIVW_total / tcIVW_total (JEDEC)	tdIVW_total / tcIVW_total (for SI, UI=234ps)
WRITE DQ	120mV	140mV	58.5ps	146ps
READ DQ	–	140mV	-	139ps
CA	145mV	170mV	140.4ps	251ps

5 Verification items and method of IO Power Distribution Network (PDN)

5.1 Verification items

The target impedance Ztarget(f) is shown in Table 5-1 and Table 5-2, which is defined for the power domain of 16bit width. Frequency range for Ztarget(f) is defined higher than 100kHz. IO PDN must be designed so that the voltage is kept in the range specified by SOC specification.

Table 5-1 Target impedance for VDDQVA_DDRp

Frequency	Target impedance : Ztarget(f)		
	Min	Max	Unit
100kHz~20MHz	-	0.100	ohm
20MHz~1GHz	-	0.500	ohm

Table 5-2 Target impedance for VDDQX_DDRp

Frequency	Target impedance : Ztarget(f)		
	Min	Max	Unit
100kHz~10MHz	-	0.100	ohm
10MHz~20MHz	-	0.200	ohm
20MHz~100MHz	-	2.000	ohm
100MHz~1GHz	-	8.000	ohm

Please also check the specifications on DRAM and PMIC side.

5.2 Verification method

Renesas prepared SOC IO PDN model to confirm target impedance of SOC IO power supply for DDR-IF (VDDQVA_DDRp and VDDQX_DDRp). Please prepare PCB PDN model of your design. “p” is from 0 to 1.

Figure 5-1 shows measurement method of VDDQVA_DDRp. VDDQX_DDRp should be verified in the same manner.

Please connect PCB and SOC PDN models as in Figure 5-1 and confirm PDN impedance in every frequency to meet the target impedance as in Figure 5-2 and Figure 5-3.

Power domain must be verified for 16bit width separately.

In the case that the different power supply domains are merged in PCB, the verification method is described in section 5.3.

All impedances are less than target impedance in every frequency as in Figure 5-2 and Figure 5-3.

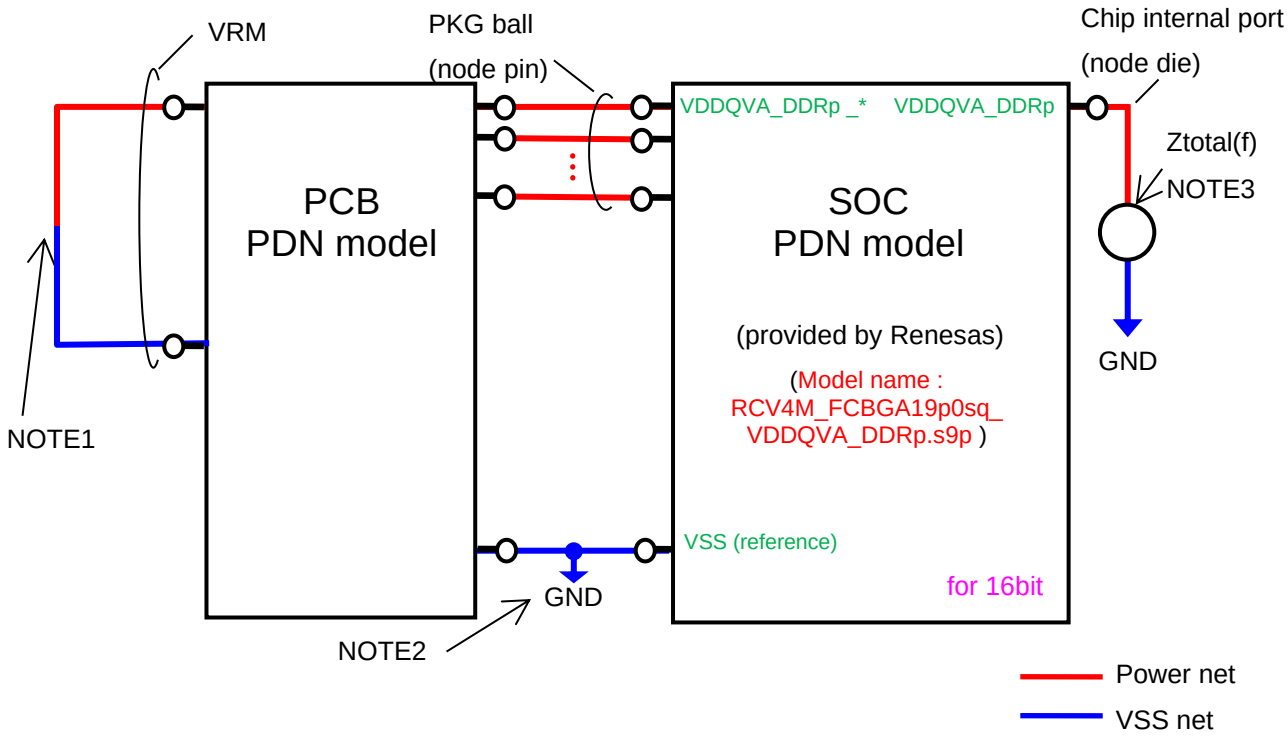


Figure 5-1 Connection for Ztotal(f) calculation

- NOTE1: Power node is shorted to VSS node on VRM side.
  Appropriate setting of GND is very important to simulate PDN impedance.
  For example, the VSS node on VRM side should NOT be connected to the GND node.
- NOTE2: VSS (reference) node on PCB PDN model (PKG ball side) is connected to the GND.
  VSS (reference) node on SOC PDN model (PKG ball side) is connected to the GND.
- NOTE3: Ztotal(f) is that loop impedance from chip internal port to the GND.

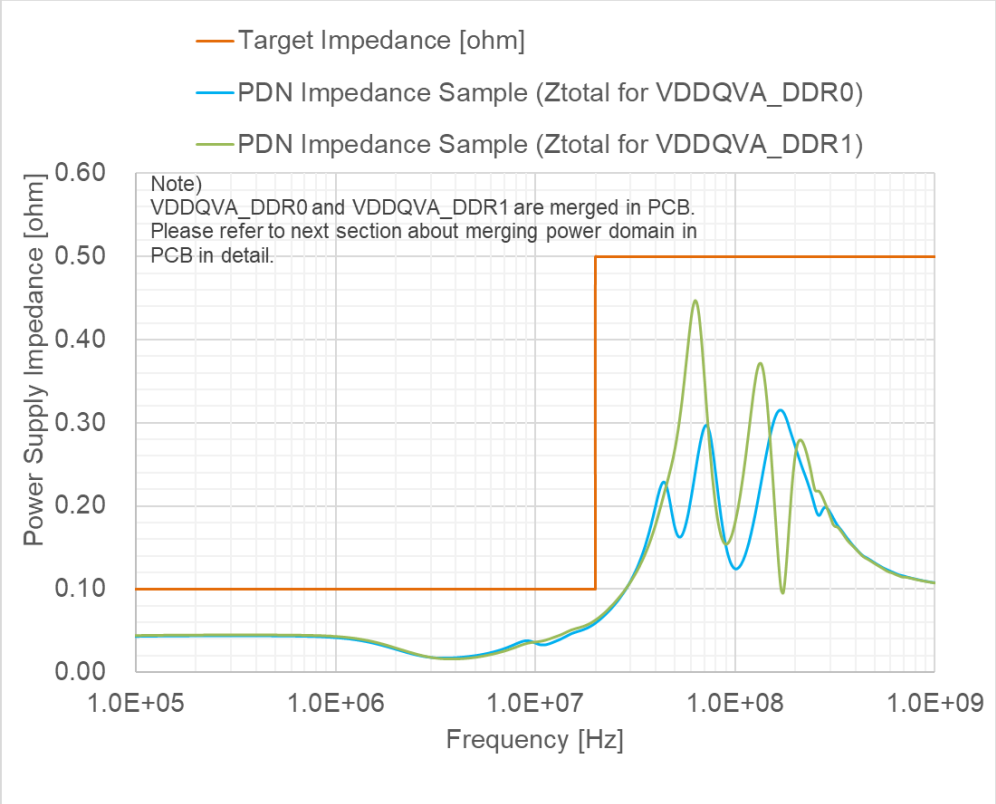


Figure 5-2 PDN impedance of VDDQVA_DDRp

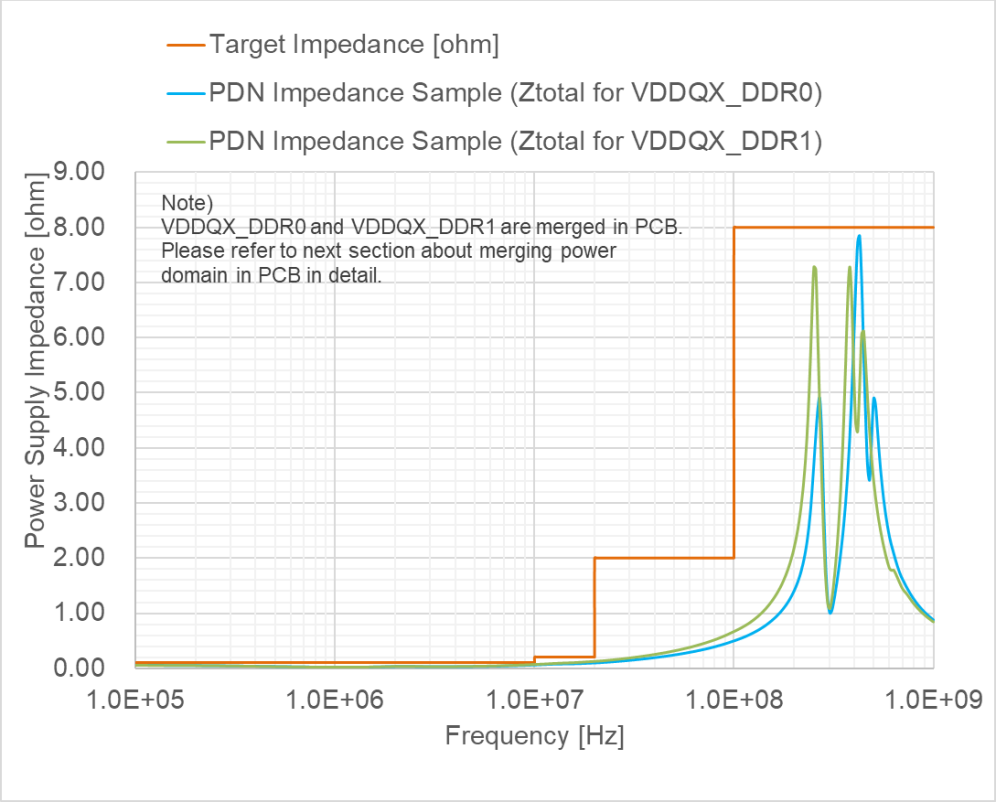


Figure 5-3 PDN impedance of VDDQX_DDRp

5.3 Merging Power Domain in PCB

This section describes how to merge between the different power supply domains in PCB. In merging power domain, please also check the specifications on DRAM and PMIC side.

For SOC side, the following power supply merging is possible.

i) Within VDDQVA_DDRp (p = 0,1):
Power supply can be merged between p=0 and 1.

ii) Within VDDQX_DDRp (p = 0,1):
Power supply can be merged between p=0 and 1.

iii) Between VDDQVA_DDRp and VDDQX_DDRp (p = 0,1):
Cannot be merged.

In merging the two power domains, it is a good way to merge these near the PMIC instead of merging from the vicinity of the SOC, because this way reduces transfer impedance effectively.

In the succeeding sections, the power supply names VDDQVA_DDRp and VDDQX_DDRp are abbreviated as q [p] and x [p], respectively, which are used for suffix of impedance Z. The meaning of each impedance is as follows:

Zq[p]q[p]:	Self-impedance of VDDQVA_DDRp.
Zx[p]x[p]:	Self impedance of VDDQX_DDRp
Zx[p]x[p'(≠p)]:	Transfer impedance from VDDQX_DDRp' to VDDQX_DDRp
Zq[p]q[p'(≠p)]:	Transfer impedance from VDDQVA_DDRp' to VDDQVA_DDRp

5.3.1 Merging Power Domain within VDDQVA_DDRp, and within VDDQX_DDRp

Possible combination of merging power supply within VDDQVA_DDRp, and within VDDQX_DDRp, namely, the case i) and ii), is summarized in 5.3.

“Base PDN” means a power supply domain for which Ztotal is calculated.

"Merged PDN" means a power domain that is merged with the Base PDN.

“Ztotal" column shows equation of Ztotal for “Base PDN” merged with “Merged PDN“.

“Ztarget spec” column shows the table number of the specification that Ztotal should satisfy. Please confirm that all Ztotals are within these specifications.

Table 5-3 Possible combination of power supply merging within VDDQVA_DDRp, and within VDDQX_DDRp (p = 0,1)

No.	Base PDN \ Merged PDN	VDDQVA_DDR0(=q0)	VDDQVA_DDR1(=q1)	VDDQX_DDR0(=x0)	VDDQX_DDR1(=x1)	Ztotal (Ztotal for "Base PDN" merged with "Merged PDN")	Ztarget spec
1	VDDQVA_DDR0(=q0)	Zq0q0	Zq0q1			Ztotal_q0=Zq0q0+Zq0q1	Table 5-1
2	VDDQVA_DDR1(=q1)	Zq1q0	Zq1q1			Ztotal_q1= Zq1q0+Zq1q1	
3	VDDQX_DDR0(=x0)			Zx0x0	Zx0x1	Ztotal_x0=Zx0x0+Zx0x1	Table 5-2
4	VDDQX_DDR1(=x1)			Zx1x0	Zx1x1	Ztotal_x1= Zx1x0+Zx1x1	

Example) q [p] is merged between p=0 and 1.
This case corresponds to No.1 to No.4 in Table 5-3.
Figure 5-4 shows how to calculate the impedance Ztotal when q [p] is merged between p=0 and 1.

Please connect the models as shown in Figure 5-4 and calculate the following impedance (p = 0,1):

Figure 5-4 (A): calculate Zq[p]q0(f),
Figure 5-4 (B): calculate Zq[p]q1(f),

where Ztotal can be obtained by the following equation:

Ztotal_q0 = Zq0q0(f) + Zq0q1(f),
Ztotal_q1 = Zq1q0(f) + Zq1q1(f),

and must be satisfied the specification in Table 5-1.

These impedances can be calculated equivalently as in the Figure 5-5.

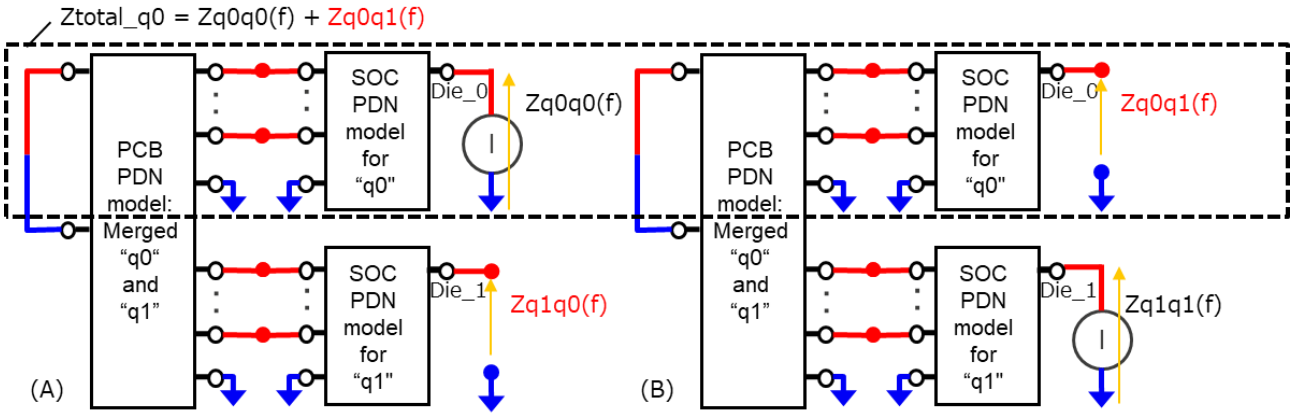


Figure 5-4 How to calculate the impedance Ztotal when q [p] is merged between p=0 and 1 (1)

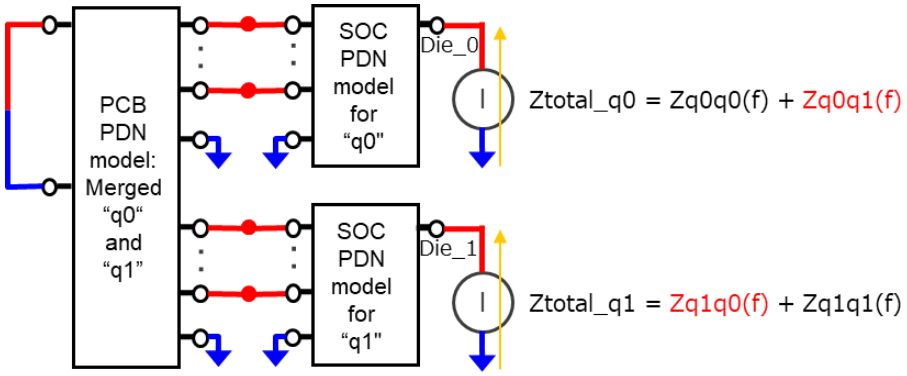


Figure 5-5 How to calculate the impedance Ztotal when q [p] is merged between p=0 and 1 (2)

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	2024/09/30	-	Newly issued.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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