CONFIDENTIAL

User's Guide

R-Car V4M FCBGA 19.0sq

PCB verification guide for Power Supply of IO

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SoCs for Automotive

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R-Car V4M

IO Power Supply Verification Guide

The purpose of this guide

This guide helps PCB design engineers to verify their design and arrive to their design goal. To achieve the best SOC performance, Power Distribution Network (PDN) for IO power supply is very important. Therefore, we recommend the PDN impedance get lower than the target impedance on PCBs for each IO power supply.

This guide describes a) PCB design restrictions, b) verification items and c) how to measure them.

It is indispensable to satisfy PCB restrictions described in this guide in order to enable core function in user's system. Renesas recommends the customer to confirm satisfying restrictions in this guide.

All information shown in this guide, including product specifications, represents the information at the time of publication and is subject to change by Renesas Electronics Corp. without notice. Please review the latest information published by Renesas Electronics Corp.

SOC means R-Car V4M (FCBGA) in this document.

R-CarV4M

IO Power Supply PCB Verification Guide

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1. Introduction

1.1 Overview

This document will provide PCB verification guide on PDN for IO power supply. The purpose of this guide is to help PCB design engineers to design power supplies in their PCB design.

To secure the stable operation of SOC, power integrity verification is needed in this guide.

This guide regulates only 100 kHz or higher. For frequencies lower than that, secure the power supply pattern width and the number of via in consideration of the DC current value.

1.2 Operating conditions

Please see SOC User’s Manual.

1.3 Power name

Power supply pins are listed in Table 1-1.

Table 1-1 Power supply list

Item	Symbol		Voltage	Reference
	Power ball	Ground ball		
Power supply (1.8V I/O)	VDDQ18	VSS	1.8V	Chapter 2-1 VDDQ18 Power Supply
Power supply (3.3V I/O)	VDDQ33	VSS	3.3V	Chapter 2-2 VDDQ33 Power Supply
Power supply (1.8V/3.3V I/O)	VDDQ18_33_SPI	VSS	1.8V/3.3V	Chapter 2-3 VDDQ18_33_SPI Power Supply
Power supply (1.8V/3.3V I/O)	VDDQ18_33_I2C	VSS	1.8V/3.3V	Chapter 2-4 VDDQ18_33_I2C Power Supply
Power supply (1.8V/3.3V I/O)	VDDQ18_33_SDHI	VSS	1.8V/3.3V	Chapter 2-5 VDDQ18_33_SDHI Power Supply
Power supply (1.8V/2.5V I/O)	VDDQ18_25_AVB	VSS	1.8V/2.5V	Chapter 2-6 VDDQ18_25_AVB Power Supply
Power supply (1.8V TRNG)	VDD18_TRNG	VSS	1.8V	Chapter 2-7 VDD18_TRNG Power Supply
Power supply (1.8V OCO)	VDD18_OCO	VSS	1.8V	Chapter 2-8 VDD18_OCO Power Supply
Power supply (1.8V OTP)	VDD18_OTP	VSS	1.8V	Chapter 2-9 VDD18_OTP Power Supply
Power supply (1.8V PLL)	VDD18_CPGPLL1	VSS	1.8V	Chapter 2-10 VDD18_CPGPLL1 Power Supply
Power supply (1.8V PLL)	VDD18_CPGPLL2	VSS	1.8V	Chapter 2-11 VDD18_CPGPLL2 Power Supply
Power supply (1.8V PLL)	VDD18_CPGPLL3	VSS	1.8V	Chapter 2-12 VDD18_CPGPLL3 Power Supply
Power supply (1.8V PLL)	VDD18_CPGPLL4	VSS	1.8V	Chapter 2-13 VDD18_CPGPLL4 Power Supply
Power supply (1.8V PLL)	VDD18_CPGPLL5	VSS	1.8V	Chapter 2-14 VDD18_CPGPLL5 Power Supply
Power supply (1.8V PLL)	VDD18_CPGPLL6	VSS	1.8V	Chapter 2-15 VDD18_CPGPLL6 Power Supply
Power supply (1.8V PLL)	VDD18_CPGPLL7	VSS	1.8V	Chapter 2-16 VDD18_CPGPLL7 Power Supply

2. Design Guidelines for Power Supply Lines on PCBs

2.1 VDDQ18 Power Supply

Specifications for the design of power supply circuits for VDDQ18 are given below.

- Place each bypass capacitors as close to SoC as possible.
- Be sure to place bypass capacitors close to VDDQ18 balls near the QSPI signal balls.
- Be sure to place bypass capacitors close to VDDQ18 balls away from the QSPI signal balls.
- Place the bypass capacitors of smaller value closer to SoC pins.

Figure 2-1 shows a circuit diagram of VDDQ18 power supply and external parts. Table 2-1 shows the recommended parameters of VDDQ18 power supply circuit component.

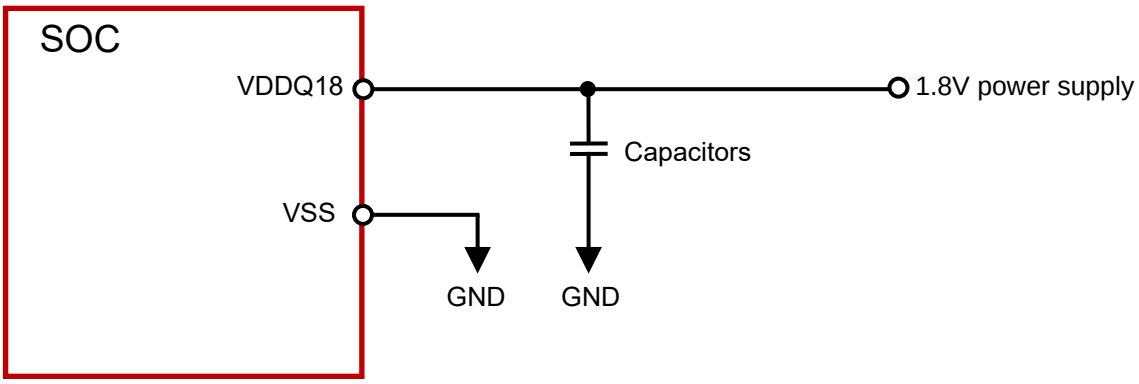


Figure 2-1 Circuit diagram of VDDQ18 power supply and external parts

Table 2-1 Recommended parameters of VDDQ18 power supply circuit component

Pin name	Value	Pics.	Loop Inductance	Note
VDDQ18	0.1 uF	1	Less than 1.11nH	Refer to “Appendix. Concept of Loop Inductance”
	4700 pF	1		

Please also check the specifications on PMIC side.

2.2 VDDQ33 Power Supply

Specifications for the design of power supply circuits for VDDQ33 are given below.

- Place each bypass capacitors as close to SoC as possible.
- Place the bypass capacitors of smaller value closer to SoC pins.

Figure 2-2 shows a circuit diagram of VDDQ33 power supply and external parts. Table 2-2 shows the recommended parameters of VDDQ33 power supply circuit component.

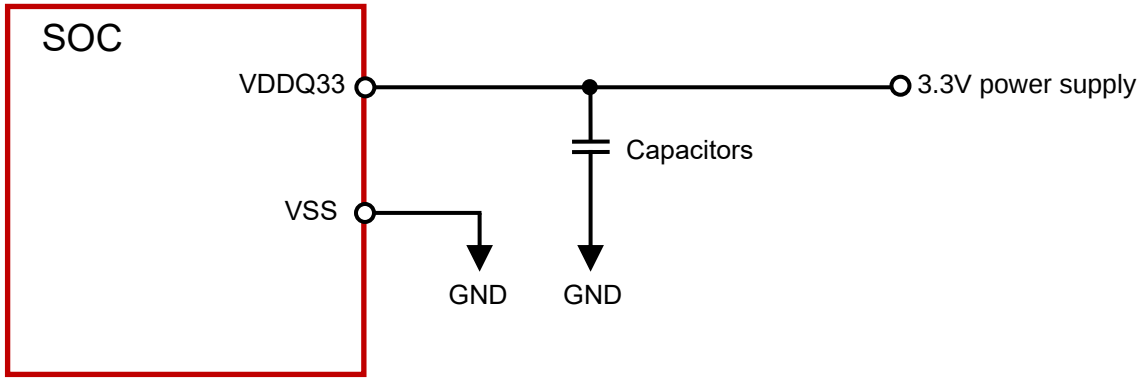


Figure 2-2 Circuit diagram of VDDQ33 power supply and external parts

Table 2-2 Recommended parameters of VDDQ33 power supply circuit component

Pin name	Value	Pics.	Loop Inductance	Note
VDDQ33	1 uF	3	Less than 1.40nH	Refer to “Appendix. Concept of Loop Inductance”

Please also check the specifications on PMIC side.

2.3 VDDQ18_33_SPI Power Supply

Specifications for the design of power supply circuits for VDDQ18_33_SPI are given below.

- Place each bypass capacitors as close to SoC as possible.
- Place the bypass capacitors of smaller value closer to SoC pins.

Figure 2-3 shows a circuit diagram of VDDQ18_33_SPI power supply and external parts. Table 2-3 shows the recommended parameters of VDDQ18_33_SPI power supply circuit component.

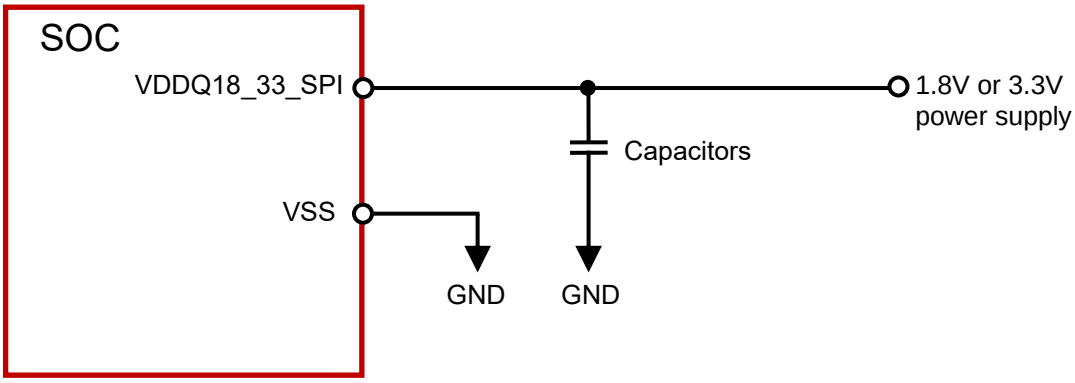


Figure 2-3 Circuit diagram of VDDQ18_33_SPI power supply and external parts

Table 2-3 Recommended parameters of VDDQ18_33_SPI power supply circuit component

Pin name	Value	Pics.	Loop Inductance	Note
VDDQ18_33_SPI	1 uF	1	Less than 1.00nH	Refer to “Appendix. Concept of Loop Inductance”
	1000 pF	4		

Please also check the specifications on PMIC side.

2.4 VDDQ18_33_I2C Power Supply

Specifications for the design of power supply circuits for VDDQ18_33_I2C are given below.

- Place each bypass capacitors as close to SoC as possible.
- Place the bypass capacitors of smaller value closer to SoC pins.

Figure 2-4 shows a circuit diagram of VDDQ18_33_I2C power supply and external parts. Table 2-4 shows the recommended parameters of VDDQ18_33_I2C power supply circuit component.

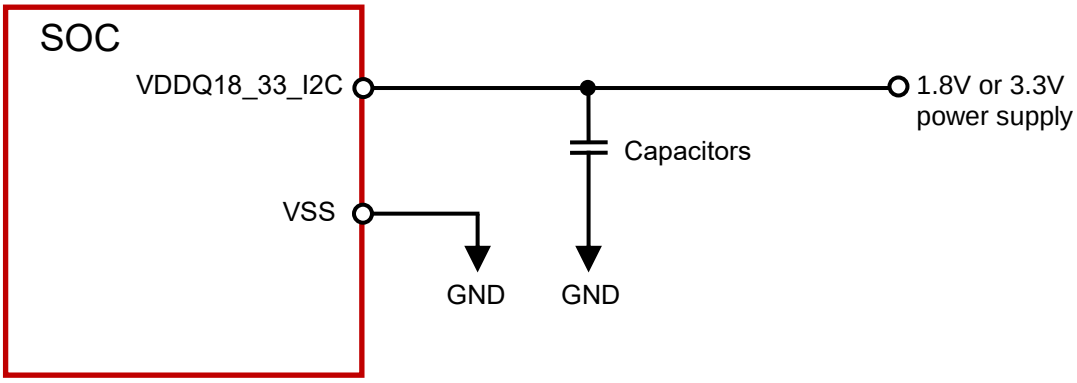


Figure 2-4 Circuit diagram of VDDQ18_33_I2C power supply and external parts

Table 2-4 Recommended parameters of VDDQ18_33_I2C power supply circuit component

Pin name	Value	Pics.	Loop Inductance	Note
VDDQ18_33_I2C	1 uF	1	Less than 1.76nH	Refer to “Appendix. Concept of Loop Inductance”
	6800 pF	2		

Please also check the specifications on PMIC side.

2.5 VDDQ18_33_SDHI Power Supply

Specifications for the design of power supply circuits for VDDQ18_33_SDHI are given below.

- Place each bypass capacitors as close to SoC as possible.
- Place the bypass capacitors of smaller value closer to SoC pins.

Figure 2-5 shows a circuit diagram of VDDQ18_33_SDHI power supply and external parts. Table 2-5 shows the recommended parameters of VDDQ18_33_SDHI power supply circuit component.

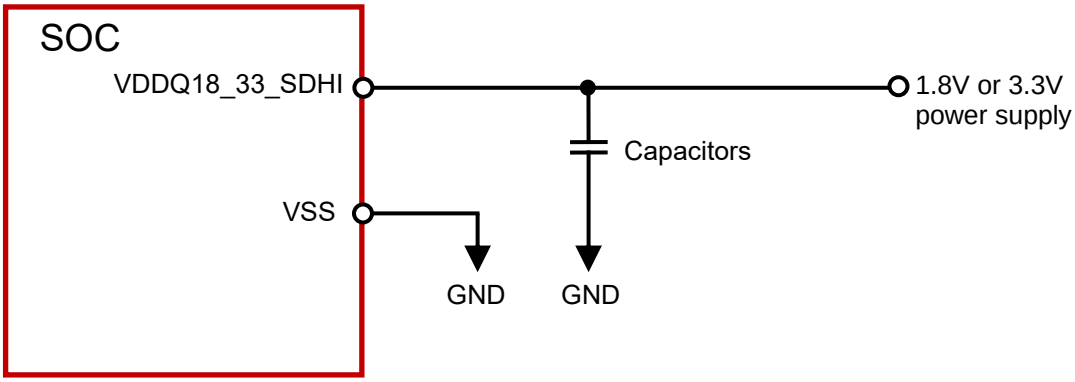


Figure 2-5 Circuit diagram of VDDQ18_33_SDHI power supply and external parts

Table 2-5 Recommended parameters of VDDQ18_33_SDHI power supply circuit component

Pin name	Value	Pics.	Loop Inductance	Note
VDDQ18_33_SDHI	1 uF	1	Less than 1.00nH	Refer to “Appendix. Concept of Loop Inductance”
	470 pF	3		

Please also check the specifications on PMIC side.

2.6 VDDQ18_25_AVB Power Supply

Specifications for the design of power supply circuits for VDDQ18_25_AVB are given below.

- Place each bypass capacitors as close to SoC as possible.
- Place the bypass capacitors of smaller value closer to SoC pins.

Figure 2-6 shows a circuit diagram of VDDQ18_25_AVB power supply and external parts. Table 2-6 shows the recommended parameters of VDDQ18_25_AVB power supply circuit component.

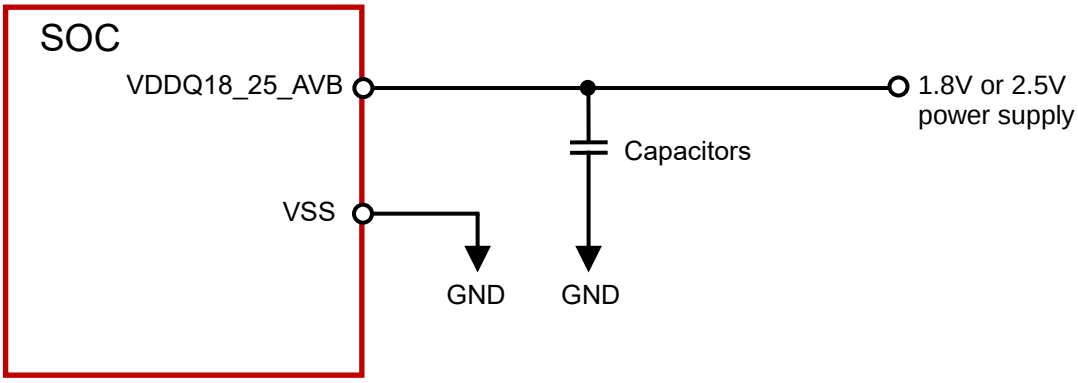


Figure 2-6 Circuit diagram of VDDQ18_25_AVB power supply and external parts

Table 2-6 Recommended parameters of VDDQ18_25_AVB power supply circuit component

Pin name	Value	Pics.	Loop Inductance	Note
VDDQ18_25_AVB	1 uF	2	Less than 0.52nH	Refer to “Appendix. Concept of Loop Inductance”
	1000 pF	3		

Please also check the specifications on PMIC side.

2.7 VDD18_TRNG Power Supply

Specifications for the design of power supply circuits for VDD18_TRNG are given below.

- Place each bypass capacitors as close to SoC as possible.
- Place the bypass capacitors of smaller value closer to SoC pins.

Figure 2-7 shows a circuit diagram image of VDD18_TRNG power supply and external parts that compose a low pass filter. Table 2-7 shows the recommended parameters of VDD18_TRNG power supply circuit component.

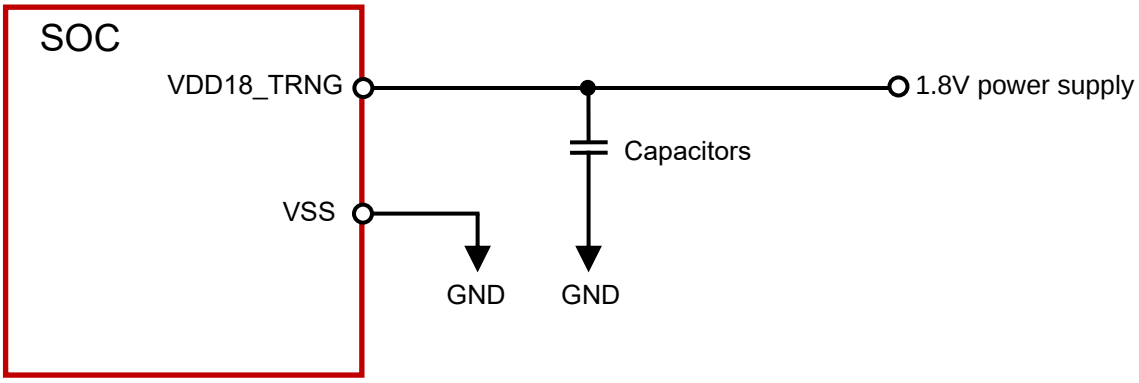


Figure 2-7 Circuit diagram of VDD18_TRNG power supply and external parts

Table 2-7 Recommended parameters of VDD18_TRNG power supply circuit component

Pin name	Value	Pics.	Loop Inductance	Note
VDD18_TRNG	4.7 uF	1	Less than 2.80nH	Refer to “Appendix. Concept of Loop Inductance”
	0.1 uF	1		

Please also check the specifications on PMIC side.

2.8 VDD18_OCO Power Supply

Specifications for the design of power supply circuits for VDD18_OCO are given below.

- Place each bypass capacitors as close to SoC as possible.
- Place the bypass capacitors of smaller value closer to SoC pins.

Figure 2-8 shows a circuit diagram image of VDD18_OCO power supply and external parts that compose a low pass filter. Table 2-8 shows the recommended parameters of VDD18_OCO power supply circuit component.

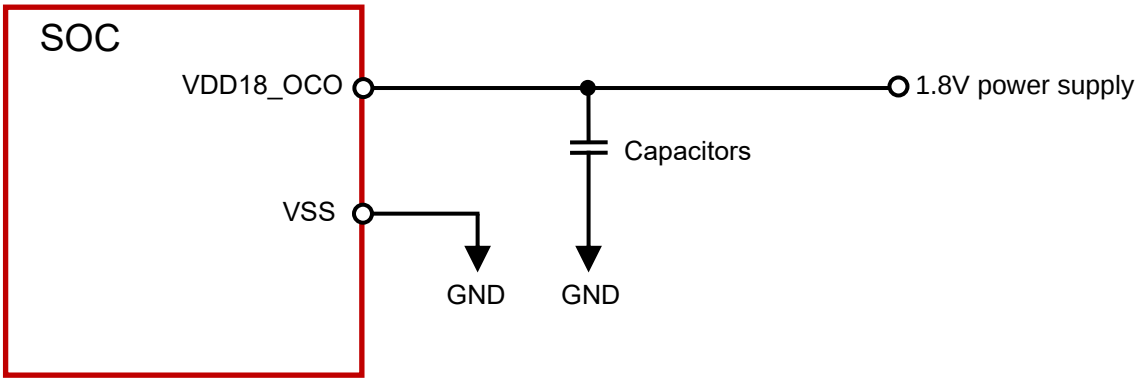


Figure 2-8 Circuit diagram of VDD18_OCO power supply and external parts

Table 2-8 Recommended parameters of VDD18_OCO power supply circuit component

Pin name	Value	Pics.	Loop Inductance	Note
VDD18_OCO	0.1 uF	1	Less than 2.80nH	Refer to “Appendix. Concept of Loop Inductance”

Please also check the specifications on PMIC side.

2.9 VDD18_OTP Power Supply

Specifications for the design of power supply circuits for VDD18_OTP are given below.

- Place each bypass capacitors as close to SoC as possible.
- Place the bypass capacitors of smaller value closer to SoC pins.

Figure 2-9 shows a circuit diagram image of VDD18_OTP power supply and external parts that compose a low pass filter. Table 2-9 shows the recommended parameters of VDD18_OTP power supply circuit component.

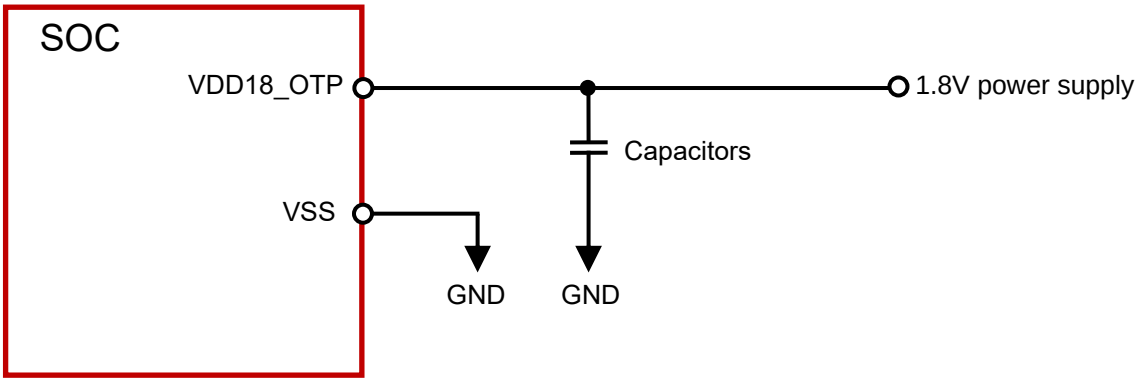


Figure 2-9 Circuit diagram of VDD18_OTP power supply and external parts

Table 2-9 Recommended parameters of VDD18_OTP power supply circuit component

Pin name	Value	Pics.	Loop Inductance	Note
VDD18_OTP	0.1 uF	1	Less than 3.00nH	Refer to “Appendix. Concept of Loop Inductance”

Please also check the specifications on PMIC side.

2.10 VDD18_CPGPLL1 Power Supply

Specifications for the design of power supply circuits for VDD18_CPGPLL1 are given below.

- RC-filter is strongly recommended because PLL is very sensitive for power noise.
- Place each bypass capacitors as close to SoC as possible.
- Place the bypass capacitors on the BGA ball side and the resistance beyond it.
- Be careful of crosstalk when resistance leaves SoC.

Figure 2-10 shows a circuit diagram image of VDD18_CPGPLL1 power supply and external parts that compose a low pass filter. Table 2-10 shows the recommended parameters of VDD18_CPGPLL1 power supply circuit component.

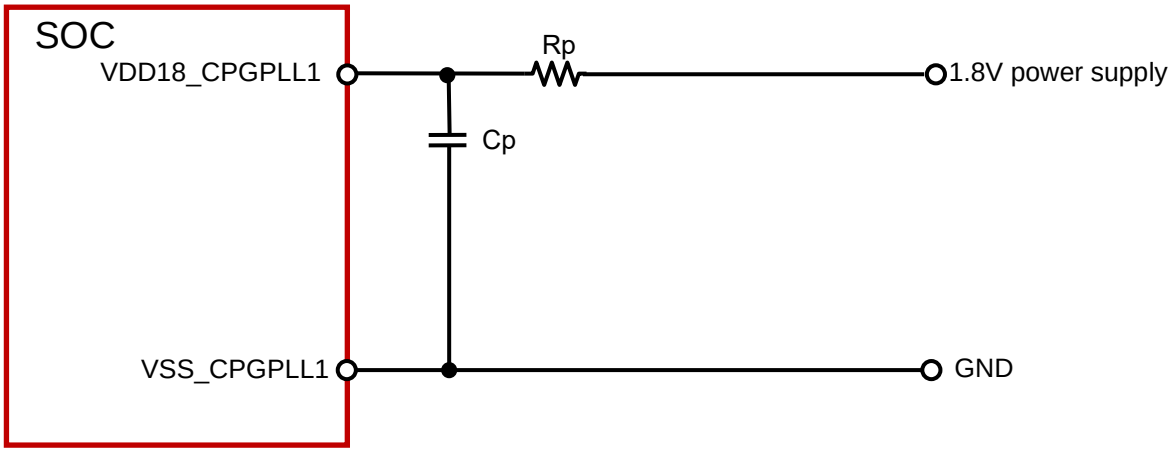


Figure 2-10 Circuit diagram of VDD18_CPGPLL1 power supply and external parts

Table 2-10 Recommended parameters of VDD18_CPGPLL1 power supply circuit component

Pin name	Low pass filter	Loop Inductance	Note
VDD18_CPGPLL1	Cp=1uF Rp=1ohm	Less than 4.30nH	Refer to “Appendix. Concept of Loop Inductance”

Please also check the specifications on PMIC side.

2.11 VDD18_CPGPLL2 Power Supply

Specifications for the design of power supply circuits for VDD18_CPGPLL2 are given below.

- LC-filter is strongly recommended because PLL is very sensitive for power noise.
- Place each bypass capacitors as close to SoC as possible.
- Place the bypass capacitors on the BGA ball side and the inductance beyond it.
- Be careful of crosstalk when resistance leaves SoC.

Figure 2-11 shows a circuit diagram image of VDD18_CPGPLL2 power supply and external parts that compose a low pass filter. Table 2-11 shows the recommended parameters of VDD18_CPGPLL2 power supply circuit component.

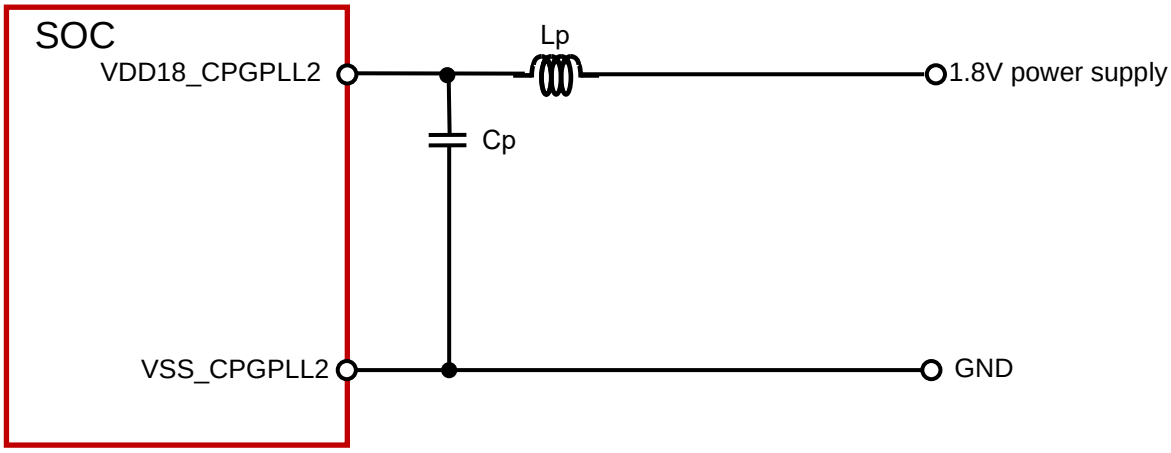


Figure 2-11 Circuit diagram of VDD18_CPGPLL2 power supply and external parts

Table 2-11 Recommended parameters of VDD18_CPGPLL2 power supply circuit component

Pin name	Low pass filter	Loop Inductance	Note
VDD18_CPGPLL2	Cp=1uF Lp=2nH	Less than 4.00nH	Refer to “Appendix. Concept of Loop Inductance”

Please also check the specifications on PMIC side.

2.12 VDD18_CPGPLL3 Power Supply

Specifications for the design of power supply circuits for VDD18_CPGPLL3 are given below.

- LC-filter is strongly recommended because PLL is very sensitive for power noise.
- Place each bypass capacitors as close to SoC as possible.
- Place the bypass capacitors on the BGA ball side and the inductance beyond it.
- Be careful of crosstalk when resistance leaves SoC.

Figure 2-12 shows a circuit diagram image of VDD18_CPGPLL3 power supply and external parts that compose a low pass filter. Table 2-12 shows the recommended parameters of VDD18_CPGPLL3 power supply circuit component.

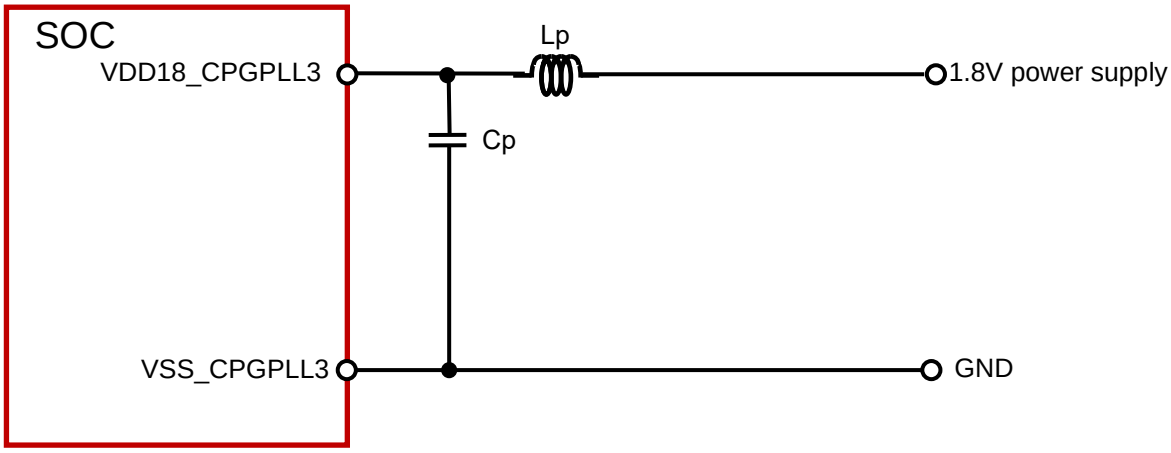


Figure 2-12 Circuit diagram of VDD18_CPGPLL3 power supply and external parts

Table 2-12 Recommended parameters of VDD18_CPGPLL3 power supply circuit component

Pin name	Low pass filter	Loop Inductance	Note
VDD18_CPGPLL3	Cp=1uF Lp=2nH	Less than 4.00nH	Refer to “Appendix. Concept of Loop Inductance”

Please also check the specifications on PMIC side.

2.13 VDD18_CPGPLL4 Power Supply

Specifications for the design of power supply circuits for VDD18_CPGPLL4 are given below.

- RC-filter is strongly recommended because PLL is very sensitive for power noise.
- Place each bypass capacitors as close to SoC as possible.
- Place the bypass capacitors on the BGA ball side and the resistance beyond it.
- Be careful of crosstalk when resistance leaves SoC.

Figure 2-13 shows a circuit diagram image of VDD18_CPGPLL4 power supply and external parts that compose a low pass filter. Table 2-13 shows the recommended parameters of VDD18_CPGPLL4 power supply circuit component.

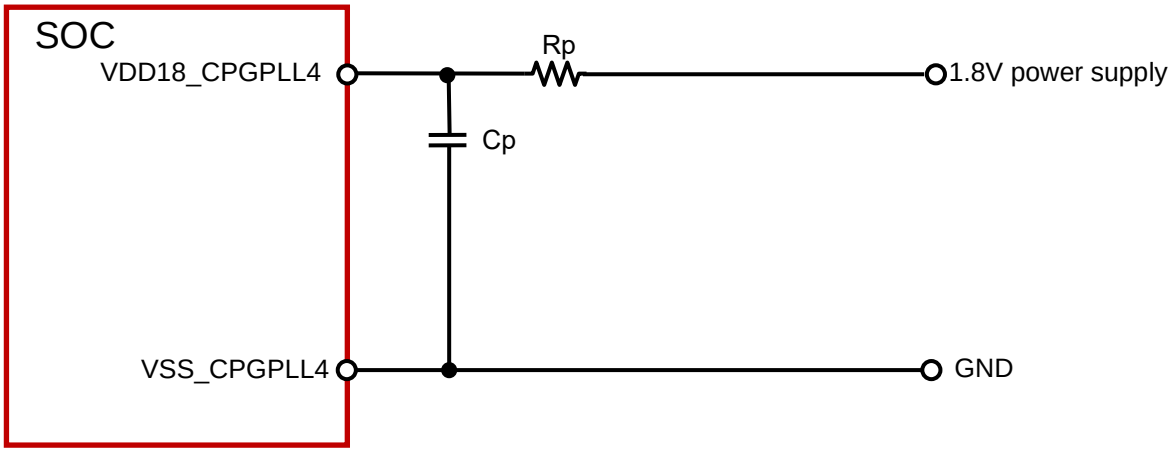


Figure 2-13 Circuit diagram of VDD18_CPGPLL4 power supply and external parts

Table 2-13 Recommended parameters of VDD18_CPGPLL4 power supply circuit component

Pin name	Low pass filter	Loop Inductance	Note
VDD18_CPGPLL4	Cp=1uF Rp=1ohm	Less than 4.30nH	Refer to “Appendix. Concept of Loop Inductance”

Please also check the specifications on PMIC side.

2.14 VDD18_CPGPLL5 Power Supply

Specifications for the design of power supply circuits for VDD18_CPGPLL5 are given below.

- RC-filter is strongly recommended because PLL is very sensitive for power noise.
- Place each bypass capacitors as close to SoC as possible.
- Place the bypass capacitors on the BGA ball side and the resistance beyond it.
- Be careful of crosstalk when resistance leaves SoC.

Figure 2-14 shows a circuit diagram image of VDD18_CPGPLL5 power supply and external parts that compose a low pass filter. Table 2-14 shows the recommended parameters of VDD18_CPGPLL5 power supply circuit component.

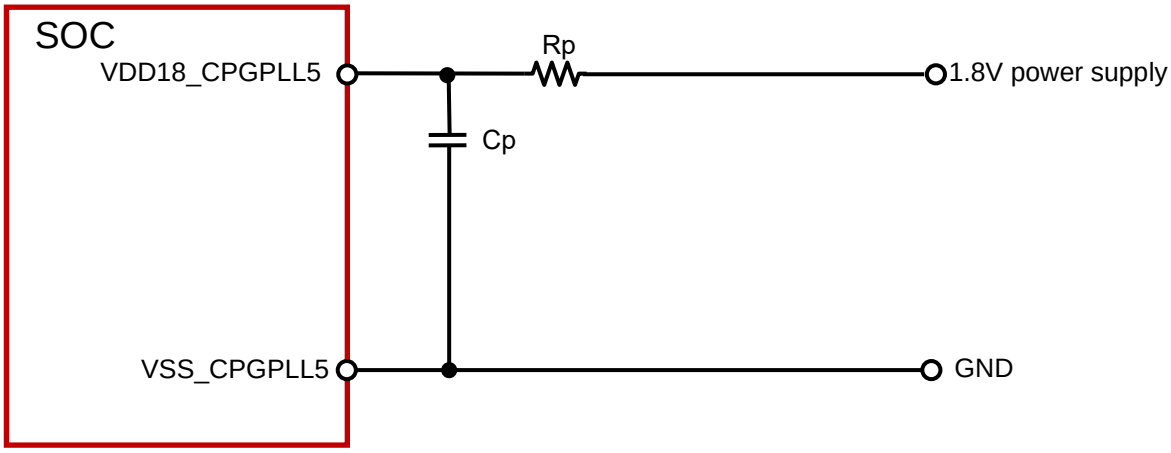


Figure 2-14 Circuit diagram of VDD18_CPGPLL5 power supply and external parts

Table 2-14 Recommended parameters of VDD18_CPGPLL5 power supply circuit component

Pin name	Low pass filter	Loop Inductance	Note
VDD18_CPGPLL5	Cp=1uF Rp=1ohm	Less than 4.30nH	Refer to “Appendix. Concept of Loop Inductance”

Please also check the specifications on PMIC side.

2.15 VDD18_CPGPLL6 Power Supply

Specifications for the design of power supply circuits for VDD18_CPGPLL6 are given below.

- LC-filter is strongly recommended because PLL is very sensitive for power noise.
- Place each bypass capacitors as close to SoC as possible.
- Place the bypass capacitors on the BGA ball side and the inductance beyond it.
- Be careful of crosstalk when resistance leaves SoC.

Figure 2-15 shows a circuit diagram image of VDD18_CPGPLL6 power supply and external parts that compose a low pass filter. Table 2-15 shows the recommended parameters of VDD18_CPGPLL6 power supply circuit component.

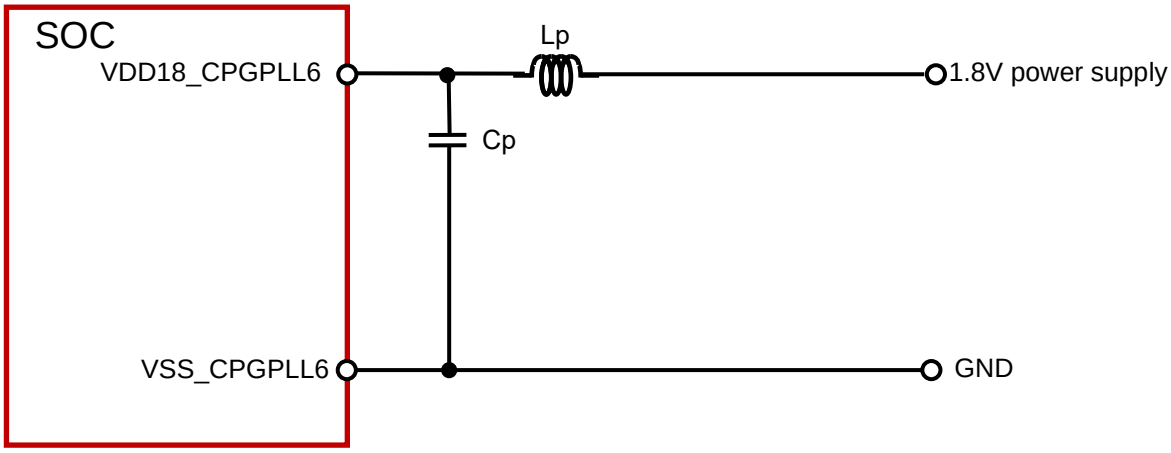


Figure 2-15 Circuit diagram of VDD18_CPGPLL6 power supply and external parts

Table 2-15 Recommended parameters of VDD18_CPGPLL6 power supply circuit component

Pin name	Low pass filter	Loop Inductance	Note
VDD18_CPGPLL6	Cp=1uF Lp=2nH	Less than 4.00nH	Refer to “Appendix. Concept of Loop Inductance”

Please also check the specifications on PMIC side.

2.16 VDD18_CPGPLL7 Power Supply

Specifications for the design of power supply circuits for VDD18_CPGPLL7 are given below.

- RC-filter is strongly recommended because PLL is very sensitive for power noise.
- Place each bypass capacitors as close to SoC as possible.
- Place the bypass capacitors on the BGA ball side and the resistance beyond it.
- Be careful of crosstalk when resistance leaves SoC.

Figure 2-16 shows a circuit diagram image of VDD18_CPGPLL7 power supply and external parts that compose a low pass filter. Table 2-16 shows the recommended parameters of VDD18_CPGPLL7 power supply circuit component.

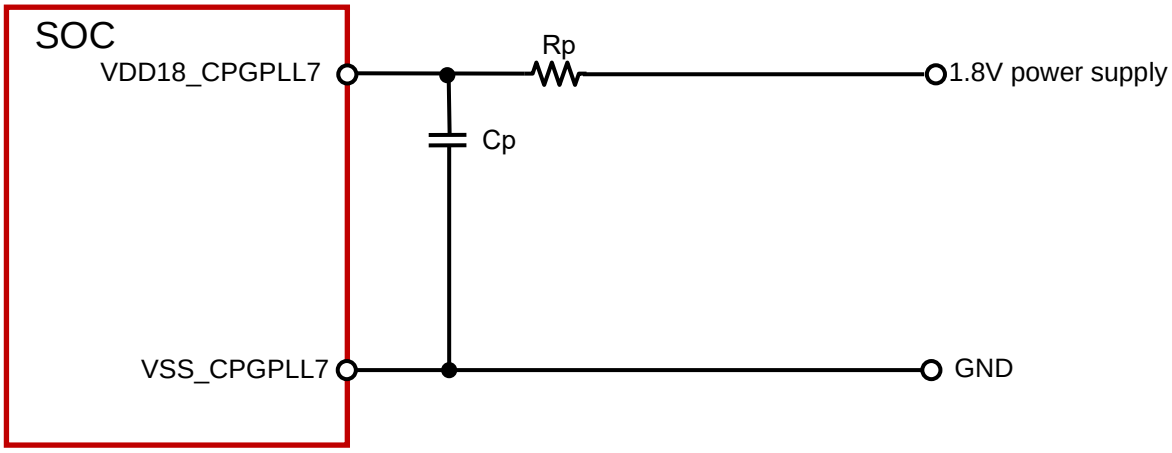


Figure 2-16 Circuit diagram of VDD18_CPGPLL7 power supply and external parts

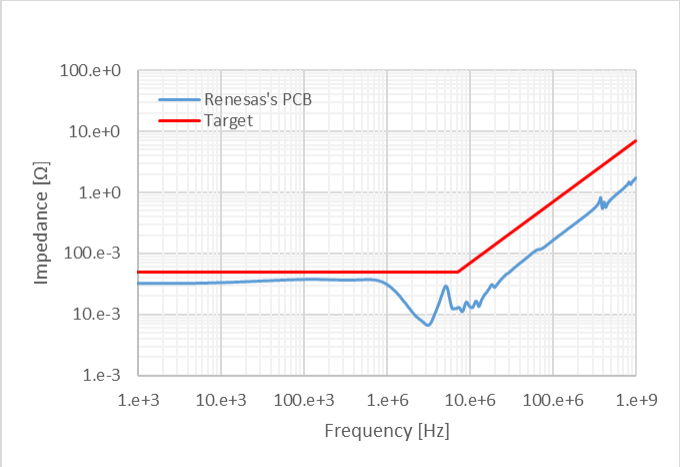
Table 2-16 Recommended parameters of VDD18_CPGPLL7 power supply circuit component

Pin name	Low pass filter	Loop Inductance	Note
VDD18_CPGPLL7	Cp=1uF Rp=1ohm	Less than 4.30nH	Refer to “Appendix. Concept of Loop Inductance”

Please also check the specifications on PMIC side.

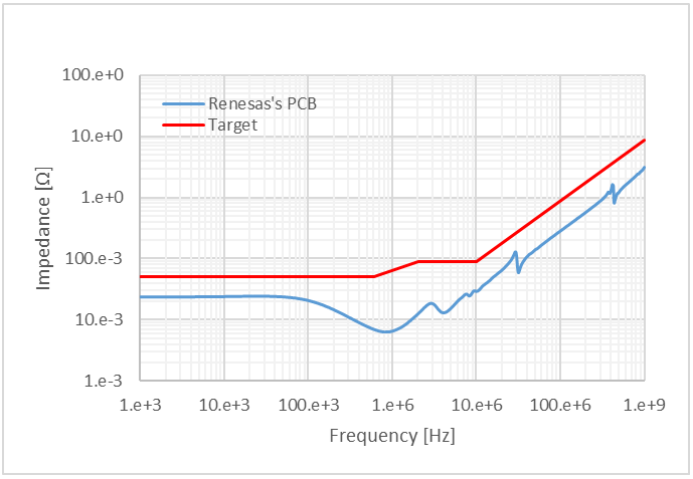
Appendix-A Target impedance on PCBs for IO power supply

Target impedance of PCB are shown below.



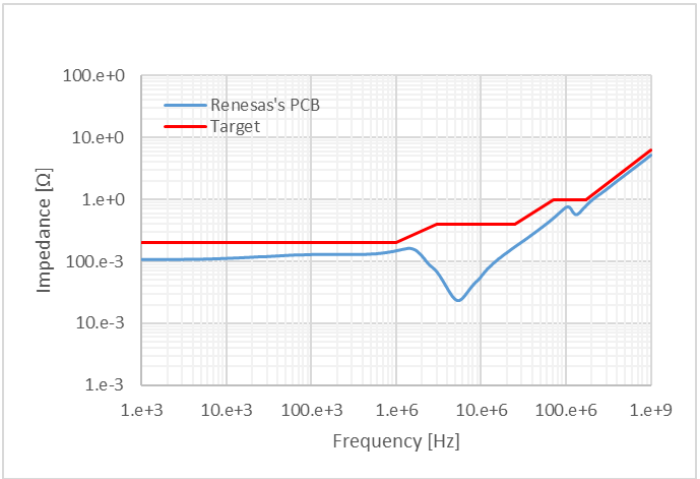
Freq [Hz]	Impedance [ohm]
1.00e+3	50.00e−3
7.15e+6	50.00e−3
1.00e+9	7.00e+0

Figure A-1 Target impedance on PCBs for VDDQ18



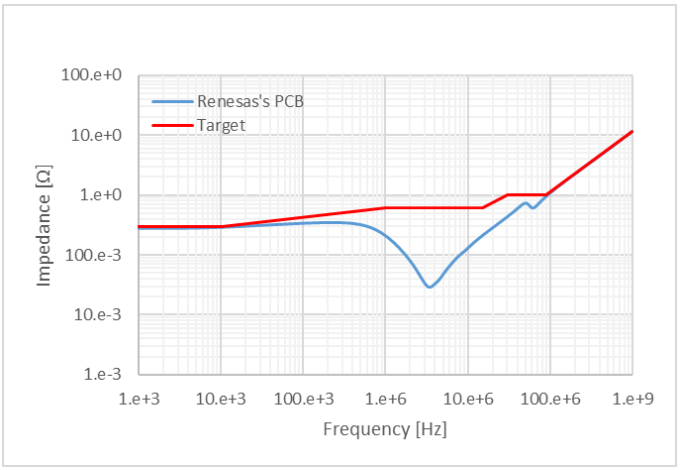
Freq [Hz]	Impedance [ohm]
1.00e+3	50.00e−3
600.00e+3	50.00e−3
2.00e+6	88.00e−3
10.00e+6	88.00e−3
1.00e+9	8.80e+0

Figure A-2 Target impedance on PCBs for VDDQ33



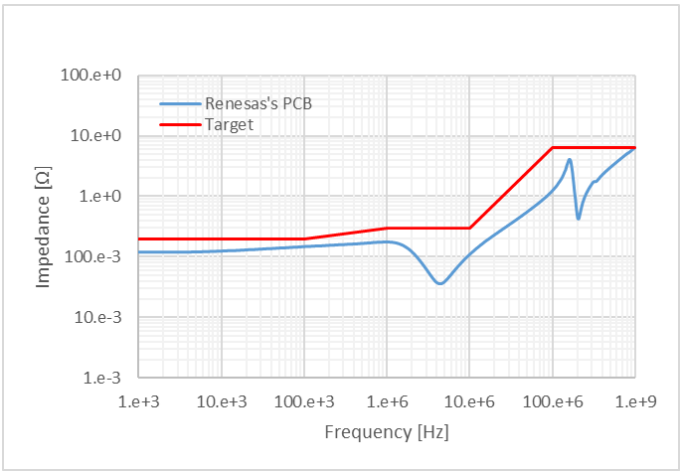
Freq [Hz]	Impedance [ohm]
1.00e+3	200.00e−3
1.00e+6	200.00e−3
3.00e+6	400.00e−3
25.00e+6	400.00e−3
70.00e+6	1.00e+0
170.00e+6	1.00e+0
1.00e+9	6.30e+0

Figure A-3 Target impedance on PCBs for VDDQ18_33_SPI



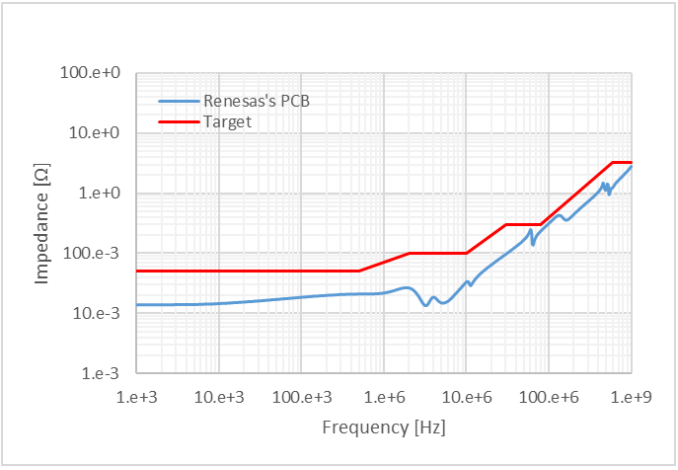
Freq [Hz]	Impedance [ohm]
1.00e+3	300.00e-3
10.00e+3	300.00e-3
1.00e+6	600.00e-3
15.00e+6	600.00e-3
30.00e+6	1.00e+0
90.00e+6	1.00e+0
1.00e+9	11.50e+0

Figure A-4 Target impedance on PCBs for VDDQ18_33_I2C



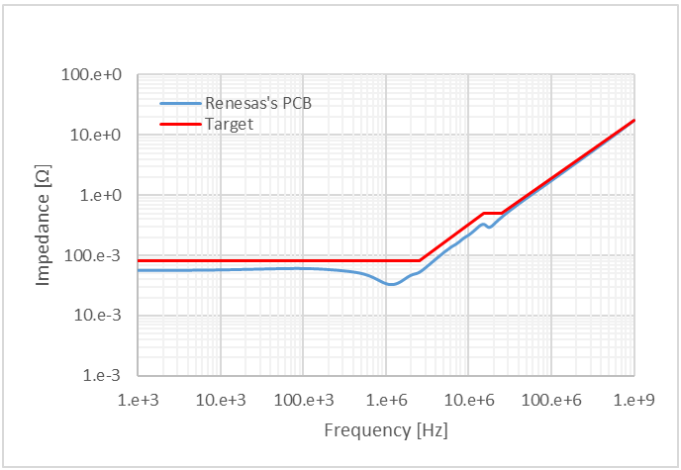
Freq [Hz]	Impedance [ohm]
1.00e+3	200.00e-3
100.00e+3	200.00e-3
1.00e+6	300.00e-3
10.00e+6	300.00e-3
100.00e+6	6.30e+0
1.00e+9	6.30e+0

Figure A-5 Target impedance on PCBs for VDDQ18_33_SDHI



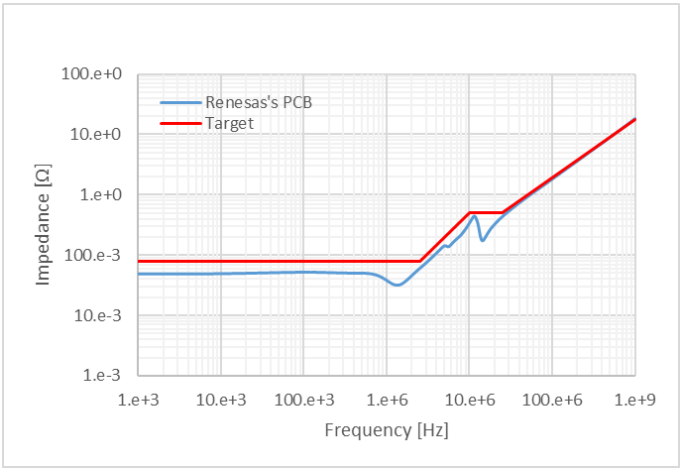
Freq [Hz]	Impedance [ohm]
1.00e+3	50.00e-3
500.00e+3	50.00e-3
2.00e+6	100.00e-3
10.00e+6	100.00e-3
30.00e+6	300.00e-3
80.00e+6	300.00e-3
600.00e+6	3.30e+0
1.00e+9	3.30e+0

Figure A-6 Target impedance on PCBs for VDDQ18_25_AVB



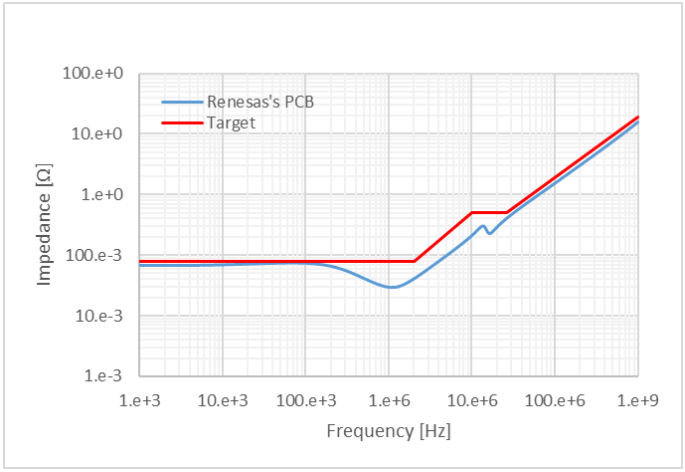
Freq [Hz]	Impedance [ohm]
1.00e+3	80.00e−3
2.50e+6	80.00e−3
15.00e+6	500.00e−3
25.00e+6	500.00e−3
1.00e+9	17.60e+0

Figure A-7 Target impedance on PCBs for VDD18_TRNG



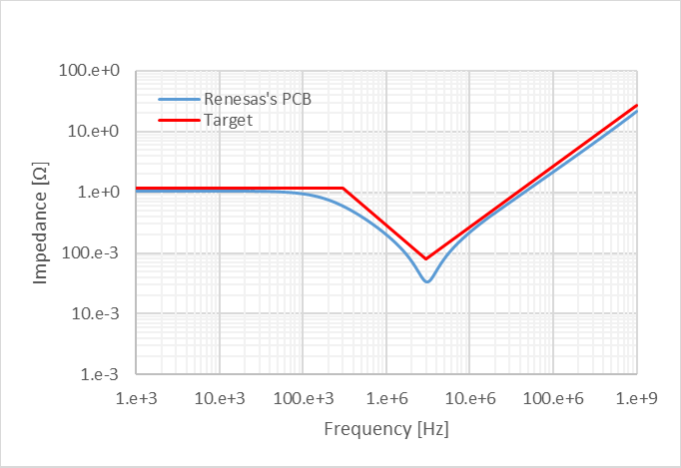
Freq [Hz]	Impedance [ohm]
1.00e+3	80.00e−3
2.50e+6	80.00e−3
10.00e+6	500.00e−3
25.00e+6	500.00e−3
1.00e+9	17.60e+0

Figure A-8 Target impedance on PCBs for VDD18_OCO



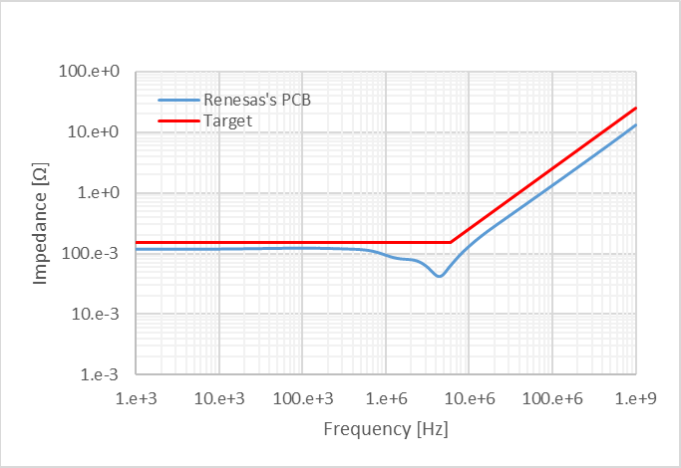
Freq [Hz]	Impedance [ohm]
1.00e+3	80.00e−3
2.00e+6	80.00e−3
10.00e+6	500.00e−3
26.50e+6	500.00e−3
1.00e+9	18.86e+0

Figure A-9 Target impedance on PCBs for VDD18_OTP



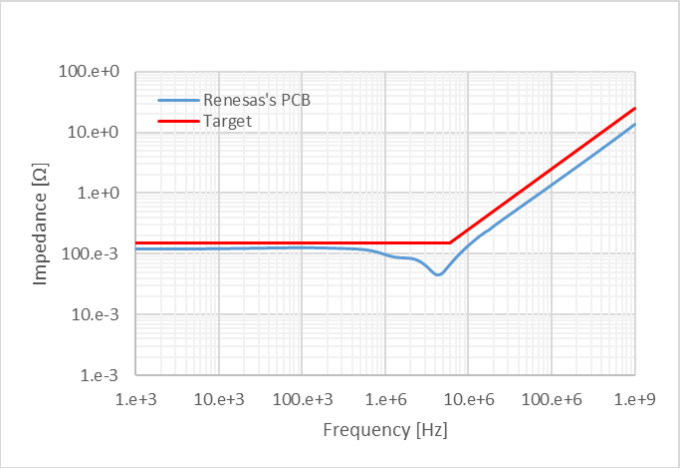
Freq [Hz]	Impedance [ohm]
1.00e+3	1.15e+0
300.00e+3	1.15e+0
3.00e+6	81.00e−3
1.00e+9	27.00e+0

Figure A-10 Target impedance on PCBs for VDD18_CPGPLL1



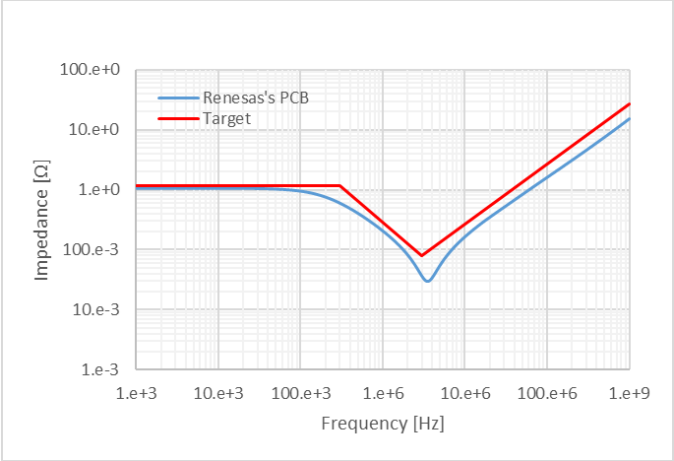
Freq [Hz]	Impedance [ohm]
1.00e+3	150.00e−3
5.97e+6	150.00e−3
1.00e+9	25.15e+0

Figure A-11 Target impedance on PCBs for VDD18_CPGPLL2



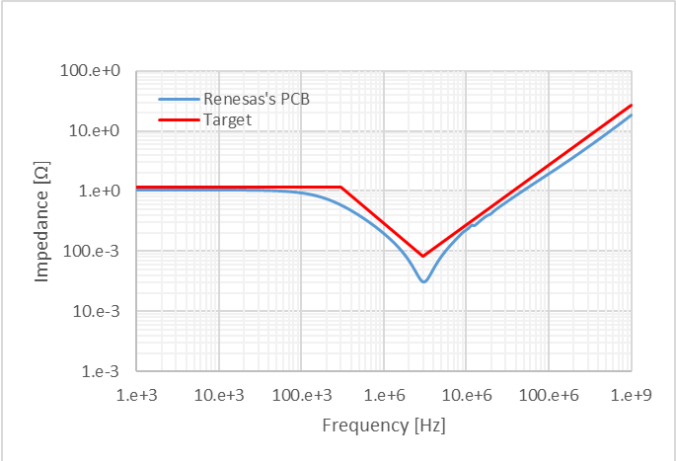
Freq [Hz]	Impedance [ohm]
1.00e+3	150.00e−3
5.97e+6	150.00e−3
1.00e+9	25.15e+0

Figure A-12 Target impedance on PCBs for VDD18_CPGPLL3



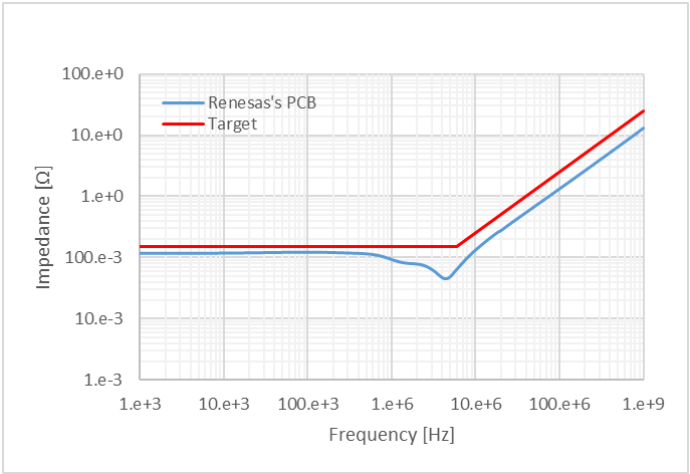
Freq [Hz]	Impedance [ohm]
1.00e+3	1.15e+0
300.00e+3	1.15e+0
3.00e+6	81.00e−3
1.00e+9	27.00e+0

Figure A-13 Target impedance on PCBs for VDD18_CPGPLL4



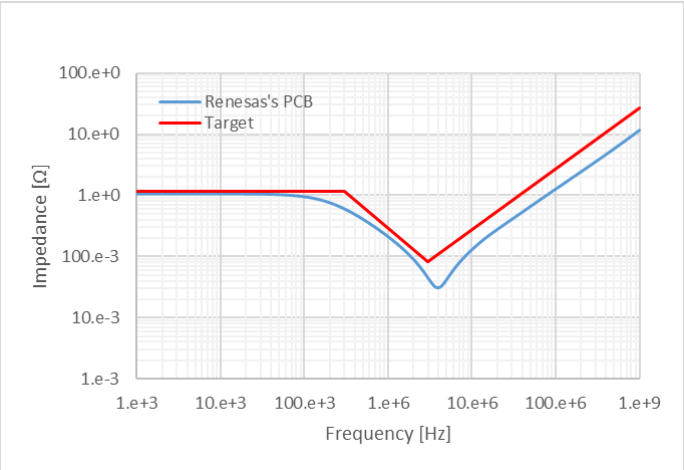
Freq [Hz]	Impedance [ohm]
1.00e+3	1.15e+0
300.00e+3	1.15e+0
3.00e+6	81.00e−3
1.00e+9	27.00e+0

Figure A-14 Target impedance on PCBs for VDD18_CPGPLL5



Freq [Hz]	Impedance [ohm]
1.00e+3	150.00e−3
5.97e+6	150.00e−3
1.00e+9	25.15e+0

Figure A-15 Target impedance on PCBs for VDD18_CPGPLL6



Freq [Hz]	Impedance [ohm]
1.00e+3	1.15e+0
300.00e+3	1.15e+0
3.00e+6	81.00e−3
1.00e+9	27.00e+0

Figure A-16 Target impedance on PCBs for VDD18_CPGPLL7

Appendix-B Concept of Loop inductance and Impedance

The loop inductance and impedance can be obtained by calculating the inductance and impedance from the VDD ball of the package to the VSS balls of the package. Consider the VSS balls of the package as an ideal GND in the way shown in the figure below. Bypass Capacitor Models should include the ESL and the ESR.

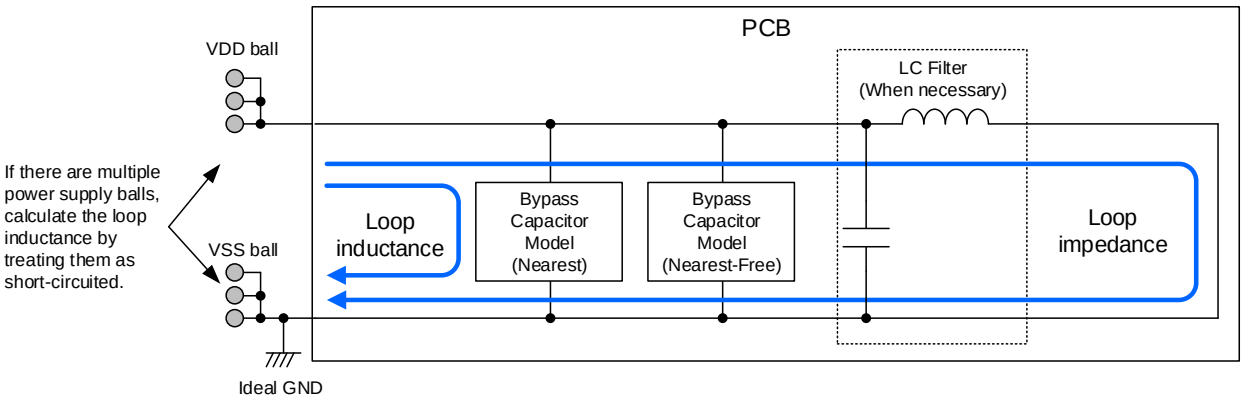


Figure B-1 Loop inductance and impedance on PCBs for IO power supply

Revision History

Rev.	Date	Description	
		Page	Summary
0.50	2022/09/30	-	Newly issued as preliminary version.
0.90	2023/01/31		Updated:
		9	■ Loop Inductance of VDDQ18_33_SPI power supply is updated: Table 2-3 Recommended parameters of VDDQ18_33_SPI power supply circuit component
		10	■ Loop Inductance of VDDQ18_33_I2C power supply is updated: Table 2-4 Recommended parameters of VDDQ18_33_I2C power supply circuit component
		11	■ Loop Inductance of VDDQ18_33_SDHI power supply is updated: Table 2-5 Recommended parameters of VDDQ18_33_SDHI power supply circuit component
		23	■ Target impedances on PCBs are updated: Figure A-1 Target impedances on PCBs for VDDQ18 Figure A-2 Target impedances on PCBs for VDDQ33
		24	Figure A-3 Target impedances on PCBs for VDDQ18_33_SPI Figure A-4 Target impedances on PCBs for VDDQ18_33_I2C Figure A-5 Target impedances on PCBs for VDDQ18_33_SDHI Figure A-6 Target impedances on PCBs for VDDQ18_25_AVB
1.00	2025/03/17	-	Updated: ■ Upgrade to revision 1.00.

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The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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