R-Car V4M

Initialization Sequence of LPDDR4X interface

Introduction

This application note explains the sequence of initializing the LPDDR4X interface in R-Car V4M series products. And this document will provide programing guide on the initialization sequence of LPDDR4X interface.

Renesas has confirmed that the flow of initialization and register settings provided in this document will correctly initialize the LPDDR4X interface.

Note that this document applies to R-Car V4M device. The specifications of other R-Car V4M series products may differ from those described in this document.

Target Device

- R-Car V4M-7
- R-Car V4M-5
- R-Car V4M-3
- R-Car V4M-2

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1. Introduction

1.1 Overview

This application note describes the initialization sequence of LPDDR4X interface. Supported products and version (Ver.) are listed in Table 1-1. SoC means the following supported products in this document. Supported LPDDR4X initialization code revision is listed in the Table 1-2.

Table 1-1 Supported products

Products	Ver.
R-Car V4M	Ver.1.0, Ver.2.0.

Table 1-2 Supported code revision

Code revision
1.00_lp4x

This application note consists of the following chapters:

- Chapter 1 describes register access and its notation used in this document.
- Chapter 2 describes the entire flow of initialization sequence.
- Chapter 3 describes the hardware configuration setting.
- Chapter 4 describes the main flow of initialization sequence.
- Chapter 5 lists the registers used in the sequence.
- Appendix lists the concrete examples of configuration values.

In this document, the word “initialization sequence” means “activation sequence” in Reference [3].

1.2 Register Access and its Notation

This section explains how to access the DBSC, DRAM, and PHY registers in the sequence of initializing the LPDDR4X interface.

Access to the DBSC is the same as access to registers in general, see section 1.2.1. However, access to the DRAM and PHY (in an SoC) registers requires a special manner. Specifically, access to these registers is through the DBSC.

Access to the DRAM proceeds in response to DRAM commands through access to the DBSC_DBCMD register, see section 1.2.2.

Access to the PHY registers (to set PHY parameters) is through access to the DBSC_DBPDRGA, DBSC_DBPDRGD, and DBSC_DBPDRGM registers, see section 1.2.3.

The registers of the DBSC and PHY are referred to with names of the form DBSC_* and DDR_* for clarity, and their addresses and the names of their bits and bit fields are listed in chapter 5 respectively.

For the details on setting of the DBSC registers, see Reference [3].

A description of the columns of the table is given below.

Op.:	Operation with the register. R: Reading W: Writing
Register Name:	Name of the register.
Bit:	The number of the bit or range of the bit field which is relevant to the operation.
Bit Name:	The name of the bit or bit field which is relevant to the operation.
Data:	The type of value of the bit field for the operation.
Description:	Register description, explanation of values, etc.

1.2.1 Access to DBSC Registers

DBSC register access is explained. General register (Registers listed in section 5.3.) can be accessed by similar way. Table 1-3 is for the case of register write access (32-bit access) to DBSC_DBPDLK{m_1}. Table 1-4 is for the case of register read access to DBSC_DBTR(24).

For DBSC registers with the following indices, a range of indices that is appropriate to the user system must be selected.

{m_1} indicates a memory channel number (DDRPHY channel number) = 0 to 1.
{n_2} indicates a rank number = 0 to 1.

The specification of a bit or bit field in Table 1-3 means a write operation for the corresponding bit or bit field. And the specification of a bit or bit field in Table 1-4 means a read operation for the corresponding bit or bit field.

The registers used in the initialization sequence are listed in chapter 5.

Table 1-3 Register Writing (32-Bit Access)

Op.	Register Name	Bit	Bit Name	Data	Description
W	DBSC_DBPDLK{m_1}	—	—	0x0000A55A	Register write (32-bit access)

Table 1-4 Register Reading (32-Bit Access)

Op.	Register Name	Bit	Bit Name	Data	Description
R	DBSC_DBTR(24)	—	—	reg_data	Register read (32-bit access)

1.2.2 Access to DRAM Registers

Access to the DRAM registers is handled as follows. DRAM commands can be issued by access to the DBSC_DBCMD register as in Table 1-5. The meanings of each of the columns are described in section 1.2.1.

Table 1-5 DRAM Command Write Access

Op.	Register Name	Bit	Bit Name	Data	Description
R	DBSC_DBCMD	—	—	—	Dummy read
R	DBSC_DBWAIT	[0]	BUSY	wait	Wait until the “wait” bit becomes 0.
W	DBSC_DBCMD	[31:24]	OPC	cmd	“cmd” corresponds to a DRAM command. For details, see Reference [3].
		[23:20]	CH		
		[18:16]	RANK		
		[15:0]	ARG		

1.2.3 Access to PHY Registers

PHY parameters are assigned to bits and bit fields of the PHY registers, and access to the PHY registers is through access to the DBSC_DBPDRGA, DBSC_DBPDRGD, and DBSC_DBPDRGM registers.

In this document, notations of write/read access to PHY parameter are shown in Table 1-6/Table 1-9 respectively.

Table 1-6 Writing PHY Parameters

Op.	Register Name	Bit	Bit Name	Data	Description
W	DDR_Z	[x:y]	PHY_param_z	w_data	Write access to “PHY_param_z” assigned to bits [x:y] of PHY register “DDR_Z”.

Table 1-6 means the sequence shown in Table 1-7 and Table 1-8. For the meanings of each of the columns, see section 1.2.1.

The sequence shown in Table 1-7 is only used for Setting initial values of PHY registers in Table 4-22, Table 4-23, Table 4-24, and Table 4-25. On the other hand, the sequence shown in Table 1-8 is used for Setting values of PHY registers other than the above. The sequence in Table 1-8 is masked write of PHY registers using the DBSC function.

Table 1-7 Writing PHY Parameters (in Details)

Op.	Register Name	Bit	Bit Name	Data	Description
W	DBSC_DBPDRGA{m_1}	[15:0]	PRA{m_1}	phy_reg_adr	Write to “DDR_Z” register address “phy_reg_adr”.
R	DBSC_DBPDRGA{m_1}	[15:0]	PRA{m_1}	adr	Wait for “adr” and “phy_reg_adr” to be equal.
W	DBSC_DBPDRGD{m_1}	[31:0]	PRD{m_1}	phy_w_data	Write 32-bit "phy_w_data" containing multiple parameters.
R	DBSC_DBPDRGA{m_1}	[15:0]	PRA{m_1}	adr	Wait for “adr” and “phy_reg_adr | 0x00008000” to be equal.
W	DBSC_DBPDRGA{m_1}	[15:0]	PRA{m_1}	phy_reg_adr | 0x00008000	Write “DDR_Z” register address “phy_reg_adr” and “status bit”.
R	DBSC_DBPDRGA{m_1}	[15:0]	PRA{m_1}	adr	Wait for “adr” and “phy_reg_adr” to be equal.
W	DBSC_DBPDRGA{m_1}	[15:0]	PRA{m_1}	phy_reg_adr	Write to “DDR_Z” register address “phy_reg_adr”.

Table 1-8 Writing PHY Parameters with Masked Write (in Details)

Op.	Register Name	Bit	Bit Name	Data	Description
W	DBSC_DBPDRGM{m_1}	[3:0]	PRM{m_1}	phy_w_msk	Write "phy_w_msk", which is the setting of 8bit masks to prevent overwriting except for bits [x:y].
R	DBSC_DBPDRGM{m_1}	[3:0]	PRM{m_1}	msk	Wait for “msk” and “phy_w_mask” to be equal.
W	DBSC_DBPDRGA{m_1}	[15:0]	PRA{m_1}	phy_reg_adr	Write to “DDR_Z” register address “phy_reg_adr”.
R	DBSC_DBPDRGA{m_1}	[15:0]	PRA{m_1}	adr	Wait for “adr” and “phy_reg_adr” to be equal.
W	DBSC_DBPDRGD{m_1}	[31:0]	PRD{m_1}	phy_w_data	Write "phy_w_data", which is the data assigned "w_data" to bit [x:y].
R	DBSC_DBPDRGA{m_1}	[15:0]	PRA{m_1}	adr	Wait for “adr” and “phy_reg_adr | 0x00008000” to be equal.
W	DBSC_DBPDRGA{m_1}	[15:0]	PRA{m_1}	phy_reg_adr | 0x00008000	Write “DDR_Z” register address “phy_reg_adr” and “status bit”.
R	DBSC_DBPDRGA{m_1}	[15:0]	PRA{m_1}	adr	Wait for “adr” and “phy_reg_adr” to be equal.
W	DBSC_DBPDRGA{m_1}	[15:0]	PRA{m_1}	phy_reg_adr	Write to “DDR_Z” register address “phy_reg_adr”.
W	DBSC_DBPDRGM{m_1}	[3:0]	PRM{m_1}	0x0	Clear the mask settings.
R	DBSC_DBPDRGM{m_1}	[3:0]	PRM{m_1}	msk	Wait for “msk” and “0x0” to be equal.

Table 1-9 Reading PHY Parameter

Op.	Register Name	Bit	Bit Name	Data	Description
R	DDR_Z	[x:y]	PHY_param_z	r_data	Read access to PHY parameter assigned to bits [x:y] of PHY register.

Table 1-9 means the sequence shown in Table 1-10. For the meanings of each of the columns, see section 1.2.1.

Table 1-10 Reading PHY Parameters (in Details)

Op.	Register Name	Bit	Bit Name	Data	Description
W	DBSC_DBPDRGA{m_1}	[15:0]	PRA{m_1}	phy_reg_adr | 0x00004000	Write to “DDR_Z” register address “phy_reg_adr” and “status bit”.
R	DBSC_DBPDRGA{m_1}	[15:0]	PRA{m_1}	adr	Wait for “adr” and “phy_reg_adr | 0x0000C000” to be equal.
R	DBSC_DBPDRGA{m_1}	[15:0]	PRA{m_1}	—	Dummy read
W	DBSC_DBPDRGA{m_1}	[15:0]	PRA{m_1}	phy_reg_adr | 0x00008000	Write to “DDR_Z” register address “phy_reg_adr” and “status bit”.
R	DBSC_DBPDRGA{m_1}	[15:0]	PRA{m_1}	adr	Wait for “adr” and “phy_reg_adr” to be equal.
W	DBSC_DBPDRGA{m_1}	[15:0]	PRA{m_1}	phy_reg_adr | 0x00008000	Write to “DDR_Z” register address “phy_reg_adr” and “status bit”.
R	DBSC_DBPDRGA{m_1}	[15:0]	PRA{m_1}	adr	Wait for “adr” and “phy_reg_adr” to be equal.
R	DBSC_DBPDRGD{m_1}	[31:0]	PRD{m_1}	phy_r_data	Read “DDR_Z” register value “phy_r_data”. The value in bits [x:y] of “phy_r_data” is returned as “r_data”.

Note: On “Bit Name”, “Register Name”, and “Bit” for PHY register

In the case of the PHY parameters, some items listed under “Register Name” and “Bit” differ with the product group. “Register Name” and “Bit” are omitted in succeeding sections. Instead, a table of correspondences between “Bit Name”, “Register Name”, and “Bit” is given in section 5.2.

2. Overall Flow of Initialization

This chapter explains the overall flow of initialization. Figure 2-1 gives flowcharts of the procedure, which is divided into the five steps outlined below.

1. Unlock the DBSC register
   This part sets access unlock to the DBSC register, see Table 2-1.
2. Configuration Settings
   This part is hardware configuration setting part. The code depends on your own hardware environment. See chapter 3.
3. Initial PLL3 Setting
   This part is the Initial PLL3 Setting, see Appendix A2.
4. Main flow of initialization
   This part is the main part of initialization sequence. Based on hardware configuration setting, initialization for DBSC and PHY are performed. See chapter 4.
5. Lock the DBSC register
   This part sets access lock to the DBSC register, see Table 2-2.

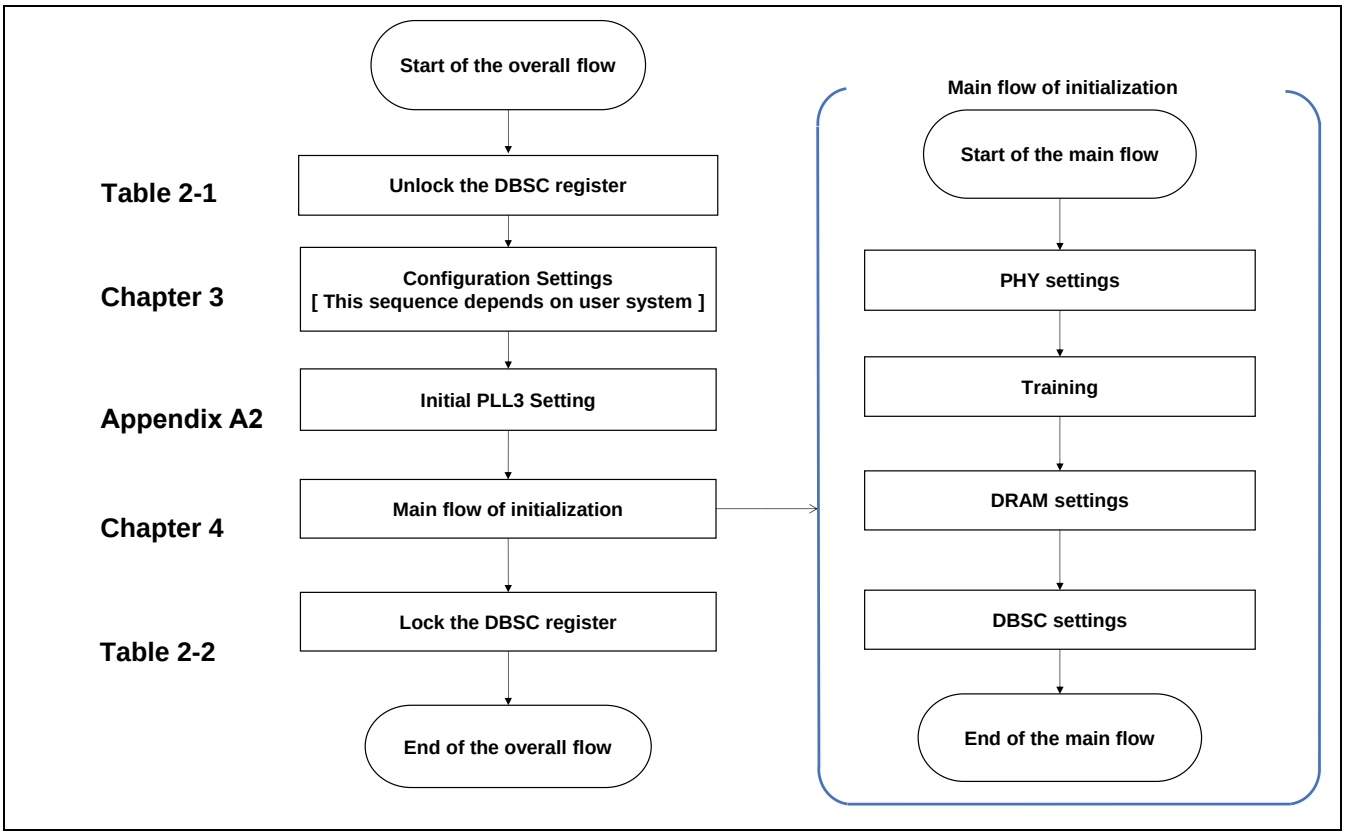


Figure 2-1 Overall Flow of Initialization

Renesas has confirmed that the flow of initialization and register settings provided will correctly initialize the LPDDR4X-SDRAM interface.

2.1 Unlocking the DBSC Register

Table 2-1 Unlocking the DBSC register

Op.	Register Name	Bit	Bit Name	Data	Description
W	DBSC_DBSYSCNT0	[15:0]	REGLOCK	0x00001234	Unlocks the DBSC register against access. See Reference [3].
W	DBSC_DBSYSCNT0A	[15:0]	REGLOCK	0x00001234	Unlocks the DBSC register against access. See Reference [3].

2.2 Locking the DBSC Register

Table 2-2 Locking the DBSC register

Op.	Register Name	Bit	Bit Name	Data	Description
W	DBSC_DBSYSCNT0	[15:0]	REGLOCK	0x00000000	Locks the DBSC register against access. See Reference [3].
W	DBSC_DBSYSCNT0A	[15:0]	REGLOCK	0x00000000	Locks the DBSC register against access. See Reference [3].

3. Configuration Settings

This chapter covers the hardware configuration settings. The code depends on your own hardware environment. Figure 3-1 is a flowchart of the configuration settings. The individual blocks in the diagram are explained in section 3.1 to section 3.6.

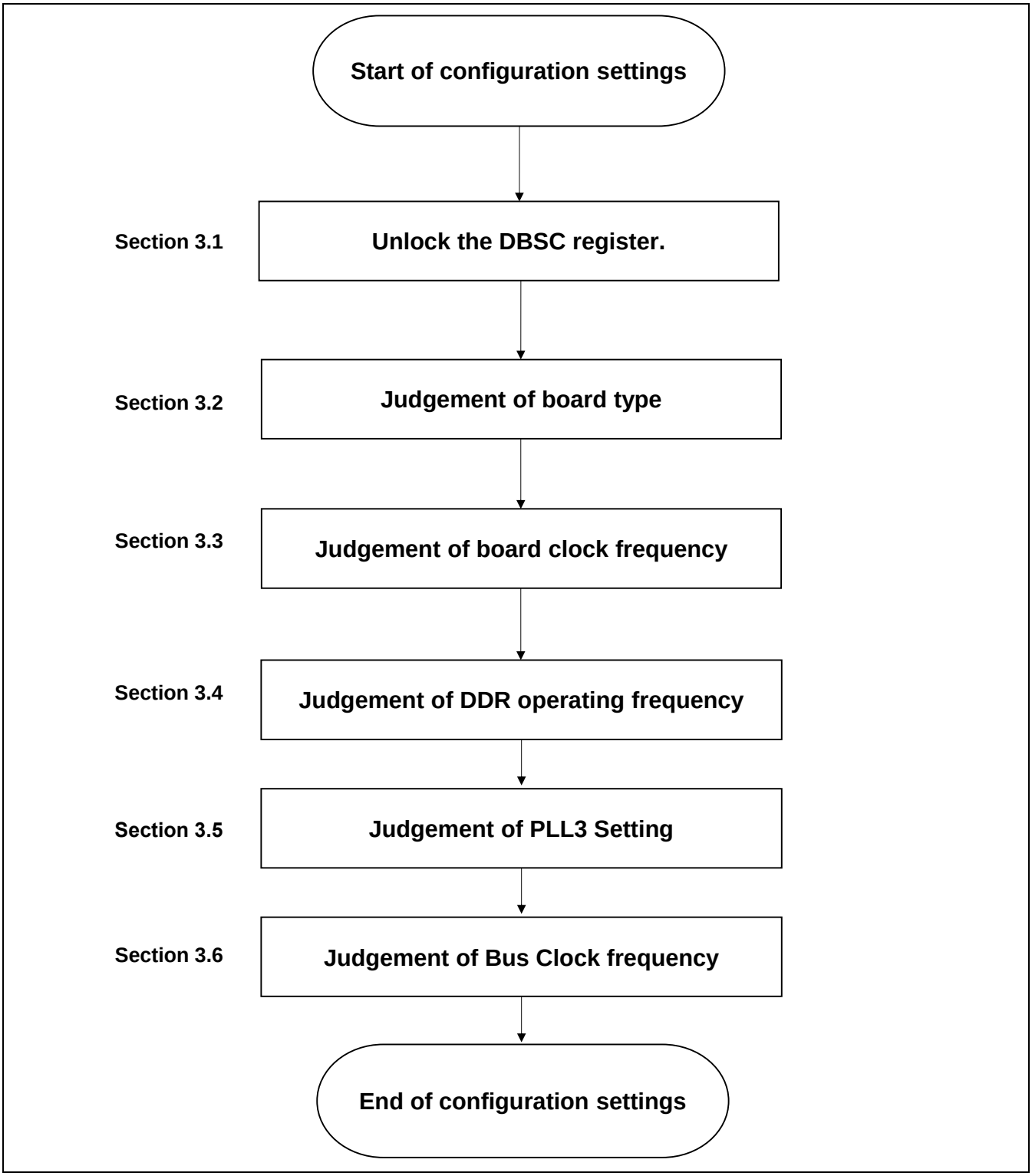


Figure 3-1 Flow of Configuration Settings

3.1 Judgement of Product and its Version

[This sequence depends on user system]

Reading from the product revision register (PRR) returns a value that indicates the type of product and the version number of the SoC as shown in Table 3-1.

Table 3-1 Reading the Product Revision Register (PRR)

Op.	Register Name	Bit	Bit Name	Data	Description
R	PRR	—	—	dataL	Bit[14:8] of “dataL” indicate the product type: V4M: 0x5D. Bit[7:0] of “dataL” indicate the version number: Ver.1.0: 0x00, Ver.2.0: 0x10. See Reference [3].

3.2 Judgement of Board Type

[This sequence depends on user system]

Initialization sequence depends on configuration of the board you use (swap configuration and so on). For details of the settings, see Appendix A1.1.

3.3 Judgement of Board Clock Frequency

[This sequence depends on user system]

Initialization sequence depends on configuration of the board clock frequency you use. The board clock frequency, namely, EXTAL input frequency[MHz] in Reference [3] is defined as xtal_clk in this document. As Code, this value can be realized by using two integers as: xtal_clk = brd_clk / brd_clkdiv (e.g., 50/3 = 16.66).

Table 3-2 Configuration of Board Clock Frequency (Examples)

Mode Monitor Register 0 (MODEMR0) MD14, MD13	brd_clk	brd_clkdiv	brd_clkdiva	xtal_clk (MHz)
0, 0	50	3	0	16.66
0, 1	60	3	0	20
1, 0	—	—	—	—
1, 1	100	3	1	33.33

Note: MD14=1 and MD13=0 settings are prohibited for V4M.

3.4 Judgement of DDR Operating Frequency

[This sequence depends on user system]

Initialization sequence depends on configuration of the DDR clock frequency you use. The DDR clock frequency, namely, LPDDR4X-DRAM access speed [MT/s] is defined as ddr_mts in this document. As Code, this value can be realized by using two integers as: ddr_mts = ddr_mbps / ddr_mbpsdiv (e.g., 12800/3 = 4266). Table 3-3, Table 3-4, Table 3-5, and Table 3-6 show the configuration value of the DDR Clock Frequency for each V4M Variant. The product ID of each V4M Variant can be referenced from the identification register (OTPMONITOR17). For details, see Reference [3].

Additionally, the medium frequency settings can be disabled in case of not using DFS(Dynamic Frequency Scaling) function at Low-Power Mode. (med_freq_en = 1: medium frequency settings are enabled. med_freq_en = 0: medium frequency settings are disabled.) For details of DFS function, see Reference [3] and DFS documentation.

Table 3-3 Configuration Value for DDR Clock Frequency (V4M-7: OTPMONITOR17 = 0x00)

Mode Monitor Register 0,1 (MODEMR0, MODEMR1) MD18, MD37, MD36	Mode Monitor Register 0 (MODEMR0) MD19, MD17	ddr_mbps	ddr_mbpsdiv	ddr_mts	med_freq_en
0,0,0	0,0	12800	3	4266	1
	0,1	11200	3	3733	1
	1,0	3200	1	3200	1
	1,1	6400	3	2133	0
0,0,1	0,0	12800	3	4266	1
	0,1	11200	3	3733	1
	1,0	3200	1	3200	1
	1,1	6400	3	2133	0
0,1,0	0,0	12800	3	4266	1
	0,1	11200	3	3733	1
	1,0	3200	1	3200	1
	1,1	6400	3	2133	0
0,1,1	0,0	12800	3	4266	1
	0,1	11200	3	3733	1
	1,0	3200	1	3200	1
	1,1	6400	3	2133	0
1,0,0	0,0	12800	3	4266	1
	0,1	11200	3	3733	1
	1,0	3200	1	3200	1
	1,1	6400	3	2133	0
1,0,1	0,0	12800	3	4266	1
	0,1	11200	3	3733	1
	1,0	3200	1	3200	1
	1,1	6400	3	2133	0
1,1,0	0,0	12800	3	4266	1
	0,1	11200	3	3733	1
	1,0	3200	1	3200	1
	1,1	6400	3	2133	0
1,1,1	0,0	12800	3	4266	1
	0,1	11200	3	3733	1
	1,0	3200	1	3200	1
	1,1	6400	3	2133	0

Note: See Reference [3] for supported DDR Clock Frequency. And, See Reference [4] for how to change DDR Clock Frequency. Furthermore, refer to Reference [3] and DFS documentation for supported DDR Clock Frequency at Low-Power Mode.

Table 3-4 Configuration Value for DDR Clock Frequency (V4M-5: OTPMONITOR17 = 0x01)

Mode Monitor Register 0,1 (MODEMR0, MODEMR1) MD18, MD37, MD36	Mode Monitor Register 0 (MODEMR0) MD19, MD17	ddr_mbps	ddr_mbpsdiv	ddr_mts	med_freq_en
—	0,0	10000	3	3333	1
	0,1	10000	3	3333	1
	1,0	3200	1	3200	1
	1,1	6400	3	2133	0

Note: See Reference [3] for supported DDR Clock Frequency. And, See Reference [4] for how to change DDR Clock Frequency. Furthermore, refer to Reference [3] and DFS documentation for supported DDR Clock Frequency at Low-Power Mode.

Table 3-5 Configuration Value for DDR Clock Frequency (V4M-3: OTPMONITOR17 = 0x02)

Mode Monitor Register 0,1 (MODEMR0, MODEMR1) MD18, MD37, MD36	Mode Monitor Register 0 (MODEMR0) MD19, MD17	ddr_mbps	ddr_mbpsdiv	ddr_mts	med_freq_en
—	0,0	3200	1	3200	1
	0,1	3200	1	3200	1
	1,0	3200	1	3200	1
	1,1	6400	3	2133	0

Note: See Reference [3] for supported DDR Clock Frequency. And, See Reference [4] for how to change DDR Clock Frequency. Furthermore, refer to Reference [3] and DFS documentation for supported DDR Clock Frequency at Low-Power Mode.

Table 3-6 Configuration Value for DDR Clock Frequency (V4M-2: OTPMONITOR17 = 0x04)

Mode Monitor Register 0,1 (MODEMR0, MODEMR1) MD18, MD37, MD36	Mode Monitor Register 0 (MODEMR0) MD19, MD17	ddr_mbps	ddr_mbpsdiv	ddr_mts	med_freq_en
—	0,0	3200	1	3200	1
	0,1	3200	1	3200	1
	1,0	3200	1	3200	1
	1,1	6400	3	2133	0

Note: See Reference [3] for supported DDR Clock Frequency. And, See Reference [4] for how to change DDR Clock Frequency. Furthermore, refer to Reference [3] and DFS documentation for supported DDR Clock Frequency at Low-Power Mode.

3.5 Judgement of PLL3 Setting

[This sequence depends on user system]

Initialization sequence depends on configuration of the DDR clock frequency you use. For more information about setting values, see Appendix A3. For information about calculating the setting value, see Appendix A3.1.

3.6 Judgement of Bus Clock Frequency

[This sequence depends on user system]

Initialization sequence depends on configuration of the bus clock frequency you use. The bus clock frequency parameters are defined as bus_clk and bus_clkdiv in this document. The board clock frequency parameters (brd_clk, brd_clkdiv) are explained in section 3.3.

Table 3-7 Configuration Value for Bus Clock Frequency

Mode Monitor Register 0 (MODEMR0) MD14, MD13	bus_clk	bus_clkdiv	xtal_clk (MHz)
0, 0	brd_clk * 0x18	brd_clkdiv	16.66
0, 1	brd_clk * 0x14	brd_clkdiv	20
1, 0	—	—	—
1, 1	brd_clk * 0x18	brd_clkdiv * 2	33.33

Note: MD14=1 and MD13=0 settings are prohibited for V4M.

4. Main Flow in Initialization

The main flow of initialization sequence is described in this chapter. The main flow is shown in Figure 4-1, and each block is explained. The training part in this figure shows the flow when the medium frequency settings are enabled. See section 4.2.5.1 for the flow when the medium frequency settings are disabled.

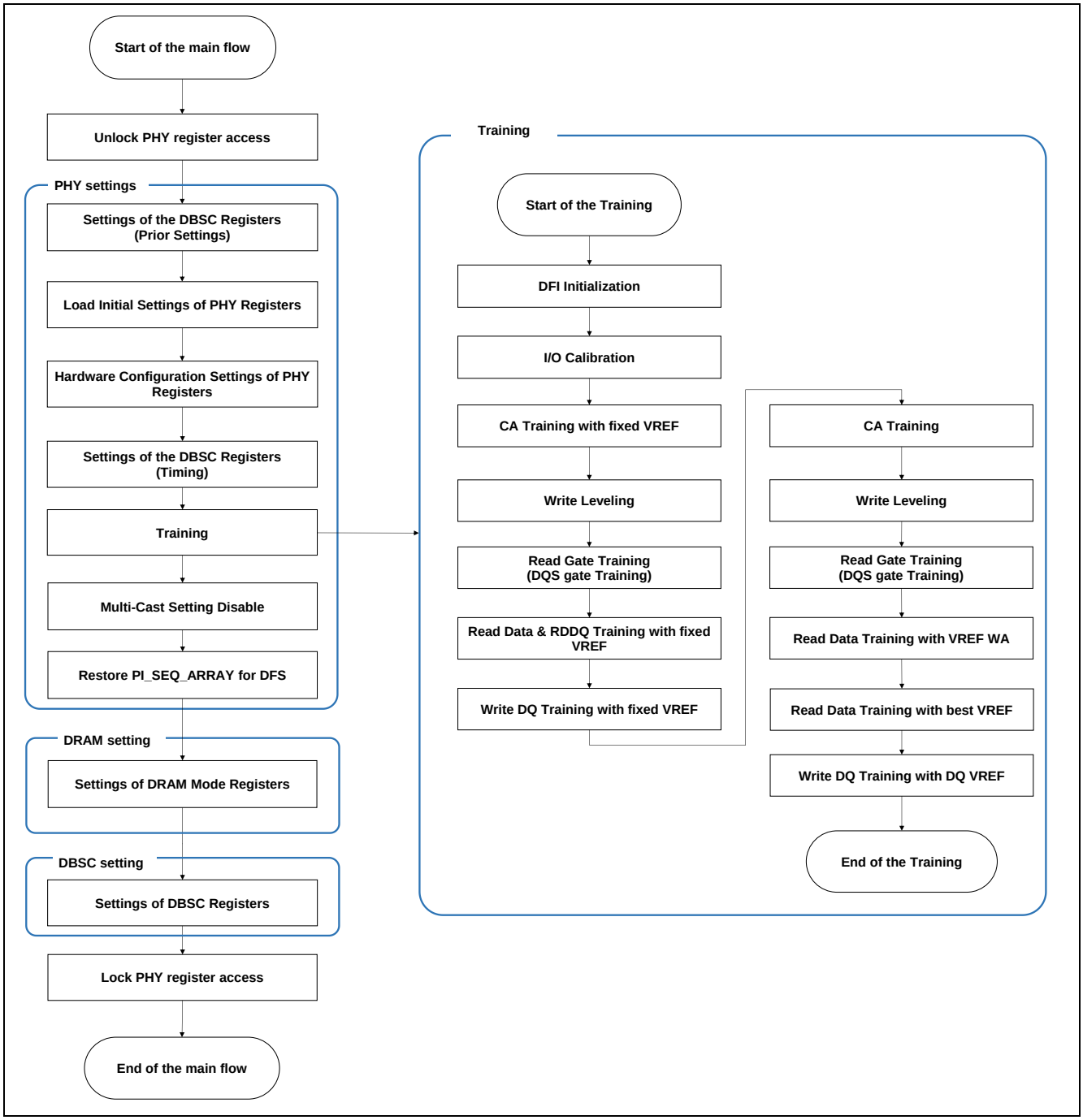


Figure 4-1 Main Flow of the Initialization Sequence

4.1 Unlocking Access to the PHY Registers

Writing 0x0000A55A to this register allows access to the registers of the PHY unit.

Table 4-1 Unlocking Access to the PHY Registers

Op.	Register Name	Bit	Bit Name	Data	Description
W	DBSC_DBPDLK{m_1}	[31:0]	PLOCK{m_1}	0x0000A55A	Unlock access to the PHY registers.

4.2 PHY Settings

PHY part of initialization sequence is described in this chapter, which is the main part of initialization sequence. PHY and some of DBSC parts are initialized based on information obtained in the sequence from section 3.1 to section 3.6: product and its version, board configuration, frequency and so on.

4.2.1 Settings of DBSC Registers (Prior Settings)

Some DBSC registers must be set before PHY and DRAM settings. The individual blocks in the diagram are explained in Table 4-2 to Table 4-5.

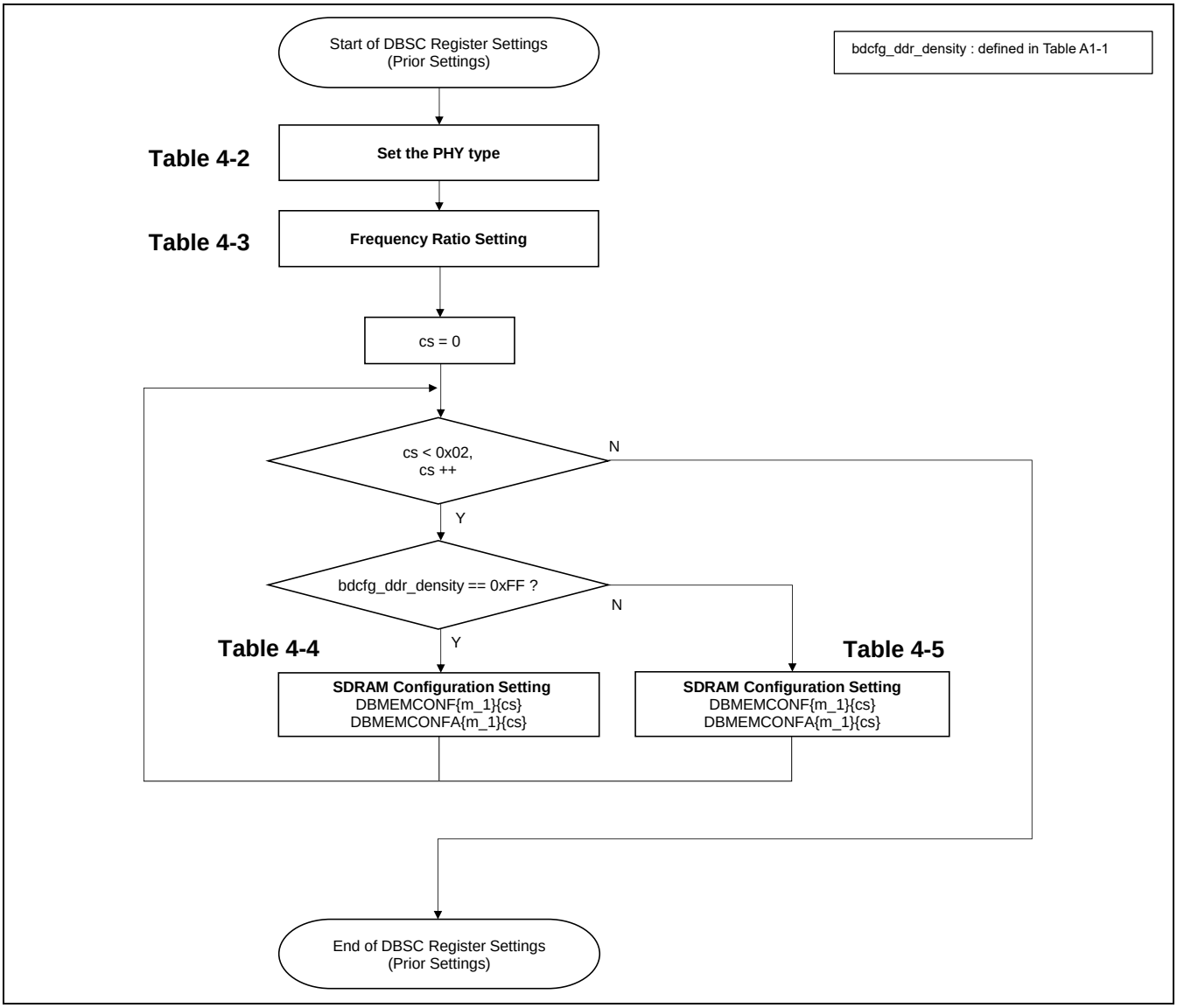


Figure 4-2 Flow of DBSC Register Settings (Prior Settings)

Table 4-2 Type Settings

Op.	Register Name	Bit	Bit Name	Data	Description
W	DBMEMKIND	[3:0]	DDCG	0xA	SDRAM type 1010: LPDDR4X SDRAM
W	DBMEMKINDA	[3:0]	DDCGA	0xA	SDRAM type 1010: LPDDR4X SDRAM
W	DBSC_DBBL	[1:0]	BL	0x2	Burst length 10: Fixed to 16
W	DBSC_DBBLA	[1:0]	BLA	0x2	Burst length 10: Fixed to 16
W	DBSC_DBPHYCONF0	[1:0]	PHYTYPE	0x1	PHY type 01: DFI
W	DBSC_DBSYSCONF0	[2:0]	PCH	0x1	

Table 4-3 Frequency Ratio Setting

Op.	Register Name	Bit	Bit Name	Data	Description
W	DBSC_DBSYSCONF1	[17:16]	DDRCKR	0x0	WCK:CK frequency ratio
		[1:0]	FREQRATIO	0x2	10: Frequency ratio of DBSC5 to memory = 1:4
W	DBSC_DBSYSCONF1A	[1:0]	FREQRATIOA	0x2	10: Frequency ratio of DBSC5 to memory = 1:4
W	DBSC_DBSYSCONF2	[2:0]	SLI_SCHMDD	0x1	
W	DBSC_DBSYSCONF2A	[9]	DFICKM	0x0	
		[8:3]	CHPOS	0x8	Channel position
		[2:0]	SLI_SCHMDDA	0x1	

Table 4-4 SDRAM Configuration Setting

Op.	Register Name	Bit	Bit Name	Data	Description
W	DBSC_DBMEMCONF{m_1}{n_2} n_2=0, n_2=1	[31:30]	DENS{m_1}{n_2}	0x0	Memory density type
		[29]	–	0x0	Reserved
		[28:24]	AWRW{m_1}{n_2}	0x0	Row address bit width
		[23:22]	–	0x0	Reserved
		[21:20]	AWBG{m_1}{n_2}	0x0	Only LPDDR5 bit.
		[19]	–	0x0	Reserved
		[18:16]	AWBK{m_1}{n_2}	0x0	Number of banks
		[15:12]	–	0x0	Reserved
		[11:8]	AWCL{m_1}{n_2}	0x0	Column address bit width
		[7:2]	–	0x00	Reserved
		[1:0]	DW{m_1}{n_2}	0x0	External data bus width
W	DBSC_DBMEMCONFA{m_1}{n_2} n_2=0, n_2=1	[31:30]	DENS{m_1}{n_2}	0x0	Memory density type
		[29]	–	0x0	Reserved
		[28:24]	AWRW{m_1}{n_2}	0x0	Row address bit width
		[23:22]	–	0x0	Reserved
		[21:20]	AWBG{m_1}{n_2}	0x0	Only LPDDR5 bit.
		[19]	–	0x0	Reserved
		[18:16]	AWBK{m_1}{n_2}	0x0	Number of banks
		[15:12]	–	0x0	Reserved
		[11:8]	AWCL{m_1}{n_2}	0x0	Column address bit width
		[7:2]	–	0x00	Reserved
		[1:0]	DW{m_1}{n_2}	0x0	External data bus width

Table 4-5 SDRAM Configuration Setting

Op.	Register Name	Bit	Bit Name	Data	Description
W	DBSC_DBMEMCONF{m_1}{n_2} n_2=0, n_2=1	[31:30]	DENS{m_1}{n_2}	(bdcfg_ddr_density % 2)	Memory density type The following parameters are explained in Appendix A1.1: bdcfg_ddr_density
		[29]	–	0x0	Reserved
		[28:24]	AWRW{m_1}{n_2}	((bdcfg_ddr_density + 1) / 2 + (28 – 3 – 0 – 10 – 1))	Row address bit width The following parameters are explained in Appendix A1.1: bdcfg_ddr_density
		[23:22]	–	0x0	Reserved
		[21:20]	AWBG{m_1}{n_2}	0x0	Only LPDDR5 bit.
		[19]	–	0x0	Reserved
		[18:16]	AWBK{m_1}{n_2}	0x3	Number of banks: 8 banks
		[15:12]	–	0x0	Reserved
		[11:8]	AWCL{m_1}{n_2}	0xA	Column address bit width: 10
		[7:2]	–	0x00	Reserved
		[1:0]	DW{m_1}{n_2}	0x1	External data bus width: 16
W	DBSC_DBMEMCONFA{m_1}{n_2} n_2=0, n_2=1	[31:30]	DENS{m_1}{n_2}	(bdcfg_ddr_density % 2)	Memory density type The following parameters are explained in Appendix A1.1: bdcfg_ddr_density
		[29]	–	0x0	Reserved
		[28:24]	AWRW{m_1}{n_2}	((bdcfg_ddr_density + 1) / 2 + (28 – 3 – 0 – 10 – 1))	Row address bit width The following parameters are explained in Appendix A1.1: bdcfg_ddr_density
		[23:22]	–	0x0	Reserved
		[21:20]	AWBG{m_1}{n_2}	0x0	Only LPDDR5 bit.
		[19]	–	0x0	Reserved
		[18:16]	AWBK{m_1}{n_2}	0x3	Number of banks: 8 banks
		[15:12]	–	0x0	Reserved
		[11:8]	AWCL{m_1}{n_2}	0xA	Column address bit width: 10
		[7:2]	–	0x00	Reserved
		[1:0]	DW{m_1}{n_2}	0x1	External data bus width: 16

4.2.2 loading Initial Settings of PHY Registers

Initial setting values are loaded as in the Figure 4-3. The “Timing parameter adjustment” block must be modified depending on user system. On the related timing parameters to be set are explained in this section. Section 4.2.2.1 makes the PHY register settings for medium frequency.

1. Figure 4-4 Flow of Loading Initial Settings
   The individual blocks in the diagram are explained in Table 4-6 to Table 4-25. In Table 4-22 to Table 4-25, the PHY registers are written in the sequence shown in Table 1-7. In addition, this block also contains the settings for “DRAM Backup Function”.

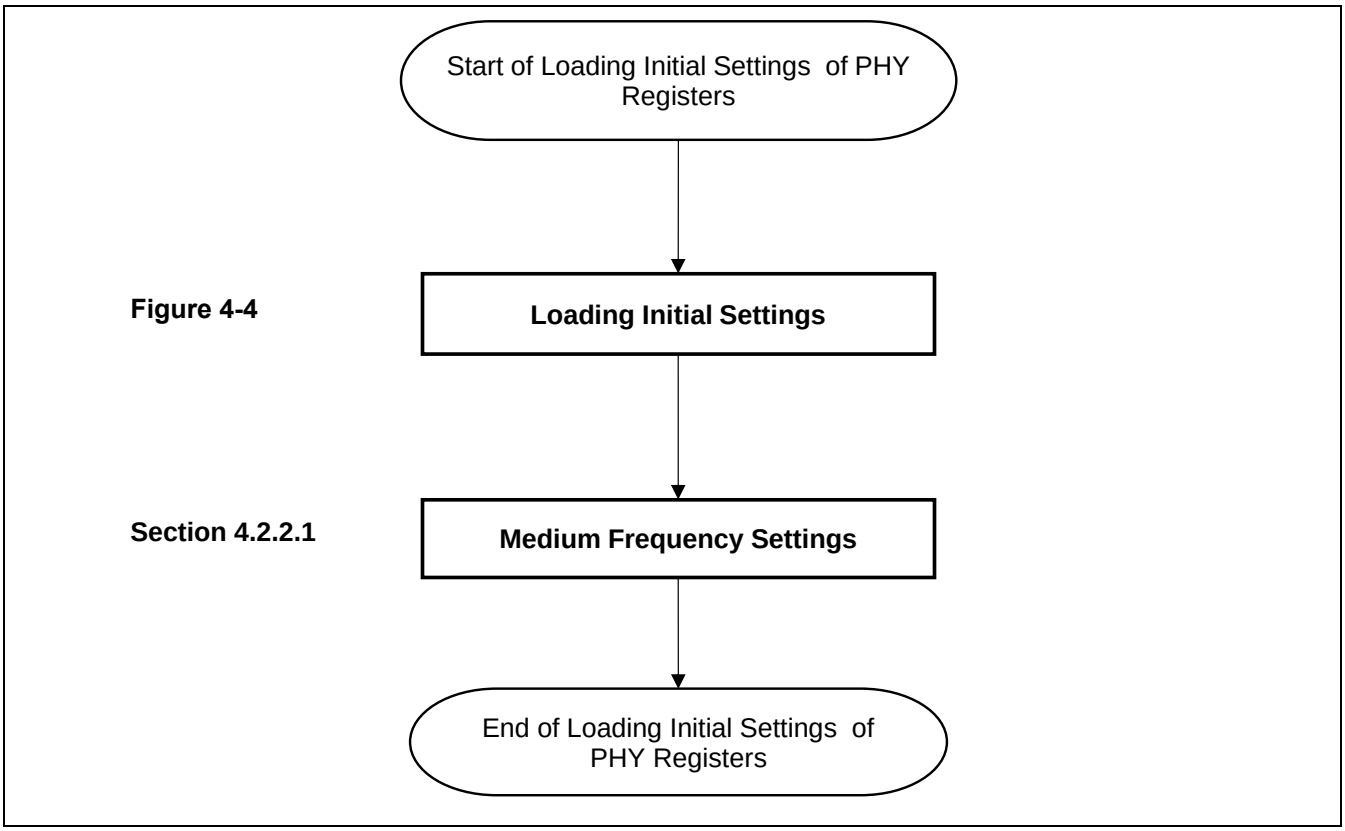
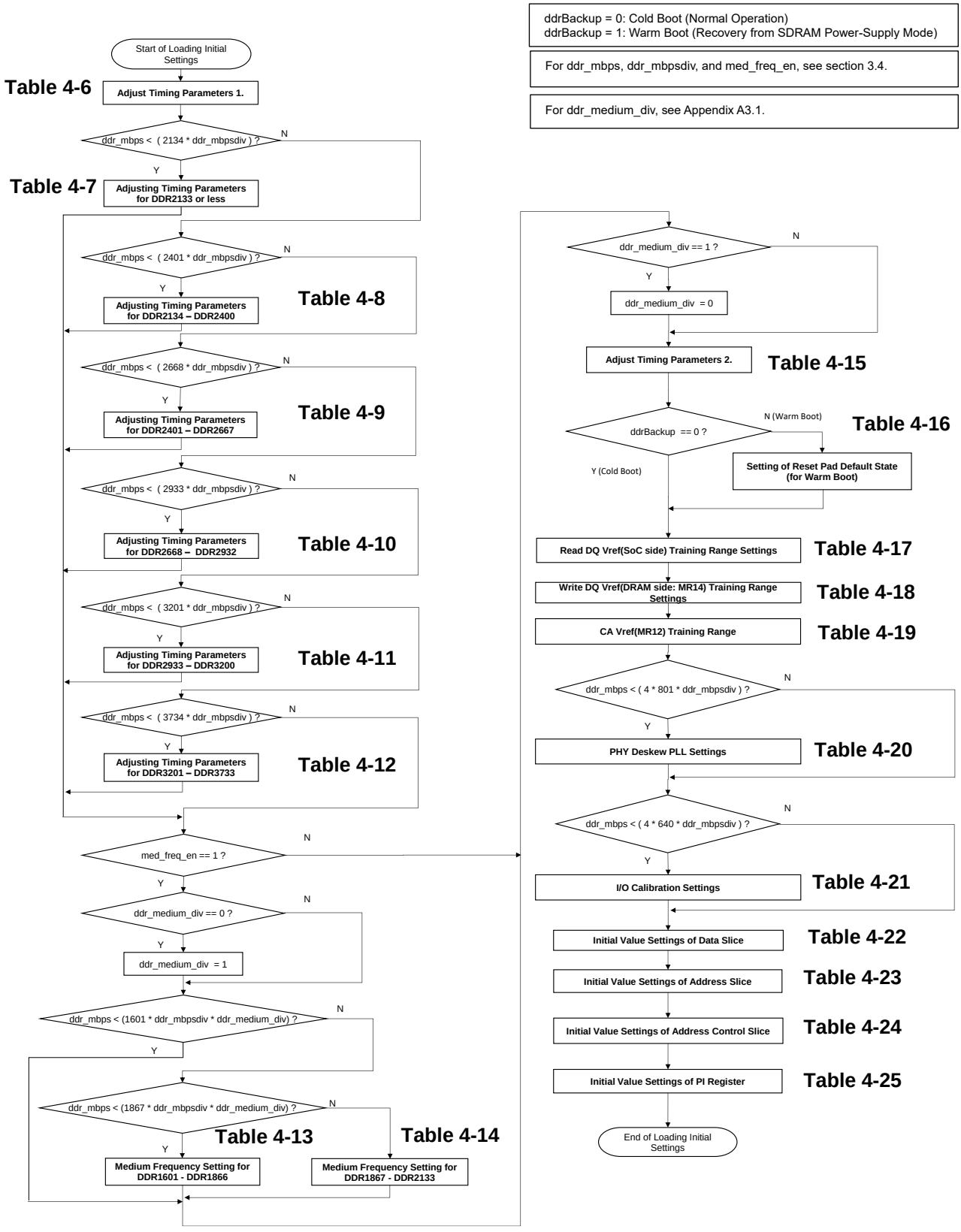


Figure 4-3 Flow of Loading Initial Settings of PHY Registers



The initial values in *1 are overridden by the values set in *2.

*1: Table 4-22, Table 4-23, Table 4-24, Table 4-25

*2: Table 4-6 to Table 4-21 (Overriding on software variables)

Figure 4-4 Flow of Loading Initial Settings

Table 4-6 Adjusting Timing Parameters 1

Op.	Bit Name	Data	Description
W	PHY_CAL_INTERVAL_COUNT_0	10000 * ddr_mbps / ddr_mbpsdiv / 4 / 256	rddq_delay = 103
W	PHY_RDDQ0_SLAVE_DELAY	rddq_delay * ddr_mbps * 256 / (ddr_mbpsdiv * 2 * 1000000)	The following parameters are explained in section 3.4: ddr_mbpsdiv, ddr_mbps.
W	PHY_RDDQ1_SLAVE_DELAY	rddq_delay * ddr_mbps * 256 / (ddr_mbpsdiv * 2 * 1000000)	
W	PHY_RDDQ2_SLAVE_DELAY	rddq_delay * ddr_mbps * 256 / (ddr_mbpsdiv * 2 * 1000000)	
W	PHY_RDDQ3_SLAVE_DELAY	rddq_delay * ddr_mbps * 256 / (ddr_mbpsdiv * 2 * 1000000)	
W	PHY_RDDQ4_SLAVE_DELAY	rddq_delay * ddr_mbps * 256 / (ddr_mbpsdiv * 2 * 1000000)	
W	PHY_RDDQ5_SLAVE_DELAY	rddq_delay * ddr_mbps * 256 / (ddr_mbpsdiv * 2 * 1000000)	
W	PHY_RDDQ6_SLAVE_DELAY	rddq_delay * ddr_mbps * 256 / (ddr_mbpsdiv * 2 * 1000000)	
W	PHY_RDDQ7_SLAVE_DELAY	rddq_delay * ddr_mbps * 256 / (ddr_mbpsdiv * 2 * 1000000)	
W	PHY_RDDM_SLAVE_DELAY	rddq_delay * ddr_mbps * 256 / (ddr_mbpsdiv * 2 * 1000000)	
W	PI_WRLAT_ADJ_F2	WL − 4	WL is defined in MR2. See Reference [1].
W	PI_WRLAT_F2	WL	WL is defined in MR2. See Reference [1].
W	PI_CASLAT_F2	RL	RL is defined in MR2. See Reference [1].
W	PI_TRFC_F2	tRFCab	Parameter is defined in Reference [1].
W	PI_TCAENT_F2	tCAENTns	Parameter is defined in Reference [1].
W	PI_TVREF_LONG_F2	tCAENTns + 1	Parameter is defined in Reference [1].
W	PI_TVREF_SHORT_F2	tCAENTns + 1	Parameter is defined in Reference [1].
W	PI_TXP_F2	tXP + 3	Parameter is defined in Reference [1].
W	PI_TRP_F2	tRPab	Parameter is defined in Reference [1].
W	PI_TRTP_F2	tRTP	Parameter is defined in Reference [1].
W	PI_TRCD_F2	tRCD	Parameter is defined in Reference [1].
W	PI_TWTR_S_F2	tWTR + 1	Parameter is defined in Reference [1].
W	PI_TWTR_L_F2	tWTR + 1	Parameter is defined in Reference [1].
W	PI_TWTR_F2	tWTR + 1	Parameter is defined in Reference [1].
W	PI_TWR_F2	tWR + 1	Parameter is defined in Reference [1].
W	PI_TRAS_MIN_F2	tRAS	Parameter is defined in Reference [1].
W	PI_TXSR_F2	tXSR	Parameter is defined in Reference [1].
W	PI_TXSNR_F2	tXSR	Parameter is defined in Reference [1].
W	PI_TSR_F2	tSR	Parameter is defined in Reference [1].
W	PI_TMRD_F2	tMRD	Parameter is defined in Reference [1].
W	PI_TMRW_F2	tMRW	Parameter is defined in Reference [1].
W	PI_TZQCAL_F2	tZQCALns	Parameter is defined in Reference [1].
W	PI_TZQLAT_F2	tZQLAT	Parameter is defined in Reference [1].
W	PI_TVRCG_ENABLE_F2	tVRCG_ENns + 1	Parameter is defined in Reference [1].
W	PI_TVRCG_DISABLE_F2	tVRCG_DISns + 1	Parameter is defined in Reference [1].

Op.	Bit Name	Data	Description
W	PI_MC_TRFC_F2	tRFCab	Parameter is defined in Reference [1].
W	PI_ZQRESET_F2	tZQRESET	Parameter is defined in Reference [1].

Table 4-7 Adjusting Timing Parameters for DDR2133 or less

Op.	Bit Name	Data	Description
W	PHY_LP4_BOOT_RX_PCLK_CLK_SEL	0x02	
W	PHY_WRLVL_PER_START	0x15	
W	PHY_REGULATOR_EN_CNT	0x04	
W	PHY_RX_CAL_ALL_DLY	0x05	
W	PHY_RX_PCLK_CLK_SEL	0x02	
W	PHY_RDDATA_EN_TSEL_DLY	0x05	
W	PHY_RDDATA_EN_OE_DLY	0x07	
W	PHY_RPTR_UPDATE	0x07	
W	PHY_WRLVL_RESP_WAIT_CNT	0x17	
W	PHY_RDLVL_MAX_EDGE	0x0112	
W	PHY_RDDATA_EN_DLY	0x07	
W	PHY_RDDQS_GATE_SLAVE_DELAY	0x0037	
W	PHY_RDDQS_LATENCY_ADJUST	0x03	
W	PHY_GTLVL_LAT_ADJ_START	0x03	
W	PHY_CSLVL_DLY_STEP	0x02	
W	PHY_LVL_MEAS_DLY_STEP_ENABLE	0x00	
W	PHY_PAD_ACS_RX_PCLK_CLK_SEL	0x02	
W	PI_TDFI_RDLVL_RR	0x0019	
W	PI_TCKCKEL_F2	0x06	
W	PI_TSDO_F2	0x16	
W	PI_TDELAY_RDWR_2_BUS_IDLE_F2	0x49	
W	PI_WCK_ACTIVE_WR_F2	0x0F	
W	PI_WCK_ACTIVE_RD_F2	0x1B	
W	PI_TREF_F2	0x00103D	
W	PI_TDFI_WRLVL_WW_F2	0x001C	
W	PI_WRLVL_WCKOFF_F2	0x12	
W	PI_RDLAT_ADJ_F2	0x000E	
W	PI_TDFI_CALVL_CC_F2	0x003E	
W	PI_TDFI_CALVL_CAPTURE_F2	0x0016	
W	PI_TMRZ_F2	0x02	
W	PI_TDFI_CALVL_STROBE_F2	0x08	
W	PI_TMRWCKEL_F2	0x10	
W	PI_TCKELCK_F2	0x0F	
W	PI_TCKEHDQS_F2	0x19	
W	PI_TFC_F2	0x010B	
W	PI_TDFI_WDQLVL_WR_F2	0x002A	
W	PI_TDFI_WDQLVL_RW_F2	0x0034	
W	PI_WDQLVL_RDLAT_ADJ_F2	0x000C	
W	PI_WDQLVL_WRLAT_ADJ_F2	0x0006	
W	PI_TRAS_MAX_F2	0x838E	
W	PI_TDQSCK_MAX_F2	0x04	

Op.	Bit Name	Data	Description
W	PI_TDFI_CTRLUPD_MAX_F2	0x00207A	
W	PI_TDFI_CTRLUPD_INTERVAL_F2	0x000144C4	
W	PI_TINIT_F2	0x0340E4	
W	PI_TINIT5_F2	0x000855	
W	PI_TWCK2DQ7H_F2	0x08	
W	PI_TDQ7HWCK_F2	0x06	
W	PI_TDQ7LWCK_F2	0x09	
W	PI_TDQ72DQ_F2	0x010B	
W	PI_TCBTRTW_F2	0x16	
W	PI_SEQ_WAIT_16_F2	0x00010B	
W	PI_SEQ_WAIT_17_F2	0x000004	
W	PI_SEQ_WAIT_18_F2	0x00000B	
W	PI_SEQ_WAIT_19_F2	0x000016	
W	PI_SEQ_WAIT_24_F2	0x00006C	
W	PI_SEQ_WAIT_25_F2	0x0000D7	
W	PI_SEQ_WAIT_26_F2	0x000000	
W	PI_SEQ_WAIT_31_F2	0x00010C	
W	PI_WP_GAP_0_F2	0x0028	
W	PI_RP_GAP_0_F2	0x0008	
W	PI_WR_GAP_S_0_F2	0x001F	
W	PI_WR_GAP_L_0_F2	0x001F	
W	PI_RW_GAP_0_F2	0x001B	
W	PI_WP_GAP_1_F2	0x0028	
W	PI_RP_GAP_1_F2	0x0008	
W	PI_WR_GAP_S_1_F2	0x001F	
W	PI_WR_GAP_L_1_F2	0x001F	
W	PI_RW_GAP_1_F2	0x001B	
W	PI_WP_GAP_2_F2	0x0028	
W	PI_RP_GAP_2_F2	0x0008	
W	PI_WR_GAP_S_2_F2	0x001F	
W	PI_WR_GAP_L_2_F2	0x001F	
W	PI_RW_GAP_2_F2	0x001B	
W	PI_WP_GAP_3_F2	0x0028	
W	PI_RP_GAP_3_F2	0x0008	
W	PI_WR_GAP_S_3_F2	0x001F	
W	PI_WR_GAP_L_3_F2	0x001F	
W	PI_RW_GAP_3_F2	0x001B	

Table 4-8 Adjusting Timing Parameters for DDR2134 - DDR2400

Op.	Bit Name	Data	Description
W	PHY_LP4_BOOT_RX_PCLK_CLK_SEL	0x02	
W	PHY_WRLVL_PER_START	0x15	
W	PHY_REGULATOR_EN_CNT	0x04	
W	PHY_RX_CAL_ALL_DLY	0x05	
W	PHY_RDDATA_EN_TSEL_DLY	0x06	
W	PHY_RDDATA_EN_OE_DLY	0x08	
W	PHY_RPTR_UPDATE	0x07	
W	PHY_WRLVL_RESP_WAIT_CNT	0x18	
W	PHY_RDLVL_MAX_EDGE	0x0123	
W	PHY_RDDATA_EN_DLY	0x08	
W	PHY_RDDQS_GATE_SLAVE_DELAY	0x008D	
W	PHY_RDDQS_LATENCY_ADJUST	0x03	
W	PHY_GTLVL_LAT_ADJ_START	0x03	
W	PHY_CSLVL_DLY_STEP	0x02	
W	PHY_LVL_MEAS_DLY_STEP_ENABLE	0x00	
W	PI_TDFI_RDLVL_RR	0x0019	
W	PI_TCKCKEL_F2	0x07	
W	PI_TSDO_F2	0x19	
W	PI_TDELAY_RDWR_2_BUS_IDLE_F2	0x51	
W	PI_WCK_ACTIVE_WR_F2	0x11	
W	PI_WCK_ACTIVE_RD_F2	0x21	
W	PI_TREF_F2	0x00124A	
W	PI_TDFI_WRLVL_WW_F2	0x001D	
W	PI_WRLVL_WCKOFF_F2	0x14	
W	PI_RDLAT_ADJ_F2	0x0013	
W	PI_TDFI_CALVL_CC_F2	0x0040	
W	PI_TDFI_CALVL_CAPTURE_F2	0x0018	
W	PI_TMRZ_F2	0x02	
W	PI_TDFI_CALVL_STROBE_F2	0x08	
W	PI_TMRWCKEL_F2	0x12	
W	PI_TCKELCK_F2	0x10	
W	PI_TCKEHDQS_F2	0x1B	
W	PI_TFC_F2	0x012D	
W	PI_TDFI_WDQLVL_WR_F2	0x002E	
W	PI_TDFI_WDQLVL_RW_F2	0x003D	
W	PI_WDQLVL_RDLAT_ADJ_F2	0x000F	
W	PI_WDQLVL_WRLAT_ADJ_F2	0x0008	
W	PI_TRAS_MAX_F2	0x9422	
W	PI_TDQSCK_MAX_F2	0x05	
W	PI_TDFI_CTRLUPD_MAX_F2	0x002494	
W	PI_TDFI_CTRLUPD_INTERVAL_F2	0x00016DC8	

Op.	Bit Name	Data	Description
W	PI_TEXCKE_F2	0x03	
W	PI_TINIT_F2	0x03A9E1	
W	PI_TINIT5_F2	0x000961	
W	PI_TWCK2DQ7H_F2	0x09	
W	PI_TDQ7HWCK_F2	0x07	
W	PI_TDQ7LWCK_F2	0x0A	
W	PI_TDQ72DQ_F2	0x012D	
W	PI_TCBTRTW_F2	0x19	
W	PI_SEQ_WAIT_16_F2	0x00012D	
W	PI_SEQ_WAIT_17_F2	0x000004	
W	PI_SEQ_WAIT_18_F2	0x00000D	
W	PI_SEQ_WAIT_19_F2	0x000019	
W	PI_SEQ_WAIT_24_F2	0x00007A	
W	PI_SEQ_WAIT_25_F2	0x0000F2	
W	PI_SEQ_WAIT_26_F2	0x000000	
W	PI_SEQ_WAIT_31_F2	0x00012E	
W	PI_WP_GAP_0_F2	0x002C	
W	PI_RP_GAP_0_F2	0x000A	
W	PI_WR_GAP_S_0_F2	0x0023	
W	PI_WR_GAP_L_0_F2	0x0023	
W	PI_RW_GAP_0_F2	0x0020	
W	PI_WP_GAP_1_F2	0x002C	
W	PI_RP_GAP_1_F2	0x000A	
W	PI_WR_GAP_S_1_F2	0x0023	
W	PI_WR_GAP_L_1_F2	0x0023	
W	PI_RW_GAP_1_F2	0x0020	
W	PI_WP_GAP_2_F2	0x002C	
W	PI_RP_GAP_2_F2	0x000A	
W	PI_WR_GAP_S_2_F2	0x0023	
W	PI_WR_GAP_L_2_F2	0x0023	
W	PI_RW_GAP_2_F2	0x0020	
W	PI_WP_GAP_3_F2	0x002C	
W	PI_RP_GAP_3_F2	0x000A	
W	PI_WR_GAP_S_3_F2	0x0023	
W	PI_WR_GAP_L_3_F2	0x0023	
W	PI_RW_GAP_3_F2	0x0020	

Table 4-9 Adjusting Timing Parameters for DDR2401 - DDR2667

Op.	Bit Name	Data	Description
W	PHY_LP4_BOOT_RX_PCLK_CLK_SEL	0x02	
W	PHY_REGULATOR_EN_CNT	0x04	
W	PHY_RX_CAL_ALL_DLY	0x06	
W	PHY_RDDATA_EN_TSEL_DLY	0x07	
W	PHY_RDDATA_EN_OE_DLY	0x09	
W	PHY_RPTR_UPDATE	0x07	
W	PHY_WRLVL_RESP_WAIT_CNT	0x1B	
W	PHY_RDLVL_MAX_EDGE	0x0134	
W	PHY_RDDATA_EN_DLY	0x09	
W	PHY_RDDQS_GATE_SLAVE_DELAY	0x00E2	
W	PHY_RDDQS_LATENCY_ADJUST	0x03	
W	PHY_GTLVL_LAT_ADJ_START	0x04	
W	PHY_CSLVL_DLY_STEP	0x02	
W	PHY_LVL_MEAS_DLY_STEP_ENABLE	0x00	
W	PI_TDFI_RDLVL_RR	0x0019	
W	PI_TCKCKEL_F2	0x07	
W	PI_TSDO_F2	0x1B	
W	PI_TDELAY_RDWR_2_BUS_IDLE_F2	0x51	
W	PI_WCK_ACTIVE_WR_F2	0x11	
W	PI_WCK_ACTIVE_RD_F2	0x21	
W	PI_TREF_F2	0x001451	
W	PI_TDFI_WRLVL_WW_F2	0x001D	
W	PI_WRLVL_WCKOFF_F2	0x16	
W	PI_RDLAT_ADJ_F2	0x0012	
W	PI_TDFI_CALVL_CC_F2	0x0041	
W	PI_TDFI_CALVL_CAPTURE_F2	0x0019	
W	PI_TMRZ_F2	0x02	
W	PI_TDFI_CALVL_STROBE_F2	0x08	
W	PI_TMRWCKEL_F2	0x14	
W	PI_TCKELCK_F2	0x10	
W	PI_TCKEHDQS_F2	0x1C	
W	PI_TFC_F2	0x014E	
W	PI_TDFI_WDQLVL_WR_F2	0x002F	
W	PI_TDFI_WDQLVL_RW_F2	0x003D	
W	PI_WDQLVL_RDLAT_ADJ_F2	0x000E	
W	PI_WDQLVL_WRLAT_ADJ_F2	0x0008	
W	PI_TRAS_MAX_F2	0xA488	
W	PI_TDQSCK_MAX_F2	0x05	
W	PI_TDFI_CTRLUPD_MAX_F2	0x0028A2	
W	PI_TDFI_CTRLUPD_INTERVAL_F2	0x00019654	
W	PI_TEXCKE_F2	0x03	

Op.	Bit Name	Data	Description
W	PI_TINIT_F2	0x0411AB	
W	PI_TINIT5_F2	0x000A6B	
W	PI_TWCK2DQ7H_F2	0x09	
W	PI_TDQ7HWCK_F2	0x07	
W	PI_TDQ7LWCK_F2	0x0A	
W	PI_TDQ72DQ_F2	0x014E	
W	PI_TCBTRTW_F2	0x1B	
W	PI_SEQ_WAIT_16_F2	0x00014E	
W	PI_SEQ_WAIT_17_F2	0x000004	
W	PI_SEQ_WAIT_18_F2	0x00000D	
W	PI_SEQ_WAIT_19_F2	0x00001B	
W	PI_SEQ_WAIT_24_F2	0x000087	
W	PI_SEQ_WAIT_25_F2	0x00010C	
W	PI_SEQ_WAIT_26_F2	0x000000	
W	PI_SEQ_WAIT_31_F2	0x00014F	
W	PI_WP_GAP_0_F2	0x002E	
W	PI_RP_GAP_0_F2	0x000A	
W	PI_WR_GAP_S_0_F2	0x0024	
W	PI_WR_GAP_L_0_F2	0x0024	
W	PI_RW_GAP_0_F2	0x0020	
W	PI_WP_GAP_1_F2	0x002E	
W	PI_RP_GAP_1_F2	0x000A	
W	PI_WR_GAP_S_1_F2	0x0024	
W	PI_WR_GAP_L_1_F2	0x0024	
W	PI_RW_GAP_1_F2	0x0020	
W	PI_WP_GAP_2_F2	0x002E	
W	PI_RP_GAP_2_F2	0x000A	
W	PI_WR_GAP_S_2_F2	0x0024	
W	PI_WR_GAP_L_2_F2	0x0024	
W	PI_RW_GAP_2_F2	0x0020	
W	PI_WP_GAP_3_F2	0x002E	
W	PI_RP_GAP_3_F2	0x000A	
W	PI_WR_GAP_S_3_F2	0x0024	
W	PI_WR_GAP_L_3_F2	0x0024	
W	PI_RW_GAP_3_F2	0x0020	

Table 4-10 Adjusting Timing Parameters for DDR2668 - DDR2932

Op.	Bit Name	Data	Description
W	PHY_LP4_BOOT_RX_PCLK_CLK_SEL	0x02	
W	PHY_REGULATOR_EN_CNT	0x05	
W	PHY_RX_CAL_ALL_DLY	0x06	
W	PHY_RDDATA_EN_TSEL_DLY	0x08	
W	PHY_RDDATA_EN_OE_DLY	0x0A	
W	PHY_RPTR_UPDATE	0x07	
W	PHY_WRLVL_RESP_WAIT_CNT	0x1D	
W	PHY_RDLVL_MAX_EDGE	0x0145	
W	PHY_RDDATA_EN_DLY	0x0A	
W	PHY_RDDQS_GATE_SLAVE_DELAY	0x0037	
W	PHY_RDDQS_LATENCY_ADJUST	0x04	
W	PHY_GTLVL_LAT_ADJ_START	0x05	
W	PHY_CSLVL_DLY_STEP	0x02	
W	PHY_LVL_MEAS_DLY_STEP_ENABLE	0x00	
W	PI_TDFI_RDLVL_RR	0x0019	
W	PI_TCKCKEL_F2	0x08	
W	PI_TSDO_F2	0x1E	
W	PI_TDELAY_RDWR_2_BUS_IDLE_F2	0x57	
W	PI_WCK_ACTIVE_WR_F2	0x13	
W	PI_WCK_ACTIVE_RD_F2	0x25	
W	PI_TREF_F2	0x001659	
W	PI_TDFI_WRLVL_WW_F2	0x001E	
W	PI_WRLVL_WCKOFF_F2	0x18	
W	PI_RDLAT_ADJ_F2	0x0015	
W	PI_TDFI_CALVL_CC_F2	0x0042	
W	PI_TDFI_CALVL_CAPTURE_F2	0x001A	
W	PI_TMRZ_F2	0x03	
W	PI_TDFI_CALVL_STROBE_F2	0x08	
W	PI_TMRWCKEL_F2	0x16	
W	PI_TCKELCK_F2	0x11	
W	PI_TCKEHDQS_F2	0x1D	
W	PI_TFC_F2	0x016F	
W	PI_TDFI_WDQLVL_WR_F2	0x0032	
W	PI_TDFI_WDQLVL_RW_F2	0x0041	
W	PI_WDQLVL_RDLAT_ADJ_F2	0x0011	
W	PI_WDQLVL_WRLAT_ADJ_F2	0x000A	
W	PI_TRAS_MAX_F2	0xB4EF	
W	PI_TDQSCK_MAX_F2	0x06	
W	PI_TDFI_CTRLUPD_MAX_F2	0x002CB2	
W	PI_TDFI_CTRLUPD_INTERVAL_F2	0x0001BEF4	
W	PI_TEXCKE_F2	0x03	

Op.	Bit Name	Data	Description
W	PI_TINIT_F2	0x047988	
W	PI_TINIT5_F2	0x000B75	
W	PI_TWCK2DQ7H_F2	0x0A	
W	PI_TDQ7HWCK_F2	0x08	
W	PI_TDQ7LWCK_F2	0x0B	
W	PI_TDQ72DQ_F2	0x016F	
W	PI_TCBTRTW_F2	0x1E	
W	PI_SEQ_WAIT_16_F2	0x00016F	
W	PI_SEQ_WAIT_17_F2	0x000005	
W	PI_SEQ_WAIT_18_F2	0x00000E	
W	PI_SEQ_WAIT_19_F2	0x00001E	
W	PI_SEQ_WAIT_24_F2	0x000094	
W	PI_SEQ_WAIT_25_F2	0x000127	
W	PI_SEQ_WAIT_26_F2	0x000000	
W	PI_SEQ_WAIT_31_F2	0x000170	
W	PI_WP_GAP_0_F2	0x0033	
W	PI_RP_GAP_0_F2	0x000B	
W	PI_WR_GAP_S_0_F2	0x0027	
W	PI_WR_GAP_L_0_F2	0x0027	
W	PI_RW_GAP_0_F2	0x0023	
W	PI_WP_GAP_1_F2	0x0033	
W	PI_RP_GAP_1_F2	0x000B	
W	PI_WR_GAP_S_1_F2	0x0027	
W	PI_WR_GAP_L_1_F2	0x0027	
W	PI_RW_GAP_1_F2	0x0023	
W	PI_WP_GAP_2_F2	0x0033	
W	PI_RP_GAP_2_F2	0x000B	
W	PI_WR_GAP_S_2_F2	0x0027	
W	PI_WR_GAP_L_2_F2	0x0027	
W	PI_RW_GAP_2_F2	0x0023	
W	PI_WP_GAP_3_F2	0x0033	
W	PI_RP_GAP_3_F2	0x000B	
W	PI_WR_GAP_S_3_F2	0x0027	
W	PI_WR_GAP_L_3_F2	0x0027	
W	PI_RW_GAP_3_F2	0x0023	

Table 4-11 Adjusting Timing Parameters for DDR2933 - DDR3200

Op.	Bit Name	Data	Description
W	PHY_REGULATOR_EN_CNT	0x05	
W	PHY_RX_CAL_ALL_DLY	0x07	
W	PHY_RDDATA_EN_TSEL_DLY	0x09	
W	PHY_RDDATA_EN_OE_DLY	0x0B	
W	PHY_RPTR_UPDATE	0x07	
W	PHY_WRLVL_RESP_WAIT_CNT	0x1E	
W	PHY_RDLVL_MAX_EDGE	0x0156	
W	PHY_RDDATA_EN_DLY	0x0B	
W	PHY_RDDQS_GATE_SLAVE_DELAY	0x008C	
W	PHY_RDDQS_LATENCY_ADJUST	0x04	
W	PHY_GTLVL_LAT_ADJ_START	0x06	
W	PI_TCKCKEL_F2	0x08	
W	PI_TSDO_F2	0x20	
W	PI_TDELAY_RDWR_2_BUS_IDLE_F2	0x57	
W	PI_WCK_ACTIVE_WR_F2	0x13	
W	PI_WCK_ACTIVE_RD_F2	0x25	
W	PI_TREF_F2	0x001863	
W	PI_TDFI_WRLVL_WW_F2	0x001F	
W	PI_WRLVL_WCKOFF_F2	0x1A	
W	PI_RDLAT_ADJ_F2	0x0014	
W	PI_TDFI_CALVL_CC_F2	0x0043	
W	PI_TDFI_CALVL_CAPTURE_F2	0x001B	
W	PI_TMRZ_F2	0x03	
W	PI_TDFI_CALVL_STROBE_F2	0x09	
W	PI_TMRWCKEL_F2	0x18	
W	PI_TCKELCK_F2	0x11	
W	PI_TCKEHDQS_F2	0x1E	
W	PI_TFC_F2	0x0190	
W	PI_TDFI_WDQLVL_WR_F2	0x0033	
W	PI_TDFI_WDQLVL_RW_F2	0x0041	
W	PI_WDQLVL_RDLAT_ADJ_F2	0x0010	
W	PI_WDQLVL_WRLAT_ADJ_F2	0x000A	
W	PI_TRAS_MAX_F2	0xC570	
W	PI_TDQSCK_MAX_F2	0x06	
W	PI_TDFI_CTRLUPD_MAX_F2	0x0030C6	
W	PI_TDFI_CTRLUPD_INTERVAL_F2	0x0001E7BC	
W	PI_TEXCKE_F2	0x03	
W	PI_TINIT_F2	0x04E200	
W	PI_TINIT5_F2	0x000C80	
W	PI_TWCK2DQ7H_F2	0x0A	
W	PI_TDQ7HWCK_F2	0x08	

Op.	Bit Name	Data	Description
W	PI_TDQ7LWCK_F2	0x0B	
W	PI_TDQ72DQ_F2	0x0190	
W	PI_TCBTRTW_F2	0x20	
W	PI_SEQ_WAIT_16_F2	0x000190	
W	PI_SEQ_WAIT_17_F2	0x000005	
W	PI_SEQ_WAIT_18_F2	0x00000F	
W	PI_SEQ_WAIT_19_F2	0x000020	
W	PI_SEQ_WAIT_24_F2	0x0000A1	
W	PI_SEQ_WAIT_25_F2	0x000141	
W	PI_SEQ_WAIT_26_F2	0x000000	
W	PI_SEQ_WAIT_31_F2	0x000191	
W	PI_WP_GAP_0_F2	0x0035	
W	PI_RP_GAP_0_F2	0x000C	
W	PI_WR_GAP_S_0_F2	0x0028	
W	PI_WR_GAP_L_0_F2	0x0028	
W	PI_RW_GAP_0_F2	0x0023	
W	PI_WP_GAP_1_F2	0x0035	
W	PI_RP_GAP_1_F2	0x000C	
W	PI_WR_GAP_S_1_F2	0x0028	
W	PI_WR_GAP_L_1_F2	0x0028	
W	PI_RW_GAP_1_F2	0x0023	
W	PI_WP_GAP_2_F2	0x0035	
W	PI_RP_GAP_2_F2	0x000C	
W	PI_WR_GAP_S_2_F2	0x0028	
W	PI_WR_GAP_L_2_F2	0x0028	
W	PI_RW_GAP_2_F2	0x0023	
W	PI_WP_GAP_3_F2	0x0035	
W	PI_RP_GAP_3_F2	0x000C	
W	PI_WR_GAP_S_3_F2	0x0028	
W	PI_WR_GAP_L_3_F2	0x0028	
W	PI_RW_GAP_3_F2	0x0023	

Table 4-12 Adjusting Timing Parameters for DDR3201 - DDR3733

Op.	Bit Name	Data	Description
W	PHY_REGULATOR_EN_CNT	0x06	
W	PHY_RX_CAL_ALL_DLY	0x08	
W	PHY_RDDATA_EN_TSEL_DLY	0x0B	
W	PHY_RDDATA_EN_OE_DLY	0x0D	
W	PHY_WRLVL_RESP_WAIT_CNT	0x23	
W	PHY_RDLVL_MAX_EDGE	0x0178	
W	PHY_RDDATA_EN_DLY	0x0D	
W	PHY_RDDQS_GATE_SLAVE_DELAY	0x0036	
W	PHY_GTLVL_LAT_ADJ_START	0x07	
W	PI_TCKCKEL_F2	0x0A	
W	PI_TSDO_F2	0x26	
W	PI_TDELAY_RDWR_2_BUS_IDLE_F2	0x5E	
W	PI_WCK_ACTIVE_WR_F2	0x15	
W	PI_WCK_ACTIVE_RD_F2	0x29	
W	PI_TREF_F2	0x001C71	
W	PI_TDFI_WRLVL_WW_F2	0x0020	
W	PI_WRLVL_WCKOFF_F2	0x1E	
W	PI_RDLAT_ADJ_F2	0x0016	
W	PI_TDFI_CALVL_CC_F2	0x0046	
W	PI_TDFI_CALVL_CAPTURE_F2	0x001E	
W	PI_TMRZ_F2	0x03	
W	PI_TDFI_CALVL_STROBE_F2	0x09	
W	PI_TMRWCKEL_F2	0x1C	
W	PI_TCKELCK_F2	0x13	
W	PI_TCKEHDQS_F2	0x21	
W	PI_TFC_F2	0x01D3	
W	PI_TDFI_WDQLVL_WR_F2	0x0038	
W	PI_TDFI_WDQLVL_RW_F2	0x0048	
W	PI_WDQLVL_RDLAT_ADJ_F2	0x0012	
W	PI_WDQLVL_WRLAT_ADJ_F2	0x000c	
W	PI_TRAS_MAX_F2	0xE638	
W	PI_TDQSCK_MAX_F2	0x07	
W	PI_TDFI_CTRLUPD_MAX_F2	0x0038E2	
W	PI_TDFI_CTRLUPD_INTERVAL_F2	0x000238D4	
W	PI_TEXCKE_F2	0x03	
W	PI_TINIT_F2	0x05B18F	
W	PI_TINIT5_F2	0x000E94	
W	PI_TWCK2DQ7H_F2	0x0C	
W	PI_TDQ7HWCK_F2	0x0A	
W	PI_TDQ7LWCK_F2	0x0D	
W	PI_TDQ72DQ_F2	0x01D3	

Op.	Bit Name	Data	Description
W	PI_TCBTRTW_F2	0x26	
W	PI_SEQ_WAIT_16_F2	0x0001D3	
W	PI_SEQ_WAIT_17_F2	0x000006	
W	PI_SEQ_WAIT_18_F2	0x000011	
W	PI_SEQ_WAIT_19_F2	0x000026	
W	PI_SEQ_WAIT_24_F2	0x0000BC	
W	PI_SEQ_WAIT_25_F2	0x000177	
W	PI_SEQ_WAIT_26_F2	0x000004	
W	PI_SEQ_WAIT_31_F2	0x0001D4	
W	PI_WP_GAP_0_F2	0x003C	
W	PI_RP_GAP_0_F2	0x000E	
W	PI_WR_GAP_S_0_F2	0x002D	
W	PI_WR_GAP_L_0_F2	0x002D	
W	PI_RW_GAP_0_F2	0x0026	
W	PI_WP_GAP_1_F2	0x003C	
W	PI_RP_GAP_1_F2	0x000E	
W	PI_WR_GAP_S_1_F2	0x002D	
W	PI_WR_GAP_L_1_F2	0x002D	
W	PI_RW_GAP_1_F2	0x0026	
W	PI_WP_GAP_2_F2	0x003C	
W	PI_RP_GAP_2_F2	0x000E	
W	PI_WR_GAP_S_2_F2	0x002D	
W	PI_WR_GAP_L_2_F2	0x002D	
W	PI_RW_GAP_2_F2	0x0026	
W	PI_WP_GAP_3_F2	0x003C	
W	PI_RP_GAP_3_F2	0x000E	
W	PI_WR_GAP_S_3_F2	0x002D	
W	PI_WR_GAP_L_3_F2	0x002D	
W	PI_RW_GAP_3_F2	0x0026	

Table 4-13 Medium Frequency Setting for DDR1601 – DDR1866

Op.	Bit Name	Data	Description
W	PI_TSDO_F1	0x13	
W	PI_TDELAY_RDWR_2_BUS_IDLE_F1	0x48	
W	PI_WRLAT_F1	0x0A	
W	PI_WCK_ACTIVE_WR_F1	0x0F	
W	PI_WCK_ACTIVE_RD_F1	0x1B	
W	PI_CASLAT_F1	0x16	
W	PI_TRFC_F1	0x0163	
W	PI_TREF_F1	0x000E38	
W	PI_TDFI_WRLVL_WW_F1	0x001B	
W	PI_WRLVL_WCKOFF_F1	0x11	
W	PI_RDLAT_ADJ_F1	0x000F	
W	PI_WRLAT_ADJ_F1	0x06	
W	PI_TDFI_CALVL_CC_F1	0x003D	
W	PI_TDFI_CALVL_CAPTURE_F1	0x0015	
W	PI_TCAENT_F1	0x00EA	
W	PI_TVREF_SHORT_F1	0x00EB	
W	PI_TVREF_LONG_F1	0x00EB	
W	PI_TVRCG_ENABLE_F1	0x00BC	
W	PI_TVRCG_DISABLE_F1	0x005F	
W	PI_TXP_F1	0x0B	
W	PI_TMRWCKEL_F1	0x0F	
W	PI_TCKELCK_F1	0x0E	
W	PI_TCKEHDQS_F1	0x18	
W	PI_TFC_F1	0x00EA	
W	PI_TDFI_WDQLVL_RW_F1	0x0034	
W	PI_WDQLVL_RDLAT_ADJ_F1	0x000D	
W	PI_WDQLVL_WRLAT_ADJ_F1	0x0006	
W	PI_TRP_F1	0x14	
W	PI_TRCD_F1	0x11	
W	PI_TWTR_S_F1	0x0B	
W	PI_TWTR_L_F1	0x0B	
W	PI_TWTR_F1	0x0B	
W	PI_TWR_F1	0x12	
W	PI_TRAS_MAX_F1	0x7337	
W	PI_TRAS_MIN_F1	0x0028	
W	PI_TDQSCK_MAX_F1	0x04	
W	PI_TSR_F1	0x0F	
W	PI_TMRD_F1	0x0E	
W	PI_TDFI_CTRLUPD_MAX_F1	0x001C70	
W	PI_TDFI_CTRLUPD_INTERVAL_F1	0x00011C60	
W	PI_TXSR_F1	0x016A	

Op.	Bit Name	Data	Description
W	PI_TINIT_F1	0x02D976	
W	PI_TINIT5_F1	0x00074C	
W	PI_TXSNR_F1	0x016A	
W	PI_TZQCAL_F1	0x03A6	
W	PI_TZQLAT_F1	0x1D	
W	PI_ZQRESET_F1	0x2F	
W	PI_TWCK2DQ7H_F1	0x07	
W	PI_TDQ7HWCK_F1	0x05	
W	PI_TDQ7LWCK_F1	0x08	
W	PI_TDQ72DQ_F1	0x00EA	
W	PI_TCBTRTW_F1	0x13	
W	PI_MC_TRFC_F1	0x0165	
W	PI_SEQ_WAIT_16_F1	0x0000EA	
W	PI_SEQ_WAIT_18_F1	0x00000B	
W	PI_SEQ_WAIT_19_F1	0x000013	
W	PI_SEQ_WAIT_24_F1	0x00005F	
W	PI_SEQ_WAIT_25_F1	0x0000BC	
W	PI_SEQ_WAIT_31_F1	0x0000EB	
W	PI_RW_GAP_0_F1	0x001B	
W	PI_RW_GAP_1_F1	0x001B	
W	PI_RW_GAP_2_F1	0x001B	
W	PI_RW_GAP_3_F1	0x001B	
W	PI_DARRAY3_0_CS0_F1	0x34	
W	PI_DARRAY3_1_CS0_F1	0x1B	
W	PI_DARRAY3_0_CS1_F1	0x34	
W	PI_DARRAY3_1_CS1_F1	0x1B	

Table 4-14 Medium Frequency Setting for DDR1867 – DDR2133

Op.	Bit Name	Data	Description
W	PI_TCKCKEL_F1	0x06	
W	PI_TSDO_F1	0x16	
W	PI_TDELAY_RDWR_2_BUS_IDLE_F1	0x49	
W	PI_WRLAT_F1	0x0A	
W	PI_WCK_ACTIVE_WR_F1	0x0F	
W	PI_WCK_ACTIVE_RD_F1	0x1B	
W	PI_CASLAT_F1	0x16	
W	PI_TRFC_F1	0x0196	
W	PI_TREF_F1	0x00103D	
W	PI_TDFI_WRLVL_WW_F1	0x001C	
W	PI_WRLVL_WCKOFF_F1	0x12	
W	PI_RDLAT_ADJ_F1	0x000E	
W	PI_WRLAT_ADJ_F1	0x06	
W	PI_TDFI_CALVL_CC_F1	0x003E	
W	PI_TDFI_CALVL_CAPTURE_F1	0x0016	
W	PI_TCAENT_F1	0x010B	
W	PI_TVREF_SHORT_F1	0x010C	
W	PI_TVREF_LONG_F1	0x010C	
W	PI_TVRCG_ENABLE_F1	0x00D7	
W	PI_TVRCG_DISABLE_F1	0x006C	
W	PI_TDFI_CALVL_STROBE_F1	0x08	
W	PI_TXP_F1	0x0B	
W	PI_TMRWCKEL_F1	0x10	
W	PI_TCKELCK_F1	0x0F	
W	PI_TCKEHDQS_F1	0x19	
W	PI_TFC_F1	0x010B	
W	PI_TDFI_WDQLVL_WR_F1	0x002A	
W	PI_TDFI_WDQLVL_RW_F1	0x0034	
W	PI_WDQLVL_RDLAT_ADJ_F1	0x000C	
W	PI_WDQLVL_WRLAT_ADJ_F1	0x0006	
W	PI_TRP_F1	0x17	
W	PI_TRCD_F1	0x14	
W	PI_TWTR_S_F1	0x0C	
W	PI_TWTR_L_F1	0x0C	
W	PI_TWTR_F1	0x0C	
W	PI_TWR_F1	0x15	
W	PI_TRAS_MAX_F1	0x838E	
W	PI_TRAS_MIN_F1	0x002D	
W	PI_TDQSCK_MAX_F1	0x04	
W	PI_TSR_F1	0x10	
W	PI_TMRD_F1	0x0F	

Op.	Bit Name	Data	Description
W	PI_TMRW_F1	0x0B	
W	PI_TDFI_CTRLUPD_MAX_F1	0x00207A	
W	PI_TDFI_CTRLUPD_INTERVAL_F1	0x000144C4	
W	PI_TXSR_F1	0x019E	
W	PI_TEXCKE_F1	0x04	
W	PI_TINIT_F1	0x0340E4	
W	PI_TINIT5_F1	0x000855	
W	PI_TXSNR_F1	0x019E	
W	PI_TZQCAL_F1	0x042B	
W	PI_TZQLAT_F1	0x20	
W	PI_ZQRESET_F1	0x36	
W	PI_TWCK2DQ7H_F1	0x08	
W	PI_TDQ7HWCK_F1	0x06	
W	PI_TDQ7LWCK_F1	0x09	
W	PI_TDQ72DQ_F1	0x010B	
W	PI_TCBTRTW_F1	0x16	
W	PI_MC_TRFC_F1	0x0198	
W	PI_SEQ_WAIT_16_F1	0x00010B	
W	PI_SEQ_WAIT_17_F1	0x000004	
W	PI_SEQ_WAIT_18_F1	0x00000B	
W	PI_SEQ_WAIT_19_F1	0x000016	
W	PI_SEQ_WAIT_24_F1	0x00006C	
W	PI_SEQ_WAIT_25_F1	0x0000D7	
W	PI_SEQ_WAIT_31_F1	0x00010C	
W	PI_WP_GAP_0_F1	0x0028	
W	PI_WR_GAP_S_0_F1	0x001F	
W	PI_WR_GAP_L_0_F1	0x001F	
W	PI_RW_GAP_0_F1	0x001B	
W	PI_WP_GAP_1_F1	0x0028	
W	PI_WR_GAP_S_1_F1	0x001F	
W	PI_WR_GAP_L_1_F1	0x001F	
W	PI_RW_GAP_1_F1	0x001B	
W	PI_WP_GAP_2_F1	0x0028	
W	PI_WR_GAP_S_2_F1	0x001F	
W	PI_WR_GAP_L_2_F1	0x001F	
W	PI_RW_GAP_2_F1	0x001B	
W	PI_WP_GAP_3_F1	0x0028	
W	PI_WR_GAP_S_3_F1	0x001F	
W	PI_WR_GAP_L_3_F1	0x001F	
W	PI_RW_GAP_3_F1	0x001B	
W	PI_DARRAY3_0_CS0_F1	0x34	
W	PI_DARRAY3_1_CS0_F1	0x1B	

Op.	Bit Name	Data	Description
W	PI_DARRAY3_0_CS1_F1	0x34	
W	PI_DARRAY3_1_CS1_F1	0x1B	

Table 4-15 Adjusting Timing Parameters 2

Op.	Bit Name	Data	Description
W	PI_DARRAY3_0_CS0_F2	MR1	MR1, MR2 are defined in Reference [1].
W	PI_DARRAY3_1_CS0_F2	MR2	
W	PI_DARRAY3_0_CS1_F2	MR1	MR1, MR2 are defined in Reference [1].
W	PI_DARRAY3_1_CS1_F2	MR2	

Table 4-16 Setting of Reset Pad Default State

Op.	Bit Name	Data	Description
W	PHY_SET_DFI_INPUT_RST_PAD	0x01	
W	PI_PWRUP_SREFRESH_EXIT	0x01	

Table 4-17 Read DQ Vref(SoC side) Training Range Settings

Op.	Bit Name	Data	Description
W	PHY_VREF_INITIAL_START_POINT	bdcfg_vref_r & 0x000000FF	This part is set when the user setting value is used. See Appendix A1.1 for the following parameters: bdcfg_vref_r
W	PHY_VREF_INITIAL_STOP_POINT	(bdcfg_vref_r & 0x0000FF00) >> 8	
W	PHY_VREF_INITIAL_STEPSIZE	(bdcfg_vref_r & 0x00FF0000) >> 16	

Table 4-18 Write DQ Vref(DRAM side: MR14) Training Range Settings

Op.	Bit Name	Data	Description
W	PI_WDQLVL_VREF_INITIAL_START_POINT_F0	bdcfg_vref_w & 0x00FF	This part is set when the user setting value is used. See Appendix A1.1 for the following parameters: bdcfg_vref_w
W	PI_WDQLVL_VREF_INITIAL_START_POINT_F1	bdcfg_vref_w & 0x00FF	
W	PI_WDQLVL_VREF_INITIAL_START_POINT_F2	bdcfg_vref_w & 0x00FF	
W	PI_WDQLVL_VREF_INITIAL_STOP_POINT_F0	(bdcfg_vref_w & 0xFF00) >> 8	
W	PI_WDQLVL_VREF_INITIAL_STOP_POINT_F1	(bdcfg_vref_w & 0xFF00) >> 8	
W	PI_WDQLVL_VREF_INITIAL_STOP_POINT_F2	(bdcfg_vref_w & 0xFF00) >> 8	

Table 4-19 CA Vref(MR12) Training range

Op.	Bit Name	Data	Description
W	PI_CALVL_VREF_INITIAL_START_POINT_F2	bdcfg_vref_ca & 0x00FF	This part is set when the user setting value is used. See Appendix A1.1 for the following parameters: bdcfg_vref_ca
W	PI_CALVL_VREF_INITIAL_STOP_POINT_F2	(bdcfg_vref_ca & 0xFF00) >> 8	

Table 4-20 PHY Deskew PLL Settings

Op.	Bit Name	Data	Description
W	PHY_PLL_CTRL	0x1342	
W	PHY_PLL_CTRL_8X	0x3342	

Table 4-21 I/O Calibration Settings

Op.	Bit Name	Data	Description
W	PHY_DATA_DC_CAL_CLK_SEL	0x04	
W	PHY_CLK_DC_CAL_CLK_SEL	0x04	
W	PHY_CAL_CLK_SELECT_0	0x05	

Table 4-22 Initial Value Settings of Data Slice

Op.	Bit Name	Data	Description
The Address Offset of the target register is DDR_PHY_SLICE_OFS.			See the table of section 5.2. Set it from the following address: DDR_PHY_SLICE_OFS + 0x100 * n (slice = 0,1)

Table 4-23 Initial Value Settings of Address Slice

Op.	Bit Name	Data	Description
The Address Offset of the target register is DDR_PHY_ADR_V_OFS.			See the table of section 5.2. Set it from the following address: DDR_PHY_ADR_V_OFS

Table 4-24 Initial Value Settings of Address Control Slice

Op.	Bit Name	Data	Description
The Address Offset of the target register is DDR_PHY_ADR_G_OFS.			See the table of section 5.2. Set it from the following address: DDR_PHY_ADR_G_OFS

Table 4-25 Initial Value Settings of PI Register

Op.	Bit Name	Data	Description
The Address Offset of the target register is DDR_PI_OFS.			See the table of section 5.2. Set it from the following address: DDR_PI_OFS

4.2.2.1 Medium Frequency Settings

In this block, PHY register settings for medium frequency are set in the Figure 4-5.

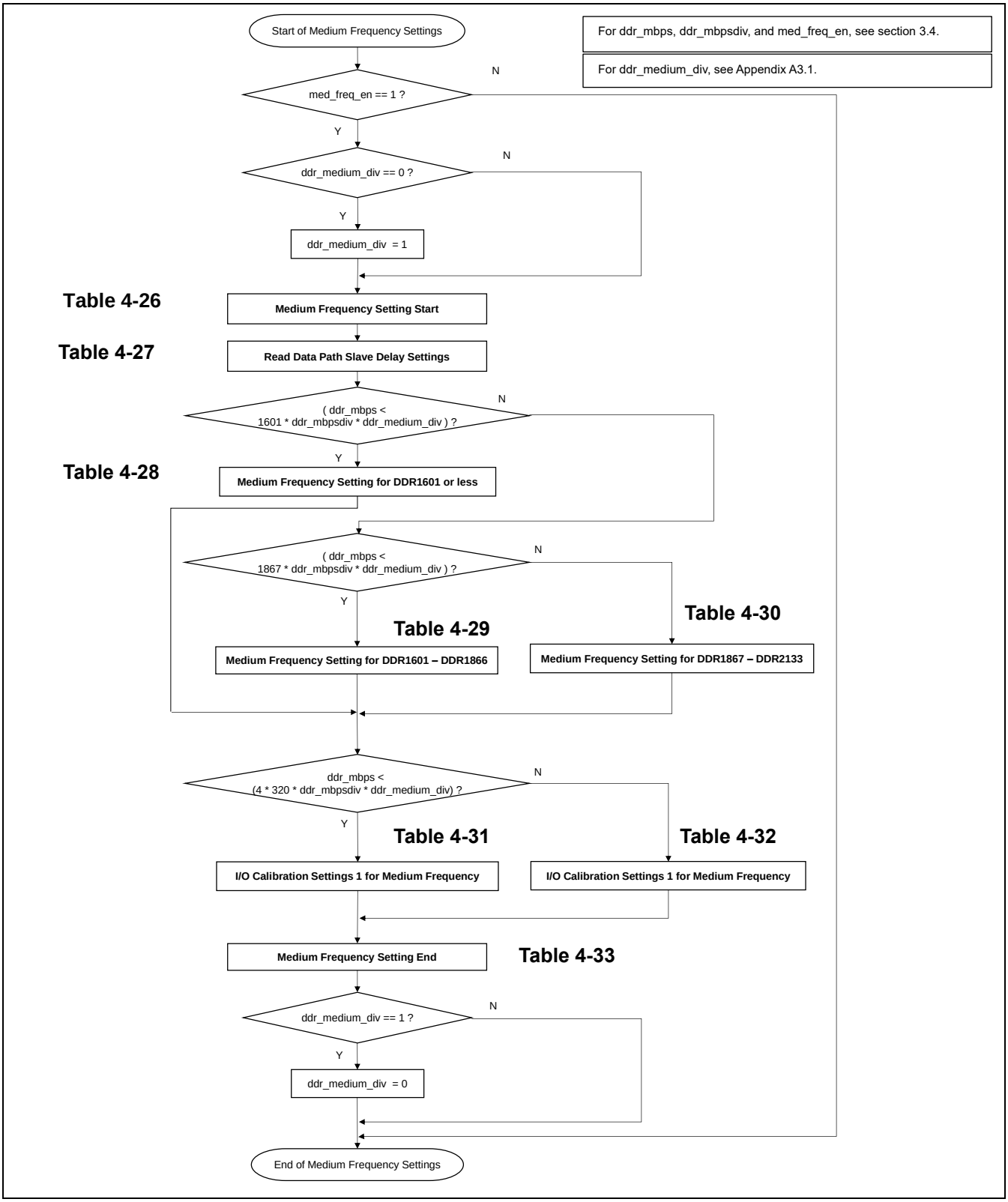


Figure 4-5 Flow of Medium Frequency Settings

Table 4-26 Medium Frequency Setting Start

Op.	Bit Name	Data	Description
W	PHY_FREQ_SEL_MULTICAST_EN	0x00	
W	PHY_FREQ_SEL_INDEX	0x00	

Table 4-27 Read Data Path Slave Delay Settings

Op.	Bit Name	Data	Description
W	PHY_RDDQ0_SLAVE_DELAY	rddq_delay * ddr_mbps * 256 / (ddr_mbpsdiv * 2 * 1000000)	rddq_delay = 103 The following parameters are explained in section 3.4: ddr_mbpsdiv, ddr_mbps. The following parameters are explained in Appendix A3.1: ddr_medium_div.
W	PHY_RDDQ1_SLAVE_DELAY	rddq_delay * ddr_mbps * 256 / (ddr_mbpsdiv * 2 * 1000000)	
W	PHY_RDDQ2_SLAVE_DELAY	rddq_delay * ddr_mbps * 256 / (ddr_mbpsdiv * 2 * 1000000)	
W	PHY_RDDQ3_SLAVE_DELAY	rddq_delay * ddr_mbps * 256 / (ddr_mbpsdiv * 2 * 1000000)	
W	PHY_RDDQ4_SLAVE_DELAY	rddq_delay * ddr_mbps * 256 / (ddr_mbpsdiv * 2 * 1000000)	
W	PHY_RDDQ5_SLAVE_DELAY	rddq_delay * ddr_mbps * 256 / (ddr_mbpsdiv * 2 * 1000000)	
W	PHY_RDDQ6_SLAVE_DELAY	rddq_delay * ddr_mbps * 256 / (ddr_mbpsdiv * 2 * 1000000)	
W	PHY_RDDQ7_SLAVE_DELAY	rddq_delay * ddr_mbps * 256 / (ddr_mbpsdiv * 2 * 1000000)	
W	PHY_RDDM_SLAVE_DELAY	rddq_delay * ddr_mbps * 256 / (ddr_mbpsdiv * 2 * 1000000)	

Table 4-28 Medium Frequency Setting for DDR1601 or less

Op.	Bit Name	Data	Description
W	PHY_REGULATOR_EN_CNT	0x03	
W	PHY_RX_CAL_ALL_DLY	0x04	
W	PHY_RX_PCLK_CLK_SEL	0x02	
W	PHY_RDDATA_EN_TSEL_DLY	0x03	
W	PHY_RDDATA_EN_OE_DLY	0x05	
W	PHY_RPTR_UPDATE	0x06	
W	PHY_WRLVL_RESP_WAIT_CNT	0x12	
W	PHY_RDLVL_MAX_EDGE	0x00F0	
W	PHY_DATA_DC_INIT_DISABLE	0x03	
W	PHY_DATA_DC_WRLVL_ENABLE	0x00	
W	PHY_DATA_DC_WDQLVL_ENABLE	0x00	
W	PHY_RDDATA_EN_DLY	0x05	
W	PHY_GTLVL_LAT_ADJ_START	0x02	
W	PHY_CLK_DC_INIT_DISABLE	0x01	
W	PHY_CSLVL_DLY_STEP	0x02	
W	PHY_LVL_MEAS_DLY_STEP_ENABLE	0x00	
W	PHY_PAD_ACS_RX_PCLK_CLK_SEL	0x02	
W	PHY_PLL_CTRL	0x1542	
W	PHY_PLL_CTRL_8X	0x3542	

Table 4-29 Medium Frequency Setting for DDR1601 - DDR1866

Op.	Bit Name	Data	Description
W	PHY_REGULATOR_EN_CNT	0x03	
W	PHY_RX_CAL_ALL_DLY	0x04	
W	PHY_RX_PCLK_CLK_SEL	0x02	
W	PHY_RDDATA_EN_TSEL_DLY	0x04	
W	PHY_RDDATA_EN_OE_DLY	0x06	
W	PHY_RPTR_UPDATE	0x07	
W	PHY_WRLVL_RESP_WAIT_CNT	0x15	
W	PHY_RDLVL_MAX_EDGE	0x0101	
W	PHY_DATA_DC_INIT_DISABLE	0x03	
W	PHY_DATA_DC_WRLVL_ENABLE	0x00	
W	PHY_DATA_DC_WDQLVL_ENABLE	0x00	
W	PHY_RDDATA_EN_DLY	0x06	
W	PHY_GTLVL_LAT_ADJ_START	0x02	
W	PHY_CLK_DC_INIT_DISABLE	0x01	
W	PHY_CSLVL_DLY_STEP	0x02	
W	PHY_LVL_MEAS_DLY_STEP_ENABLE	0x00	
W	PHY_PAD_ACS_RX_PCLK_CLK_SEL	0x02	
W	PHY_PLL_CTRL	0x1342	
W	PHY_PLL_CTRL_8X	0x3342	

Table 4-30 Medium Frequency Setting for DDR1867 - DDR2133

Op.	Bit Name	Data	Description
W	PHY_REGULATOR_EN_CNT	0x04	
W	PHY_RX_CAL_ALL_DLY	0x05	
W	PHY_RX_PCLK_CLK_SEL	0x02	
W	PHY_RDDATA_EN_TSEL_DLY	0x05	
W	PHY_RDDATA_EN_OE_DLY	0x07	
W	PHY_RPTR_UPDATE	0x07	
W	PHY_WRLVL_RESP_WAIT_CNT	0x17	
W	PHY_RDLVL_MAX_EDGE	0x0112	
W	PHY_DATA_DC_INIT_DISABLE	0x04	
W	PHY_RDDATA_EN_DLY	0x07	
W	PHY_GTLVL_LAT_ADJ_START	0x03	
W	PHY_CLK_DC_INIT_DISABLE	0x00	
W	PHY_CSLVL_DLY_STEP	0x02	
W	PHY_LVL_MEAS_DLY_STEP_ENABLE	0x00	
W	PHY_PAD_ACS_RX_PCLK_CLK_SEL	0x02	
W	PHY_PLL_CTRL	0x1342	
W	PHY_PLL_CTRL_8X	0x3342	

Table 4-31 I/O Calibration Settings 1 for Medium Frequency

Op.	Bit Name	Data	Description
W	PHY_DATA_DC_CAL_CLK_SEL	0x03	
W	PHY_CLK_DC_CAL_CLK_SEL	0x03	
W	PHY_CAL_CLK_SELECT_0	0x04	

Table 4-32 I/O Calibration Settings 2 for Medium Frequency

Op.	Bit Name	Data	Description
W	PHY_DATA_DC_CAL_CLK_SEL	0x04	
W	PHY_CLK_DC_CAL_CLK_SEL	0x04	
W	PHY_CAL_CLK_SELECT_0	0x05	

Table 4-33 Medium Frequency Setting End

Op.	Bit Name	Data	Description
W	PHY_FREQ_SEL_MULTICAST_EN	0x01	

4.2.3 Hardware Configuration Settings of PHY Registers

Hardware configuration settings are made in the order shown in Figure 4-6. The individual blocks in the diagram are explained in section 4.2.3.1. The part of initial values must be modified depending on user system. The related configuration parameters to be set are explained in this section and listed in Appendix A1.1.

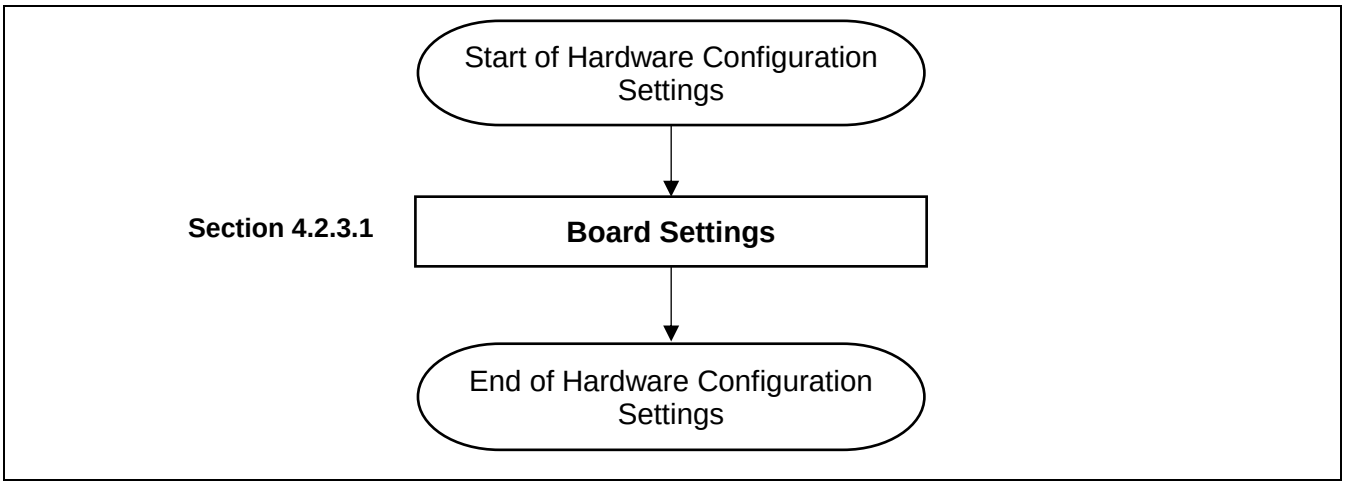


Figure 4-6 Flow of Hardware Configuration Settings

4.2.3.1 Board Settings

In this block, the configuration of the board is set.

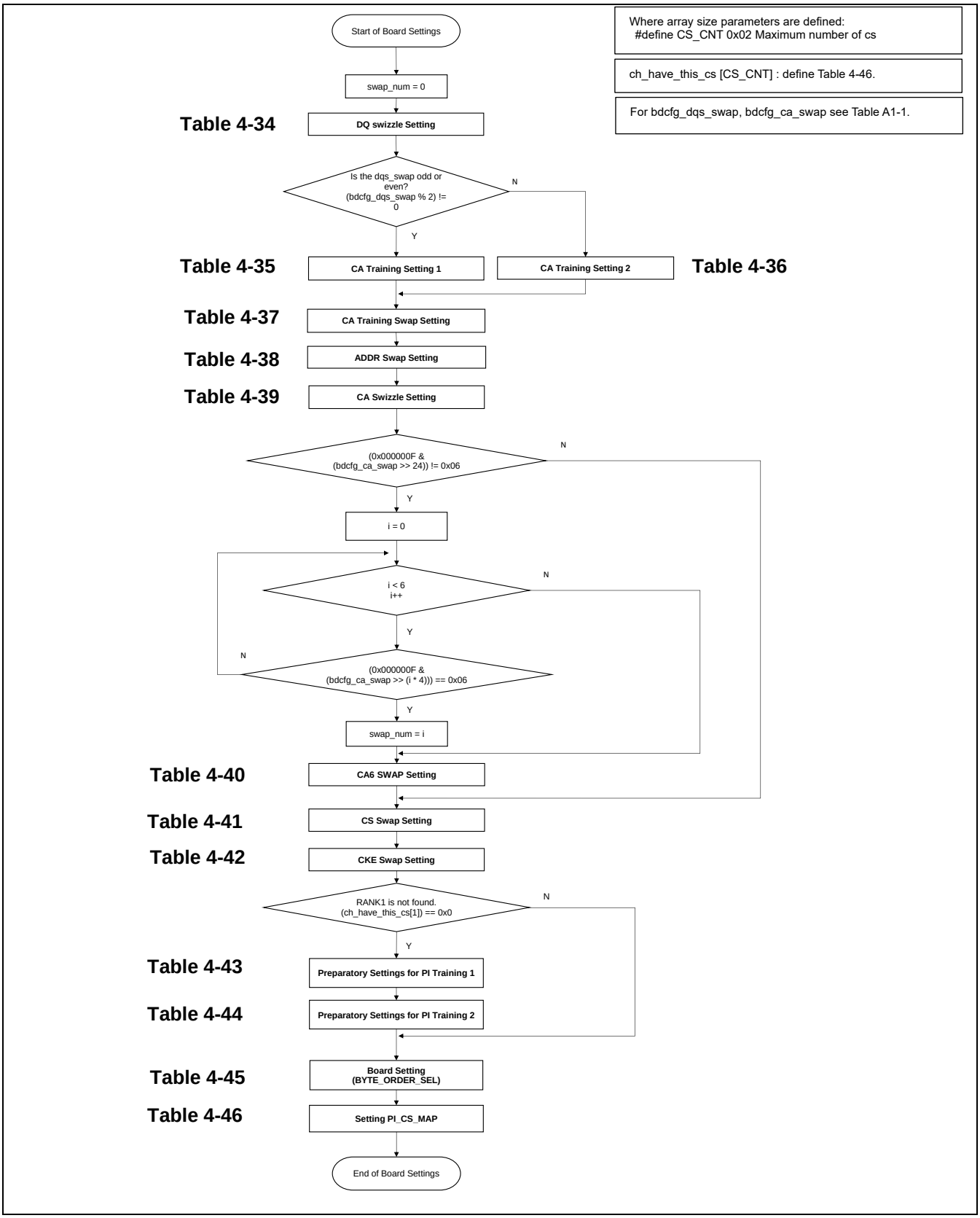


Figure 4-7 Flow of Board Settings

Table 4-34 DQ Swizzle Setting

Op.	Bit Name	Data	Description
W	PHY_DQ_DM_SWIZZLE0	bdcfg_dq_swap	The parameters are explained in Appendix A1.1.
W	PHY_DQ_DM_SWIZZLE1	bdcfg_dm_swap	The parameters are explained in Appendix A1.1.

Table 4-35 CA Training Setting 1

Op.	Bit Name	Data	Description
W	PHY_CALVL_VREF_DRIVING_SLICE	0x00	

Table 4-36 CA Training Setting 2

Op.	Bit Name	Data	Description
W	PHY_CALVL_VREF_DRIVING_SLICE	0x01	

Table 4-37 CA Training Swap Setting

Op.	Bit Name	Data	Description
W	PHY_DATA_BYTE_ORDER_SEL	0x76543200 | (0x000000FF & bdcfg_dqs_swap)	The parameters are explained in Appendix A1.1.

Table 4-38 ADDR Swap Setting

Op.	Bit Name	Data	Description
W	PI_ADDRESS_MUX_0	0x0000000F & bdcfg_ca_swap	The parameters are explained in Appendix A1.1.
W	PI_ADDRESS_MUX_1	0x0000000F & (bdcfg_ca_swap >> 4)	
W	PI_ADDRRSS_MUX_2	0x0000000F & (bdcfg_ca_swap >> 8)	
W	PI_ADDRESS_MUX_3	0x0000000F & (bdcfg_ca_swap >> 12)	
W	PI_ADDRESS_MUX_4	0x0000000F & (bdcfg_ca_swap >> 16)	
W	PI_ADDRESS_MUX_5	0x0000000F & (bdcfg_ca_swap >> 20)	
W	PI_ADDRESS_MUX_6	0x0000000F & (bdcfg_ca_swap >> 24)	

Table 4-39 CA Swizzle Setting

Op.	Bit Name	Data	Description
W	PHY_ADR_CALVL_SWIZZLE0	bdcfg_ca_swap | 0x70000000	The parameters are explained in Appendix A1.1.

Table 4-40 CA6 SWAP Setting

Op.	Bit Name	Data	Description
W	PHY_ADR_CALVL_SWIZZLE0	(((~(0xF0000000 | (0xF << (swap_num * 4)))) & bdcfg_ca_swap) | ((0x0000000F & (bdcfg_ca_swap >> 24)) << (swap_num * 4)) | 0x70000000)	The parameters are explained in Appendix A1.1.
W	PHY_ADR_ADDR_SEL	(((~(0xF0000000 | (0xF << (swap_num * 4)))) & 0x06543210) | (0x6 << (swap_num * 4)))	

Table 4-41 CS Swap Setting

Op.	Bit Name	Data	Description
W	PI_CS_MUX_0	0x0F & bdcfg_cs_swap	The parameters are explained in Appendix A1.1.
W	PI_CS_MUX_1	0x0F & (bdcfg_cs_swap >> 4)	
W	PHY_CS_ACS_ALLOCATION_BIT0_2	0x0F & bdcfg_cs_swap + 1	
W	PHY_CS_ACS_ALLOCATION_BIT1_2	0x0F & (bdcfg_cs_swap >> 4) + 1	

Table 4-42 CKE Swap Setting

Op.	Bit Name	Data	Description
W	PI_CKE_MUX_0	(0x0F & bdcfg_cke_swap) + 2	The parameters are explained in Appendix A1.1.
W	PI_CKE_MUX_1	(0x0F & (bdcfg_cke_swap >> 4)) + 2	

Table 4-43 Preparatory Settings for PI Training 1

Op.	Bit Name	Data	Description
W	PHY_ADR_CALVL_RANK_CTRL	0x00	Initial value is 'b11. See the table of section 5.2. 0x00: DRAM of 1Rank is connected. 0x03: DRAM of 2Ranks is connected.

Table 4-44 Preparatory Settings for PI Training 2

Op.	Bit Name	Data	Description
W	PHY_PER_CS_TRAINING_EN	0x00: DRAM of 1Rank is connected. 0x01: DRAM of 2Ranks is connected.	Initial value is 'b1. See the table of section 5.2.

Table 4-45 Board Setting (BYTE_ORDER_SEL)

Op.	Bit Name	Data	Description
W	PI_DATA_BYTE_SWAP_EN	0x01	
W	PI_DATA_BYTE_SWAP_SLICE0	bdcfg_dqs_swap & 0x0F	The parameters are explained in Appendix A1.1.
W	PI_DATA_BYTE_SWAP_SLICE1	(bdcfg_dqs_swap >> 4) & 0x0F	

Table 4-46 Setting PI_CS_MAP

Op.	Bit Name	Data	Description
W	PI_CS_MAP	0x01	CS_MAP Op. Bit Name Data Description W PI_CS_MAP data Set CS enable / disable for each channel. The correspondence between PI_CS_MAP bit field and CS signals is as: Bit signal ---------- 25 CS1 24 CS0 Initial value of PI_CS_MAP is 'b11 (enable). In the sample code, Matrix (ch_have_this_cs) that indicate w/wo rank (CS) for each channel is prepared from bdcfg_ddr_density (Memory density (Number of rank)), see Appendix A1.1, and bit field of PI_CS_MAP that corresponds to disabled CS are set (because default is enable). ch_have_this_cs [CS_CNT]: Defined by per cs. 2-bit array that identifies whether a rank exists for the channel. Based on the bdcfg_ddr_density information, values of this bit are as follows: Value description ---------- 1: When the ch has a memory. 0: When the ch has no memory.

4.2.4 Settings of the DBSC Registers (Timing)

The DBSC timing registers must be set before DRAM settings is made. In this block, the registers related to DRAM timing are set. See Reference [1].

Table 4-47 Settings of the DBSC Registers (Timing)

Op.	Register Name	Bit	Bit Name	Data	Description
W	DBSC_DBTR(0)	[7:0]	CL	RL	RL and WL are defined in Reference [1].
W	DBSC_DBTR(1)	[7:0]	CWL	WL	
W	DBSC_DBTR(2)	[7:0]	AL	0x00	Fixed. See Reference [3].
W	DBSC_DBTR(3)	[7:0]	TRCD	tRCD	Parameters are defined in Reference [1]. The value of tRCpb is the following formula: tRCpb = tRAS + tRPpb tRCD*, tRPab*, tRPpb*, tRAS*, tRRD*.
W	DBSC_DBTR(4)	[23:16]	TRPA	tRPab	
		[7:0]	TRP	tRPpb	
W	DBSC_DBTR(5)	[7:0]	TRC	tRCpb	
W	DBSC_DBTR(6)	[7:0]	TRAS	tRAS	
W	DBSC_DBTR(7)	[23:16]	TRRD_S	tRRD – 3	
		[7:0]	TRRD	tRRD – 3	
W	DBSC_DBTR(8)	[7:0]	TFAW	tFAW – 4	
W	DBSC_DBTR(9)	[7:0]	TRDPR	nRTP	
W	DBSC_DBTR(10)	[7:0]	TWR	nWR	
W	DBSC_DBTR(11)	[7:0]	TRDWR	RL + (16 / 2) + 1 + 3 – ODTLon + tDQSCK – tODTon,min + PCB delay(out+in) + tPHY_ODToff	RL, ODTLon, and tODTon,min are defined in Reference [1]. PCB delay(out+in) + tPHY_ODToff = Roundup (2.8ns/tCK) tDQSCK*.
W	DBSC_DBTR(12)	[23:16]	TWRRD_S	WL + 1 + (16 / 2) + tWTR	WL and tWTR are defined in Reference [1].
		[7:0]	TWRRD	WL + 1 + (16 / 2) + tWTR	
W	DBSC_DBTR(13)	[15:0]	TRFC/TRFCAB	tRFCab	Parameters are defined in Reference [1].
W	DBSC_DBTR(14)	[23:16]	TCKEHDLL	tXP + 3	Parameters are defined in Reference [1]. The settings must satisfy the following conditions: TCKEH = TCKEHDLL See Reference [3].
		[7:0]	TCKEH	tXP + 3	
W	DBSC_DBTR(15)	[31:24]	TESPD	0x00	Parameters are defined in Reference [1].
		[23:16]	TCKESR	tSR	
		[7:0]	TCKEL	tCKE	

Op.	Register Name	Bit	Bit Name	Data	Description
W	DBSC_DBTR(16)	[31:24]	DQIENLTNCY	RL – 1 – PHY_RDDATA_EN_DLY – (PHY_TWO_CYC_PREAMBLE & 0x01)	RL and WL are defined in Reference [1]. Regarding PHY parameters, see Table 5-3.
		[23:16]	DQL	RL – 1 + PHY_RPTR_UPDATE + PHY_RDDQS_LATENCY_ADJUST + PHY_LPDDR + 18	
		[15:8]	DQENLTNCY	WL – 4	
		[7:0]	WDQL	WL	
W	DBSC_DBTR(17)	[31:24]	TMODRD	tMRR	Parameters are defined in Reference [1].
		[23:16]	TMOD	tMRD	
W	DBSC_DBTR(18)	[26:24]	RODTL	0x0	
		[18:16]	RODTA	0x0	
		[10:8]	WODTL	0x0	
		[2:0]	WODTA	0x0	
W	DBSC_DBTR(19)	[31:16]	TZQCL	0x0000	
		[7:0]	TZQCS	0x0	
W	DBSC_DBTR(20)	[31:16]	TXSDLL	tXSR + 3	Parameters are defined in Reference [1].
		[15:0]	TXS	tXSR + 3	The settings must satisfy the following conditions: TXS = TXSDLL See Reference [3].
W	DBSC_DBTR(21)	[23:16]	TCCD_S	0x8	
		[7:0]	TCCD	0x8 * 2	
W	DBSC_DBTR(22)	[31:16]	TZQCAL	tZQCALns	Parameters are defined in Reference [1].
		[7:0]	TZQLAT	tZQLAT	
W	DBSC_DBTR(23)	[1:0]	RRSPC	0x3	
W	DBSC_DBTR(24)	[31:24]	RDCSGAP	3 + (PHY_TWO_CYC_PREAMBLE & 0x01) + 3	RL and WL are defined in Reference [1]. Regarding PHY parameters, see Table 5-3.
		[23:16]	RDCSLAT	RL – 5 – (PHY_TWO_CYC_PREAMBLE & 0x01)	
		[15:8]	WRCSGAP	6 + 1	
		[7:0]	WRCSLAT	WL – 4 – 5 + 2	
W	DBSC_DBRNK(2)	[7:4]	RKRR1	0x8	
		[3:0]	RKRR0	0x8	
W	DBSC_DBRNK(3)	[7:4]	RKRW1	0x6	
		[3:0]	RKRW0	0x6	
W	DBSC_DBRNK(4)	[7:4]	RKWR1	0x6	
		[3:0]	RKWR0	0x6	
W	DBSC_DBRNK(5)	[7:4]	RKWW1	0xE	
		[3:0]	RKWW0	0xE	

Op.	Register Name	Bit	Bit Name	Data	Description
W	DBSC_DBSCHFCTST0	[31:24]	SCACTACT	1 * tRCpb * bus_clk * ddr_mbpsdiv * 2 / ddr_mbps / bus_clkdiv	Parameters are defined in Reference [1].
		[23:16]	SCRDACT	1 * ((16 / 2) + tRTP – 8 + tRPpb) * bus_clk * ddr_mbpsdiv * 2 / ddr_mbps / bus_clkdiv	The following parameters are explained in section 3.4: ddr_mbpsdiv, ddr_mbps.
		[15:8]	SCWRACT	1 * (WL + 1 + (16 / 2) + nWR) * bus_clk * ddr_mbpsdiv * 2 / ddr_mbps / bus_clkdiv	The following parameters are explained in section 3.6: bus_clk, bus_clkdiv.
		[7:0]	SCPREACT	1 * tRPpb * bus_clk * ddr_mbpsdiv *2 / ddr_mbps / bus_clkdiv	
W	DBSC_DBSCHFCTST1	[31:24]	SCRDWR	1 * TRDWR * bus_clk * ddr_mbpsdiv * 2 / ddr_mbps / bus_clkdiv	Parameters are defined in Reference [1].
		[23:16]	SCWRRD	1 * TWRRD * bus_clk * ddr_mbpsdiv * 2 / ddr_mbps / bus_clkdiv	The following parameters are explained in section 3.4: ddr_mbpsdiv, ddr_mbps.
		[15:8]	SCACTRDWR	1 * tRCD * bus_clk * ddr_mbpsdiv * 2 / ddr_mbps / bus_clkdiv	
		[7:0]	SCASYNCOFS	0x0C	The following parameters are explained in section 3.6: bus_clk, bus_clksdiv.
W	DBSC_DBSCHRW1	[7:0]	SCTRFCAB	tmp = tRFCab + tZQLAT dataL = DQL + 0x50 + tZQLAT + 0x07 1 * dataL * bus_clk * ddr_mbpsdiv * 2 / ddr_mbps / bus_clkdiv : tmp < dataL 1 * tmp * bus_clk * ddr_mbpsdiv * 2 / ddr_mbps / bus_clkdiv : tmp >= dataL	Parameters are defined in Reference [1]. The following parameters are explained in section 3.4: ddr_mbpsdiv, ddr_mbps. The following parameters are explained in section 3.6: bus_clk, bus_clkdiv.
W	DBSC_DBBCAMDIS	—	—	0x00000001	See Reference [3].

Note: For the timing parameters used in the above table, refer to the corresponding documents and sections listed below.
Timing values (RL, WL and so on): Document for Reference [1]
Fixed timing values: Document for Reference [3]
ddr_mbpsdiv and ddr_mbps: Section 3.4
bus_clk and bus_clkdiv: Section 3.6
PHY register values: Section 5.2

Note: * At higher temperatures (>85 degrees), AC timing derating may be required. If derating is required, set JS2_DERATE to 1. (The default value of JS2_DERATE is 0.) See Reference [4] for the temperature derating function of LPDDR4X. And, see Reference [1] for Temperature Derating AC Timing.

4.2.5 Training

Figure 4-8 shows the flow chart of Training. The individual blocks in the diagram are explained from section 4.2.5.1 to section 4.2.5.3.

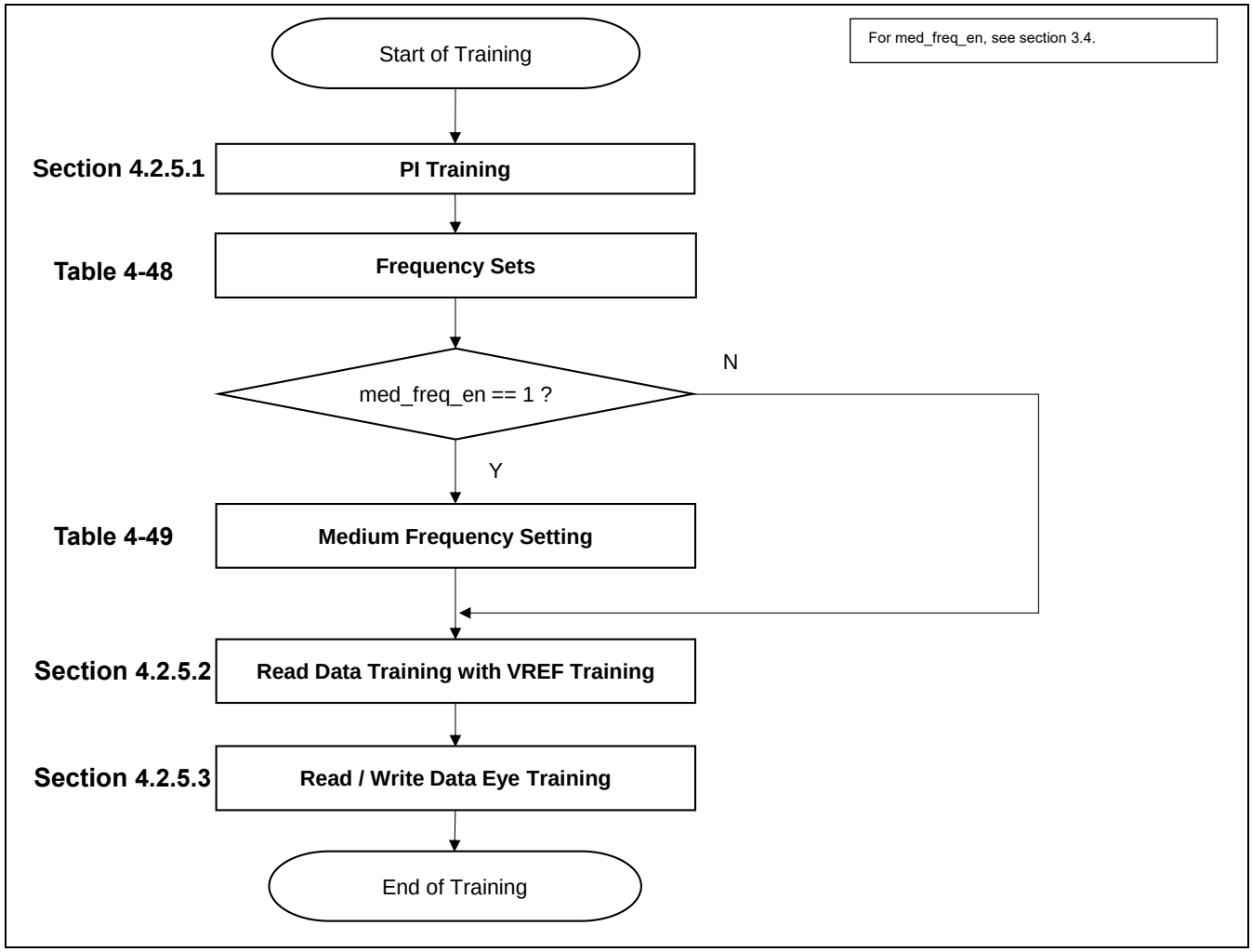


Figure 4-8 Flow of Training

Table 4-48 Frequency Sets

Op.	Register Name	Data	Description
W	PHY_FREQ_SEL_INDEX	0x01	Frequency selection change (F1->F2)
W	PHY_FREQ_SEL_MULTICAST_EN	0x00	Write the value without read-modify-write.

Table 4-49 Medium Frequency Setting

Op.	Register Name	Data	Description
W	PI_WDQLVL_VREF_EN	0x01	
W	PI_FREQ_MAP	0x04	
W	PI_INIT_WORK_FREQ	0x02	

4.2.5.1 PI Training

The following trainings are performed by PI module as in the Figure 4-9, Figure 4-10, and Figure 4-11. During PI training, DFI initialization is performed, these trainings are executed continuously. And, the behavior of this part is different depending on whether the medium frequency settings are enabled or disabled. For details of the differences, refer to the followings.

(1) When medium frequency settings are enabled.

The following trainings are performed on the medium speed. Several switching between medium frequency and low frequency occur to perform CA training with fixed VREF.

- DFI Initialization
- I/O Calibration
- CA Training with fixed VREF
- Write Leveling
- Read Gate Training (DQS gate Training)
- Read Data & RDDQ Training with fixed VREF
- Write DQ Training with fixed VREF

The following trainings are performed on the high speed. Several switching between high frequency and medium frequency occur to perform CA training.

- CA Training
- Write Leveling
- Read Gate Training (DQS gate Training)

(2) When medium frequency settings are disabled.

The following trainings are performed on the high speed. Several switching between high frequency and low frequency occur to perform CA training.

- DFI Initialization
- I/O Calibration
- CA Training
- Write Leveling
- Read Gate Training (DQS gate Training)

1. Figure 4-9 Flow of PI Training
   This flowchart shows the procedure for PI Training.
2. Figure 4-10 Flow of PLL3 Frequency Setting
   This flowchart shows the procedure for setting the frequency of PLL3.
3. Figure 4-11 Flow of PI Training Error Check
   This flowchart shows the procedure for PI Training Error Check.

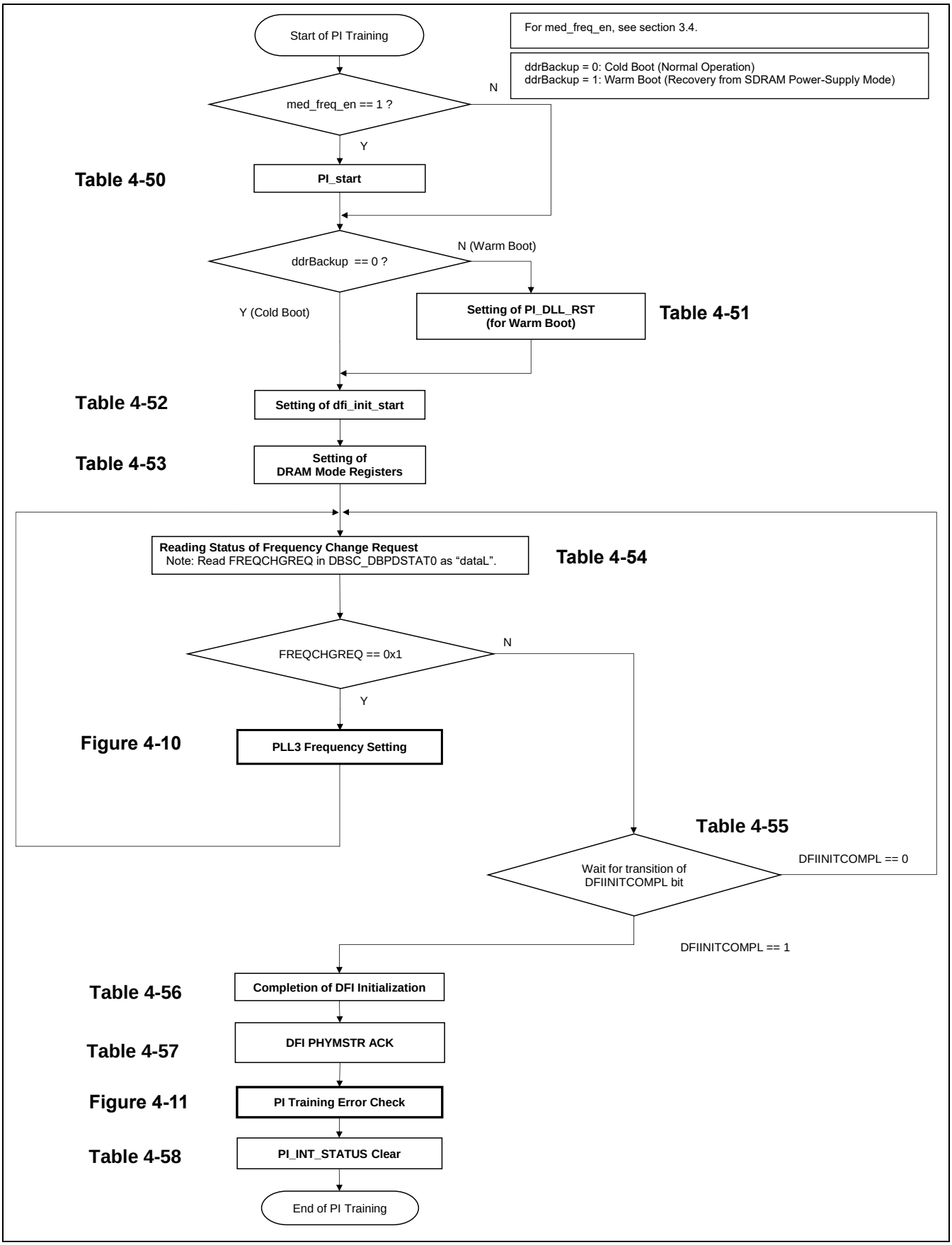


Figure 4-9 Flow of PI Training

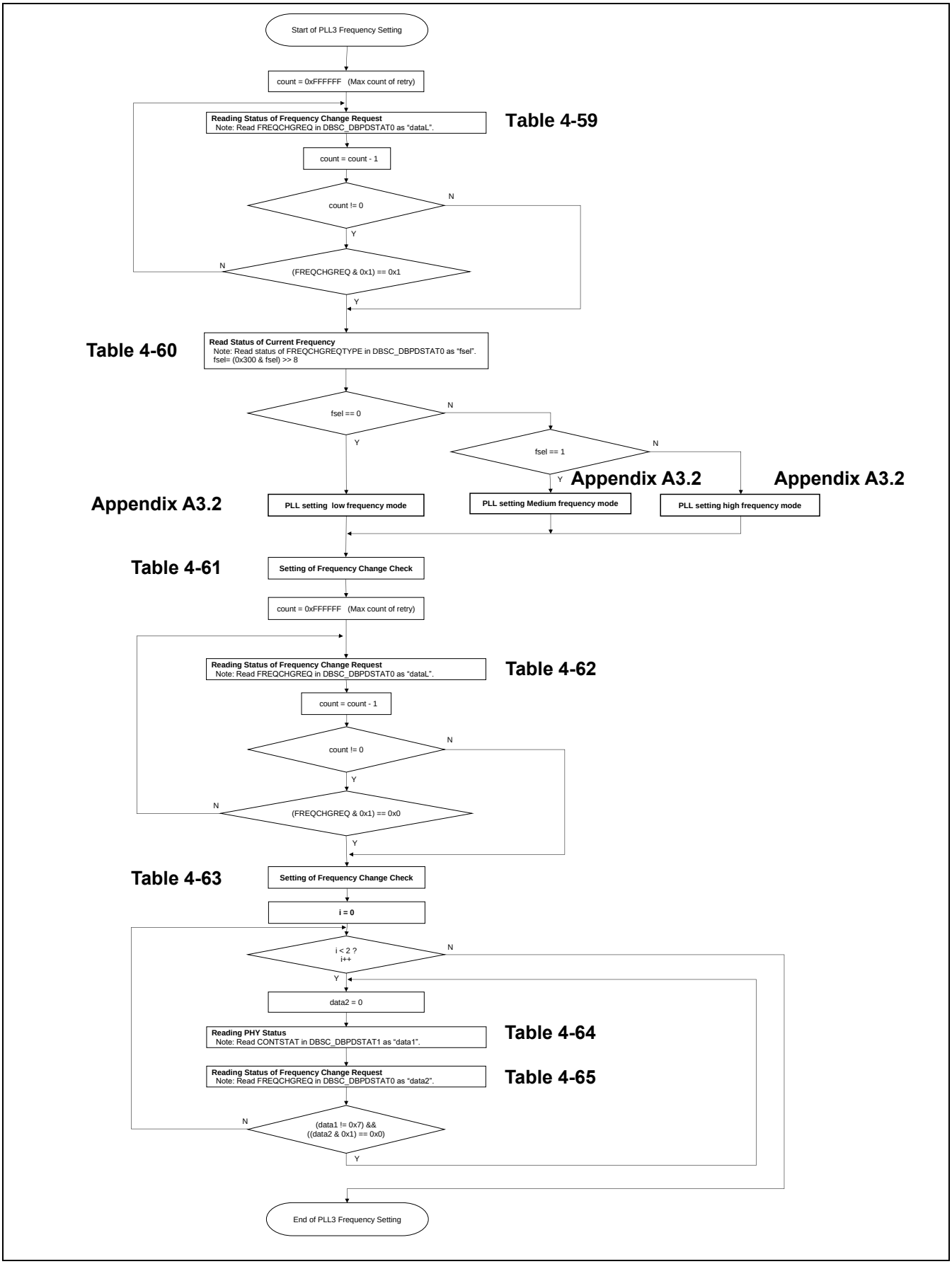


Figure 4-10 Flow of PLL3 Frequency Setting

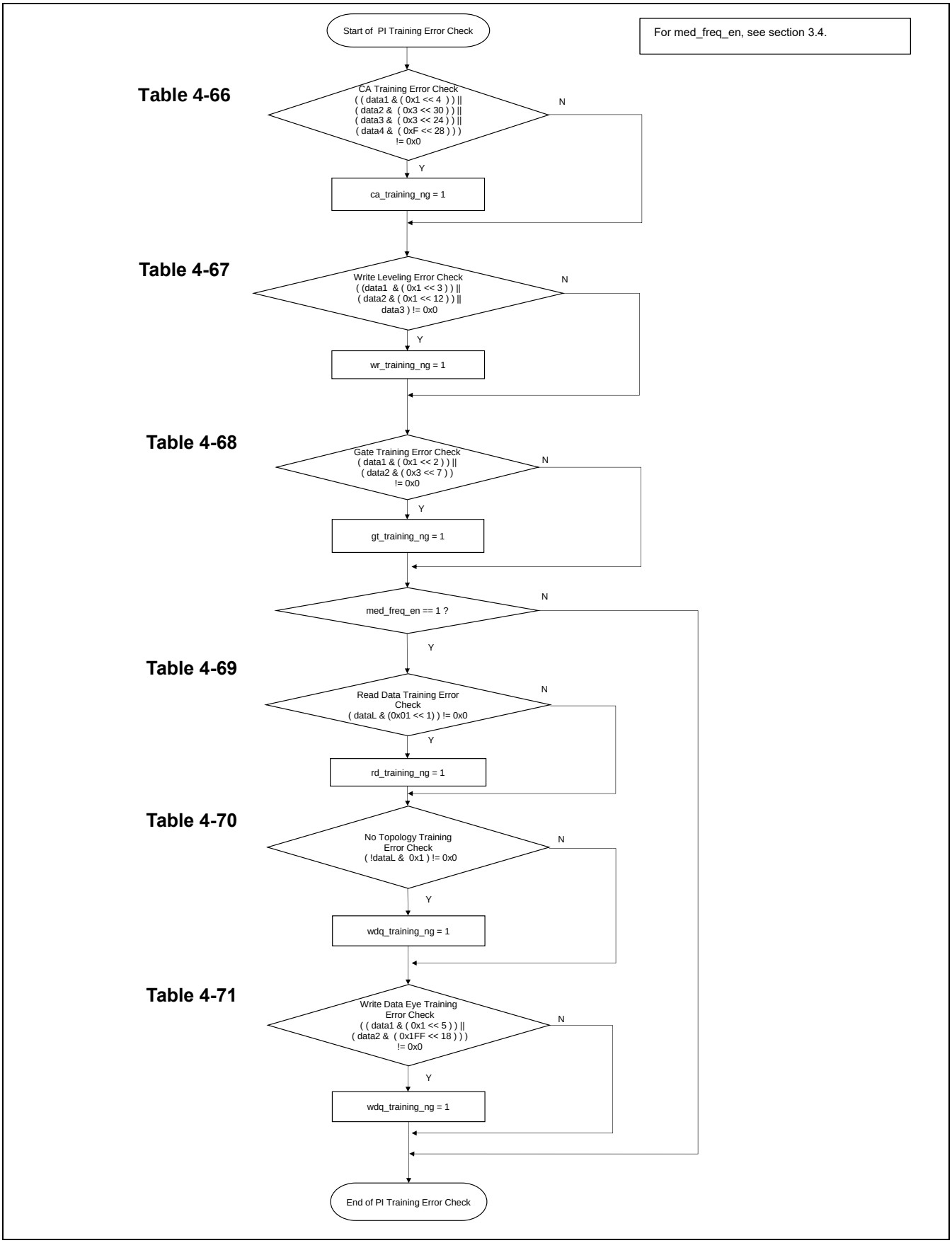


Figure 4-11 Flow of PI Training Error Check

Table 4-50 PI_START

Op.	Register Name	Data	Description
W	PI_FREQ_MAP	0x07	
W	PI_INIT_WORK_FREQ	0x02	
W	PI_CALVL_EN_F1	0x01	
W	PI_WRLVL_EN_F1	0x01	
W	PI_RDLVL_GATE_EN_F1	0x01	
W	PI_RDLVL_EN_F1	0x01	
W	PI_WDQLVL_EN_F1	0x01	
W	PI_RDLVL_RDDQ_EN_F1	0x00	
W	PI_RDLVL_VREF_EN_F1	0x00	
W	PHY_VREF_TRAINING_CTRL	0x00	
W	PI_WDQLVL_VREF_EN	0x00	
W	PI_RDLVL_EN_F2	0x00	
W	PI_WDQLVL_EN_F2	0x00	
W	PI_START	0x01	

Table 4-51 Setting of PI_DLL_RST

Op.	Bit Name	Data	Description
W	PI_DLL_RST	0x01	
W	PI_PWRUP_SREFRESH_EXIT	0x00	

Table 4-52 Setting of dfi_init_start

Op.	Register Name	Bit	Bit Name	Data	Description
W	DBSC_DBDFICNT{m_1}	[28:24]	DFIFREQUENCY{m_1}	0x0	
		[23:16]	DFIBYTEDIS{m_1}	0x0	
		[13:12]	DFIFREQFSP{m_1}	0x0	
		[11:8]	DFICLKDIS{m_1}	0x0	
		[5:4]	DFIFREQRATIO{m_1}	0x1	DBSC5: PHY = 1:2
		[0]	DFIINITSTART{m_1}	0x0	INITSTART = 0
W	DBSC_DBDFICNT{m_1}	[28:24]	DFIFREQUENCY{m_1}	0x0	
		[23:16]	DFIBYTEDIS{m_1}	0x0	
		[13:12]	DFIFREQFSP{m_1}	0x0	
		[11:8]	DFICLKDIS{m_1}	0x0	
		[5:4]	DFIFREQRATIO{m_1}	0x1	DBSC5: PHY = 1:2
		[0]	DFIINITSTART{m_1}	0x1	INITSTART = 1

Table 4-53 Setup of DRAM Mode Registers

Op.	Register Name	Bit	Bit Name	Data	Description
R	DBSC_DBCMD	—	—	—	Dummy read
R	DBSC_DBWAIT	[0]	BUSY	0x0	Wait for the ready of DBSC_DBCMD.
W	DBSC_DBCMD	[31:24]	OPC	0x8	Code = PD Operation = Issue “Power Down Entry/Exit”.
		[23:20]	CH	0x8	A particular physical channel is specified for the operation. CH = 0x8: All channels
		[18:16]	RANK	0x4	A particular rank is specified for the operation. RANK = 0x4: All ranks
		[15:0]	ARG	0x0000	ARG = 0x0000: Enter the power-down mode.
R	DBSC_DBCMD	—	—	—	Dummy read
R	DBSC_DBWAIT	[0]	BUSY	0x0	Wait for the ready of DBSC_DBCMD.
W	DBSC_DBCMD	[31:24]	OPC	0x8	Code = PD Operation = Issue “Power Down Entry/Exit”.
		[23:20]	CH	0x8	A particular physical channel is specified for the operation. CH = 0x8: All channels
		[18:16]	RANK	0x4	A particular rank is specified for the operation. RANK = 0x4: All ranks
		[15:0]	ARG	0x0001	ARG = 0x0001: Exit from the power-down mode.

Note: Use Power Down Entry command to match the internal state of DBSC and DRAM.
Then, use Power Down Exit command to set CKE pins of DRAM to the high level.

Table 4-54 Reading Status of Frequency Change Request

Op.	Register Name	Bit	Bit Name	Data	Description
R	DBSC_DBPDSTAT0{m_1}	[0]	FREQCHGREQ{m_1}	dataL	Read status of FREQCHGREQ as “dataL”.

Table 4-55 Waiting for Transition of DFIINITCOMPL Bit

Op.	Register Name	Bit	Bit Name	Data	Description
R	DBSC_DBDFISTAT{m_1}	[0]	DFIINITCOMPL{m_1}	dataL	Wait for the DFIINITCOMPL bit of DBSC_DBDFISTAT {m_1} to become 1.

Table 4-56 Completion of DFI Initialization

Op.	Register Name	Bit	Bit Name	Data	Description
W	DBSC_DBDFICNT{m_1}	[28:24]	DFIFREQUENCY{m_1}	0x0	
		[23:16]	DFIBYTEDIS{m_1}	0x0	
		[13:12]	DFIFREQFSP{m_1}	0x0	
		[11:8]	DFICLKDIS{m_1}	0x0	
		[5:4]	DFIFREQRATIO{m_1}	0x1	
		[0]	DFIINITSTART{m_1}	0x0	

Table 4-57 DFI PHYMSTR ACK Enable

Op.	Register Name	Bit	Bit Name	Data	Description
W	DBSC_DBDFIPMSTRCNF	[31:6]	—	0x0000000	Reserved
		[5:4]	WTMODE	0x0	DFI PHY expert receive mode
		[3:1]	—	0x0	Reserved
		[0]	PMSTREN	0x1	DFI PHY head control

Table 4-58 Clear Request

Op.	Bit Name	Data	Description
W	PI_INT_ACK_0	0xFFFFFFFF	
W	PI_INT_ACK_1	0x01	

Table 4-59 Reading Status of Frequency Change Request

Op.	Register Name	Bit	Bit Name	Data	Description
R	DBSC_DBPDSTAT0{m_1}	[0]	FREQCHGREQ{m_1}	dataL	Read status of FREQCHGREQ as “dataL”.

Table 4-60 Reading Status of Current Frequency

Op.	Register Name	Bit	Bit Name	Data	Description
R	DBSC_DBPDSTAT0{m_1}	[12:8]	FREQCHGRETYPE{m_1}	fsel	Read status of FREQCHGREQTYPE as “fsel”.

Table 4-61 Setting of Frequency Change Check

Op.	Register Name	Bit	Bit Name	Data	Description
W	DBSC_DBPDCNT{m_1}2	—	—	0x0000CF01	

Table 4-62 Reading Status of Frequency Change Request

Op.	Register Name	Bit	Bit Name	Data	Description
R	DBSC_DBPDSTAT0{m_1}	[0]	FREQCHGREQ{m_1}	dataL	Read status of FREQCHGREQ as “dataL”.

Table 4-63 Setting of Frequency Change Check

Op.	Register Name	Bit	Bit Name	Data	Description
W	DBSC_DBPDCNT{m_1}2	—	—	0x00000000	

Table 4-64 Reading PHY Status

Op.	Register Name	Bit	Bit Name	Data	Description
R	DBSC_DBPDSTAT1{m_1}	[7:0]	CNTSTAT1{m_1}	data1	Read status of CONTSTAT as “data1”.

Table 4-65 Reading Status of Frequency Change Request

Op.	Register Name	Bit	Bit Name	Data	Description
R	DBSC_DBPDSTAT0{m_1}	[0]	FREQCHGREQ{m_1}	data2	Read status of FREQCHGREQ as “data2”.

Table 4-66 Get CA Training Error Information

Op.	Bit Name	Data	Description
R	PI_INT_STATUS	data1	
R	PHY_ADR_CALVL_OBS1	data2	
R	PHY_ADR_CALVL_OBS2	data3	
R	PHY_CSLVL_OBS1	data4	

Table 4-67 Get WCK2CK Training Error Information

Op.	Bit Name	Data	Description
R	PI_INT_STATUS	data1	
R	PHY_WRLVL_STATUS_OBS	data2	
R	PHY_WRLVL_ERROR_OBS	data3	

Table 4-68 Get Read Gate Training Error Information

Op.	Bit Name	Data	Description
R	PI_INT_STATUS	data1	
R	PHY_GTLVL_STATUS_OBS	data2	

Table 4-69 Get Read Data Training Error Information

Op.	Bit Name	Data	Description
R	PI_INT_STATUS	dataL	

Table 4-70 Get No Topology Training Error Information

Op.	Bit Name	Data	Description
R	PHY_NTP_PASS	dataL	

Table 4-71 Get Write Data Eye Training Error Information

Op.	Bit Name	Data	Description
R	PI_INT_STATUS	data1	
R	PHY_WDQLVL_STATUS_OBS	data2	

4.2.5.2 Read Data Training with VREF Training

The following training is performed as in the Figure 4-12 and Figure 4-13.

- Read Data Training with VREF Training

1. Figure 4-12 Flow of Read Data Vref Training
   This flowchart shows the procedure for Read Data Vref Training.
2. Figure 4-13 Flow of Best Vref Setting
   This flowchart shows the procedure for Best Vref Setting.

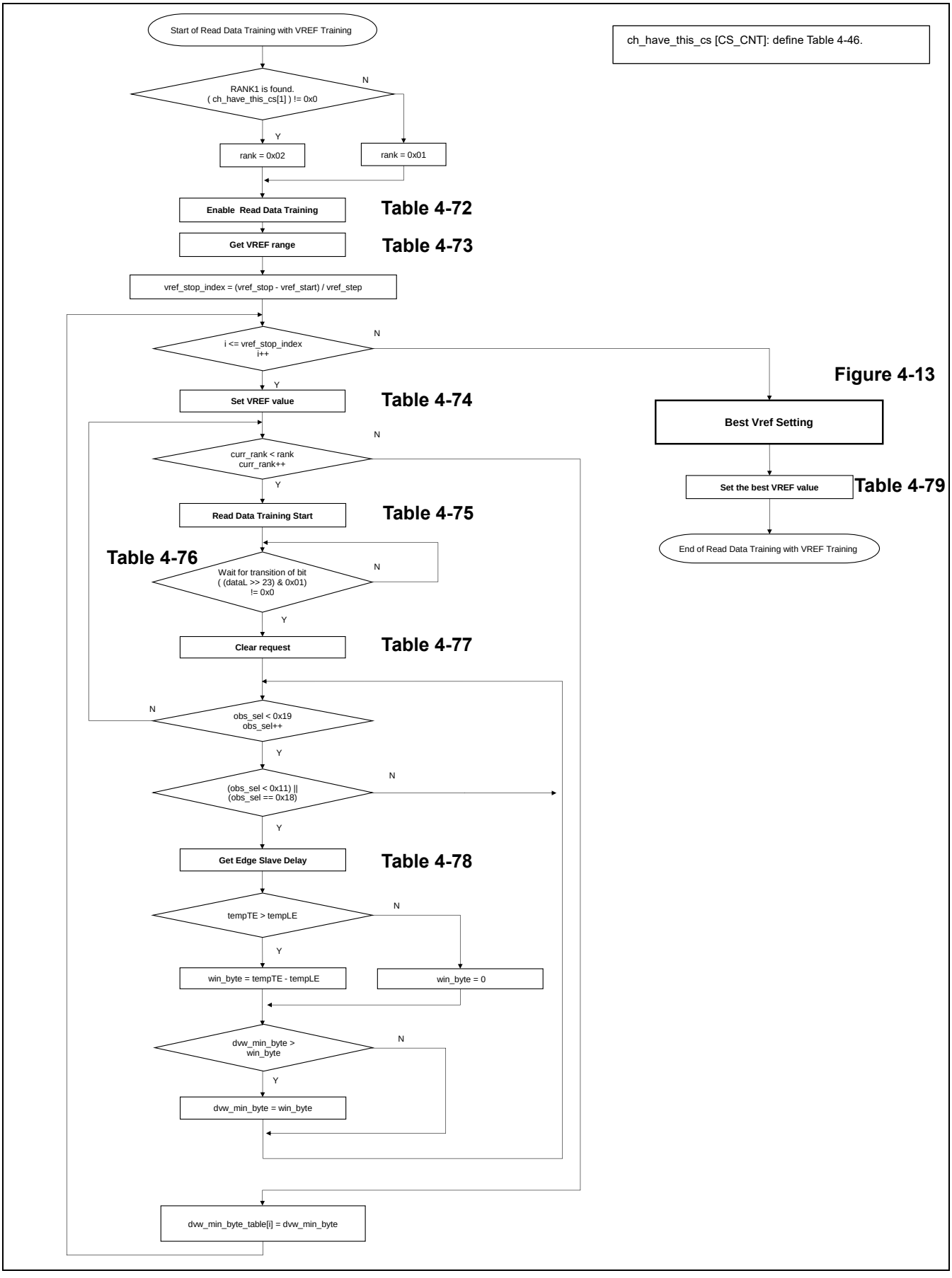


Figure 4-12 Flow of Read Data Vref Training

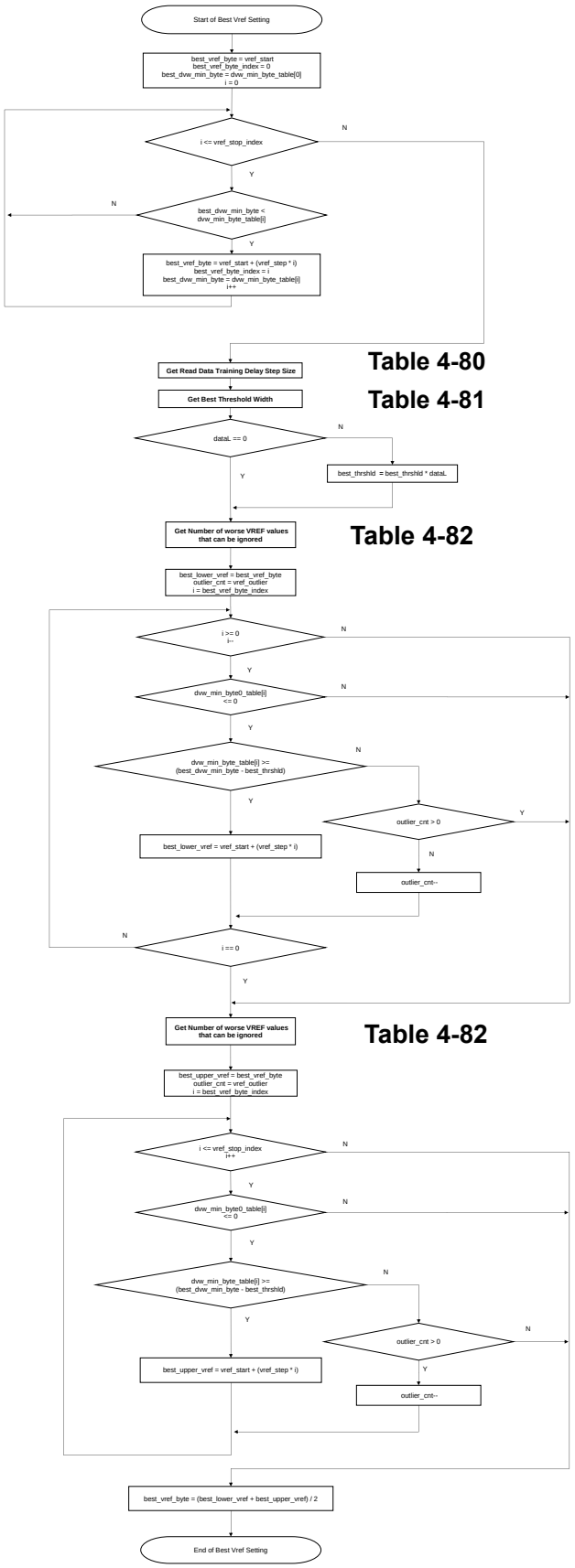


Figure 4-13 Flow of Best Vref Setting

Table 4-72 Enable Read Data Training

Op.	Bit Name	Data	Description
W	PI_RDLVL_EN_F2	0x03	
W	PI_RDLVL_VREF_EN_F0	0x00	
W	PI_RDLVL_VREF_EN_F1	0x00	
W	PI_RDLVL_VREF_EN_F2	0x00	
W	PHY_VREF_TRAINING_CTRL	0x00	

Table 4-73 Get VREF range

Op.	Bit Name	Data	Description
R	PHY_VREF_INITIAL_START_POINT	vref_start	
R	PHY_VREF_INITIAL_STOP_POINT	vref_stop	
R	PHY_VREF_INITIAL_STEPSIZE	vref_step	

Table 4-74 Set VREF value

Op.	Bit Name	Data	Description
R	PHY_PAD_VREF_CTRL_DQ	dataL	
W	PHY_PAD_VREF_CTRL_DQ	((dataL & (0x0F << 10)) | (0x1 << 9) | (vref_start + (vref_step * i)))	

Table 4-75 Read Data Training Start

Op.	Bit Name	Data	Description
W	PI_RDLVL_CS_SW	0x1 << curr_rank	
W	PI_RDLVL_REQ	0x1	

Table 4-76 Wait for Read Data Training Complete

Op.	Bit Name	Data	Description
R	PI_INT_STATUS	dataL	

Table 4-77 Clear request

Op.	Bit Name	Data	Description
W	PI_INT_ACK_0	0x1 << 23	

Table 4-78 Get Edge Slave Delay

Op.	Bit Name	Data	Description
W	PHY_RDLVL_RDDQS_DQ_OBS_SELECT	obs_sel	
R	PHY_RDLVL_RDDQS_DQ_LE_DLY_OBS	tempLE	
R	PHY_RDLVL_RDDQS_DQ_TE_DLY_OBS	tempTE	

Table 4-79 Set the best VREF value

Op.	Bit Name	Data	Description
R	PHY_PAD_VREF_CTRL_DQ	dataL	
W	PHY_PAD_VREF_CTRL_DQ	((dataL & (0x0F << 10)) | (0x1 << 9) | best_vref_byte)	

Table 4-80 Get Read Data Training Delay Step Size

Op.	Bit Name	Data	Description
R	PHY_RDLVL_DLY_STEP	dataL	

Table 4-81 Get Best Threshold Width

Op.	Bit Name	Data	Description
R	PHY_RDLVL_BEST_THRSHLD	best_thrshld	

Table 4-82 Get Number of worse VREF values that can be ignored

Op.	Bit Name	Data	Description
R	PHY_RDLVL_VREF_OUTLIER	vref_outlier	

4.2.5.3 Read/Write Data Eye Training

The following trainings are performed as in the Figure 4-14. These trainings are executed continuously. In this flow, no switching between high frequency and low frequency occurs. The frequency change request in this flow is a necessary procedure to run the trainings.

- Read Data Training (RDLVL Training)
- Write Data Eye Training (WDQLVL Training)

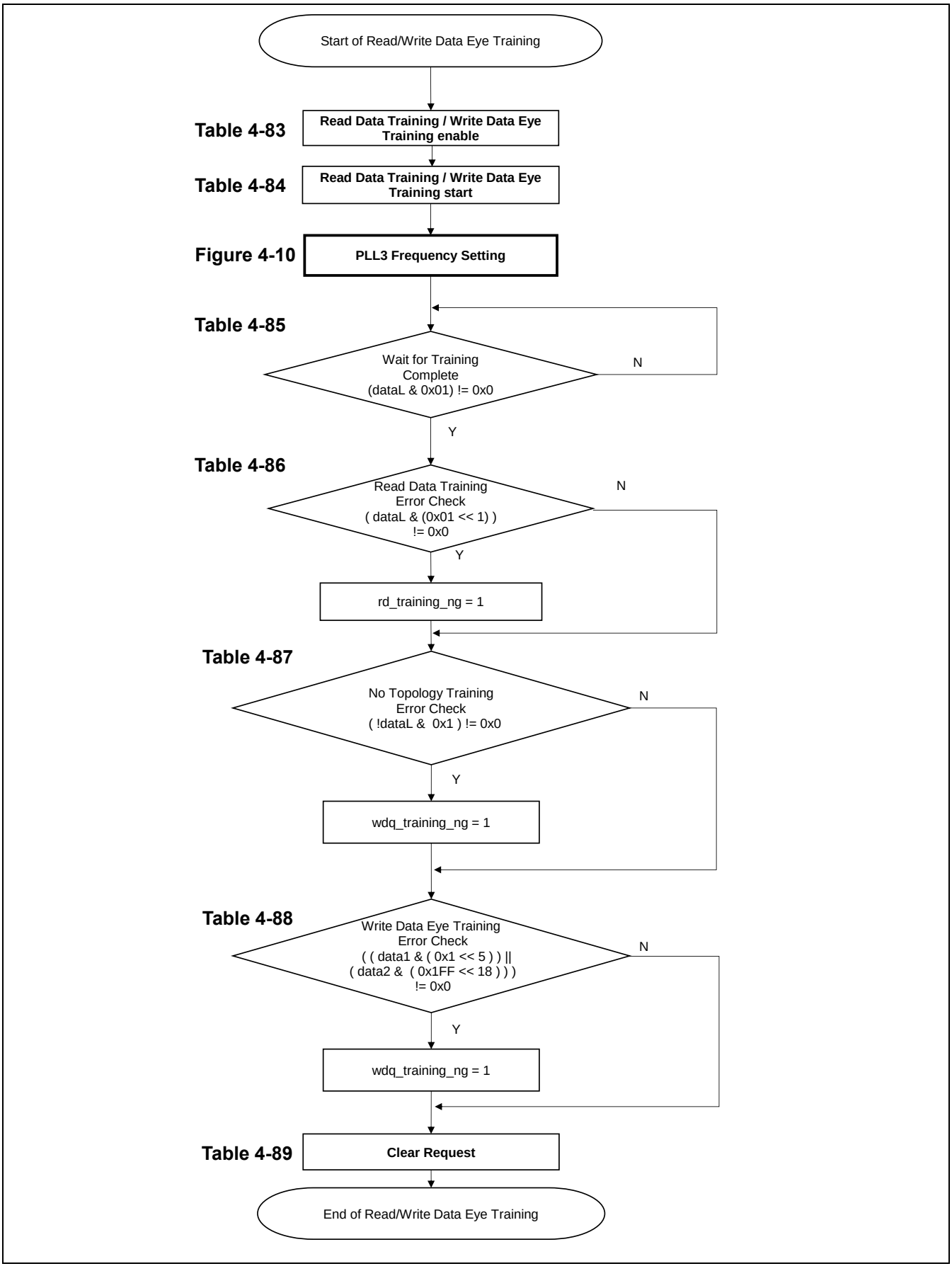


Figure 4-14 Flow of Read/Write Data Eye Training

Table 4-83 Read Data Training / Write Data Eye Training enable

Op.	Bit Name	Data	Description
W	PI_CALVL_EN_F2	0x00	
W	PI_WRLVL_EN_F2	0x00	
W	PI_RDLVL_GATE_EN_F2	0x00	
W	PI_RDLVL_EN_F2	0x03	
W	PI_WDQLVL_EN_F2	0x03	

Table 4-84 Read Data Training / Write Data Eye Training start

Op.	Bit Name	Data	Description
W	PI_SEQ_ARRAY_29	0x181F0000	
W	PI_SEQ_ARRAY_64	0x00000000	
W	PI_TRAIN_ALL_FREQ_REQ	0x01	

Table 4-85 Wait for Training Complete

Op.	Bit Name	Data	Description
R	PI_INT_STATUS	dataL	

Table 4-86 Get Read Data Training Error Information

Op.	Bit Name	Data	Description
R	PI_INT_STATUS	dataL	

Table 4-87 Get No Topology Training Error Information

Op.	Bit Name	Data	Description
R	PHY_NTP_PASS	dataL	

Table 4-88 Get Write Data Eye Training Error Information

Op.	Bit Name	Data	Description
R	PI_INT_STATUS	data1	
R	PHY_WDQLVL_STATUS_OBS	data2	

Table 4-89 Clear Request

Op.	Bit Name	Data	Description
W	PI_INT_ACK_0	0xFFFFFFFF	
W	PI_INT_ACK_1	0x01	

4.2.6 Multi-Cast Setting Disable

Table 4-90 Multi-Cast Setting

Op.	Bit Name	Data	Description
W	PHY_PER_CS_TRAINING_MULTICAST_EN	0x00	

4.2.7 Restore PI_SEQ_ARRAY for DFS

In this block, the configuring DFS settings after initialization is completed in the Figure 4-15.

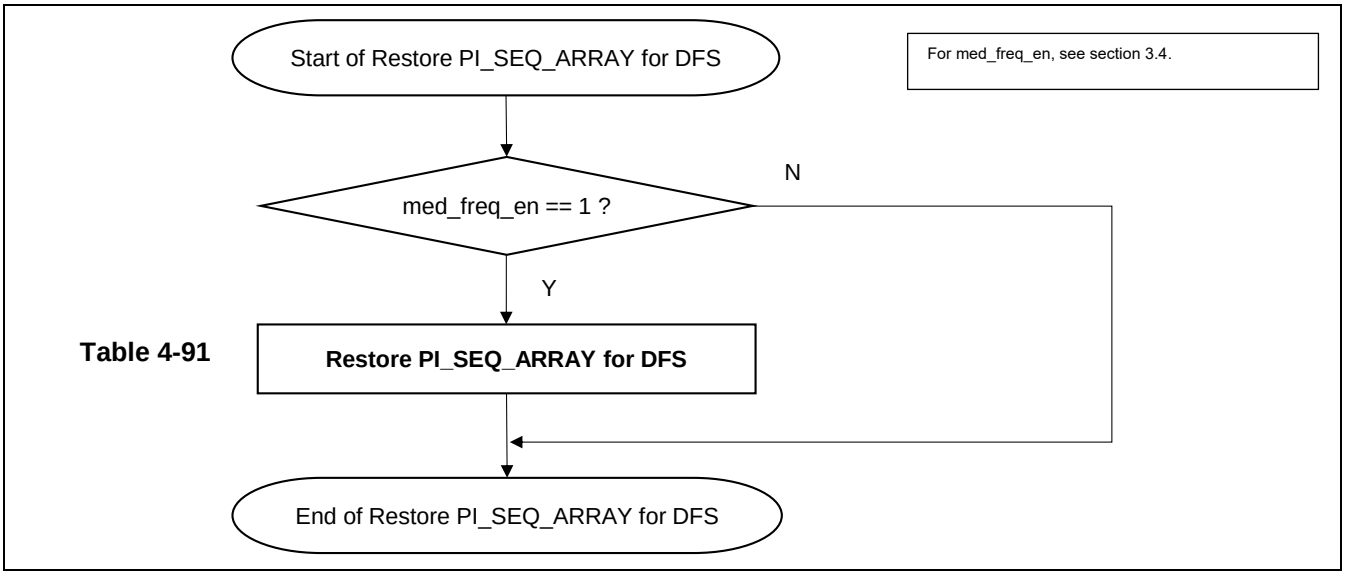


Figure 4-15 Flow of Restore PI_SEQ_ARRAY for DFS

Table 4-91 Restore PI_SEQ_ARRAY for DFS

Op.	Bit Name	Data	Description
W	PI_SEQ_ARRAY_29	0x11910048	
W	PI_SEQ_ARRAY_64	0x19A10D06	
W	PI_FREQ_MAP	0x07	

4.3 DRAM Settings

4.3.1 Settings of DRAM Mode Registers

In this block, DRAM mode registers are set.

Table 4-92 Settings of DRAM Mode Registers

Op.	Register Name	Bit	Bit Name	Data	Description
R	DBSC_DBCMD	—	—	—	Dummy read
R	DBSC_DBWAIT	[0]	BUSY	0x0	Wait for the ready of DBSC_DBCMD.
W	DBSC_DBCMD	[31:24]	OPC	0xE	Code = MRW Operation = Issue MRW.
		[23:20]	CH	0x08	A particular physical channel is specified for the operation. CH = 0x8: All channels
		[18:16]	RANK	0x4	A particular rank is specified for the operation. RANK = 0x4: All ranks
		[15:0]	ARG	0x0A01	Set the value of MA[7:0] in ARG[15:8] and of OP[7:0] in ARG[7:0]. MA[7:0] = 0x0A: MR10 Register OP[7:0] = 0x01: Write value

4.4 DBSC Setting

4.4.1 DBSC Register Setting

DBSC register setting should be done before normal operation. In this block, the registers related to DRAM timings are set.

This block also contains the settings for “Periodic write DQ training” and “Periodic read DQ training”. Not only DBSC/PHY settings but also QoS settings are needed for using these functions. And these functions are controlled by the QoS settings. These functions should be enabled other than for debugging purpose. And this block also contains the settings for “Periodic training separate mode”. For details of this settings, see Appendix A4.

In addition, this block also contains the settings for “DRAM Backup Function”.

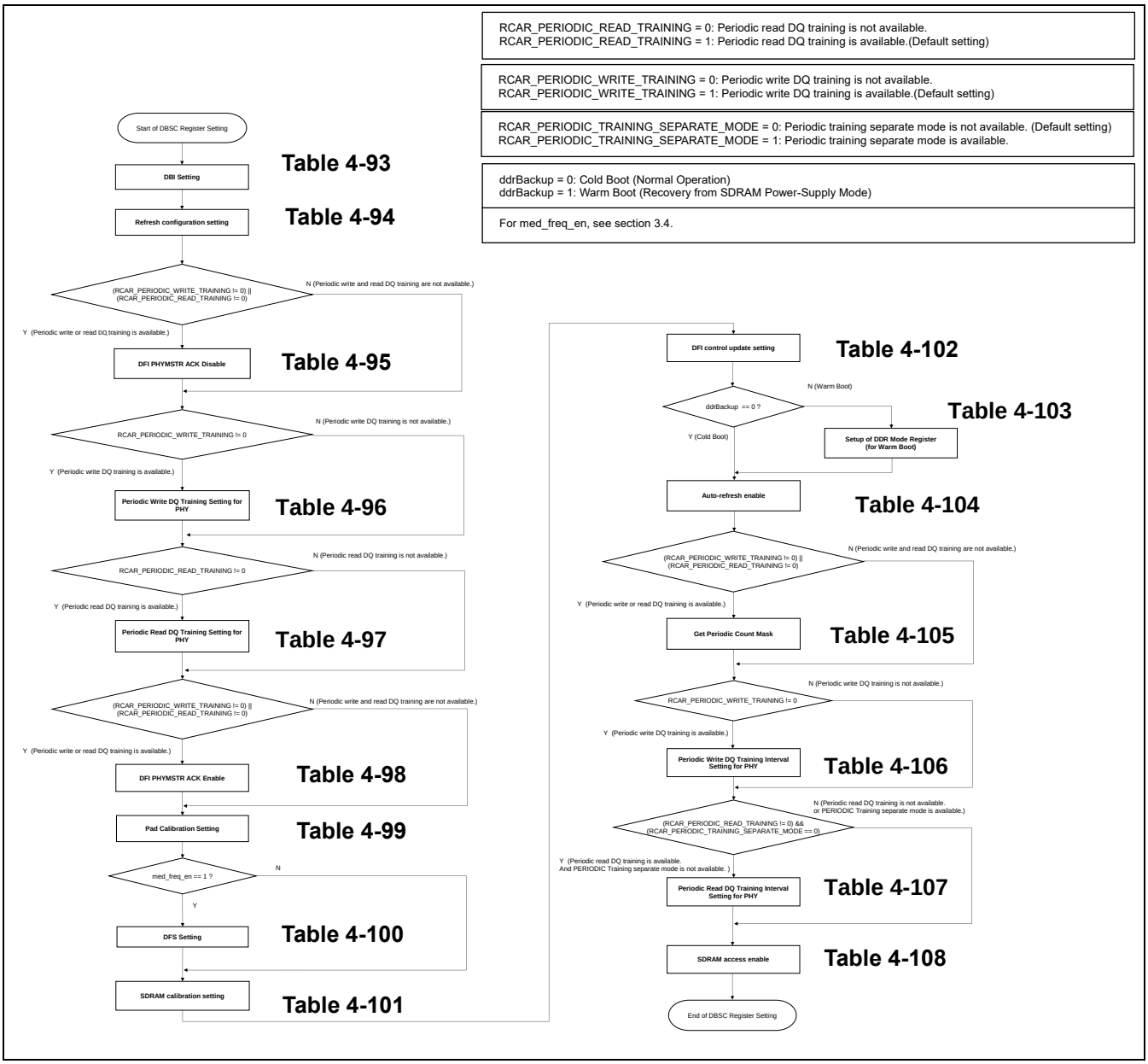


Figure 4-16 Flow of Setting the DBSC Registers

Table 4-93 DBI Setting

Op.	Register Name	Bit	Bit Name	Data	Description
W	DBSC_DBDBICNT	[31:2]	—	0x00000000	Reserved
		[1]	DBIRDEN	0x1	Read DBI setting
		[0]	DBIWREN	0x1	Write DBI setting

Table 4-94 Refresh Configuration Setting

Op.	Register Name	Bit	Bit Name	Data	Description
W	DBSC_DBRFCNF1	[31:16]	REFPMAX	0x0008	
		[15:0]	REFINT	DBSC_REFINT * ddr_mbps / 2000 / ddr_mbpsdiv	DBSC_REFINT = 1920 For details of this settings, see QoS documentation.
W	DBSC_DBRFCNF2	[31:20]	—	0x000	Reserved
		[19:16]	REFPMIN	0x1	Refresh commands setting
		[15:1]	—	0x0000	Reserved
		[0]	REFINTS	DBSC_REFINTS	DBSC_REFINTS = 0: Average interval is REFINT. (default) DBSC_REFINTS = 1: Average interval is 1/2 REFINT.

Table 4-95 DFI PHYMSTR ACK Disable

Op.	Register Name	Bit	Bit Name	Data	Description
W	DBSC_DBDFIPMSTRCNF	[31:6]	—	0x0000000	Reserved
		[5:4]	WTMODE	0x0	DFI PHY expert receive mode
		[3:1]	—	0x0	Reserved
		[0]	PMSTREN	0x0	DFI PHY primary control

Table 4-96 Periodic Write DQ Training Setting for PHY

Op.	Bit Name	Data	Description
W	PI_WDQLVL_EN_F2	0x03	
W	PI_WDQLVL_VREF_EN	0x00	
W	PHY_WDQLVL_QTR_DLY_STEP	0x04	
W	PHY_MEAS_DLY_STEP_ENABLE	0x00	
W	PHY_DATA_DC_WDQLVL_ENABLE	0x00	
W	PI_WDQLVL_PERIODIC	0x01	

Table 4-97 Periodic Read DQ Training Setting for PHY

Op.	Bit Name	Data	Description
W	PI_RDLVL_EN_F2	0x03	
W	PI_RDLVL_VREF_EN_F2	0x00	
W	PHY_RDLVL_DLY_STEP	0x04	
W	PHY_MEAS_DLY_STEP_ENABLE	0x00	
W	PI_RDLVL_PERIODIC	0x01	

Table 4-98 DFI PHYMSTR ACK Enable

Op.	Register Name	Bit	Bit Name	Data	Description
W	DBSC_DBDFIPMSTRCNF	[31:6]	—	0x0000000	Reserved
		[5:4]	WTMODE	0x1	DFI PHY primary receive mode
		[3:1]	—	0x0	Reserved
		[0]	PMSTREN	0x1	DFI PHY head control

Table 4-99 Pad Calibration Setting

Op.	Bit Name	Data	Description
R	PHY_CAL_MODE_0	dataL	
W	PHY_CAL_MODE_0	dataL | 0x02	

Table 4-100 DFS Setting

Op.	Bit Name	Data	Description
W	PI_RDLVL_GATE_EN_F1	0x03	
W	PI_RDLVL_EN_F1	0x01	
W	PI_WDQLVL_EN_F1	0x03	
W	PI_RDLVL_GATE_EN_F2	0x03	
W	PI_RDLVL_EN_F2	0x03	
W	PI_WDQLVL_EN_F2	0x03	

Table 4-101 SDRAM Calibration Setting

Op.	Register Name	Bit	Bit Name	Data	Description
W	DBSC_DBCALCNF	[31:25]	—	0x00	Reserved
		[24]	CALEN	0x1	SDRAM calibration enable
		[23:17]	—	0x00	Reserved
		[16]	CALSL	0x0	Calibration command selection 0: ZQCS
		[15:0]	CALINT	0x0010	SDRAM calibration frequency

Table 4-102 DFI Control Update Setting

Op.	Register Name	Bit	Bit Name	Data	Description
W	DBSC_DBDFICUPDCNF	[31:24]	CUPDREQMAX	0x50	
		[23:16]	CUPDREQMIN	0x4C	
		[15:1]	—	0x0000	
		[0]	CUPDEN	0x1	

Table 4-103 Setup of DRAM Mode Register (for Warm Boot)

Op.	Register Name	Bit	Bit Name	Data	Description
R	DBSC_DBCMD	—	—	—	Dummy read
R	DBSC_DBWAIT	[0]	BUSY	0x0	Wait for the ready of DBSC_DBCMD.
W	DBSC_DBCMD	[31:24]	OPC	0xA	Code = SR Operation = Issue “Self-Refresh Entry/Exit”.
		[23:20]	CH	0x8	A particular physical channel is specified for the operation. CH = 0x8: All channels
		[18:16]	RANK	0x4	A particular rank is specified for the operation. RANK = 0x4: All ranks
		[15:0]	ARG	0x0001	ARG = 0x0001: Exit from the self-refresh mode.

Table 4-104 Auto-Refresh Enable

Op.	Register Name	Bit	Bit Name	Data	Description
W	DBSC_DBRFEN	[31:1]	—	0x00000000	Reserved
		[0]	ARFEN	0x1	Auto-refresh enable

Table 4-105 Get Periodic Count Mask

Op.	Bit Name	Data	Description
R	PI_LONG_COUNT_MASK	count	

Table 4-106 Periodic Write DQ Training Setting for PHY

Op.	Bit Name	Data	Description
W	PI_WDQLVL_INTERVAL	((PERIODIC_TRAINING_INTERVAL – 3000) * (ddr_mbps / ddr_mbpsdiv / 8) / (1024 – count * 32))	PERIODIC_TRAINING_INTERVAL = 20000 For details of this settings, see QoS documentation. The following parameters are explained in section 3.4: ddr_mbpsdiv, ddr_mbps.

Table 4-107 Periodic Read DQ Training Setting for PHY

Op.	Bit Name	Data	Description
W	PI_RDQLVL_INTERVAL	((PERIODIC_TRAINING_INTERVAL – 3000) * (ddr_mbps / ddr_mbpsdiv / 8) / (1024 – count * 32))	PERIODIC_TRAINING_INTERVAL = 20000 For details of this settings, see QoS documentation. The following parameters are explained in section 3.4: ddr_mbpsdiv, ddr_mbps.

Table 4-108 SDRAM Access Enable

Op.	Register Name	Bit	Bit Name	Data	Description
W	DBSC_DBACEN	[31:1]	—	0x00000000	Reserved
		[0]	ACCEN	0x1	SDRAM access enable

4.5 Locking the PHY Registers

Writing 0x00000000 to this register to lock the registers in the PHY unit.

Table 4-109 Locking the PHY Registers

Op.	Register Name	Bit	Bit Name	Data	Description
W	DBSC_DBPDLK{m_1}	[31:0]	PLOCK{m_1}	0x00000000	Locks the PHY registers against access.

5. List of Registers

5.1 List of DBSC Registers

Table 5-1 lists the DBSC registers. For the latest explanation, see Reference [3].

AXI clock domain DBSC0 0xE679 0000
DFI clock domain DBSC0 0xE67A 4000

Table 5-1 DBSC registers

Register Name	Abbreviation	R/W	Value after Reset	Address	Bit Name	Bit
DBSC5 System Configuration Register 0	DBSYSCONF0	R/W	0x0000 0000	DBSC(AXI) + 0000	PCH	[2:0]
DBSC5 System Configuration Register 1	DBSYSCONF1A	R/W	0x0000 0000	DBSC(AXI) + 0004	FREQRATIOA	[1:0]
DBSC5 System Configuration Register 2	DBSYSCONF2A	R/W	0x0000 0000	DBSC(AXI) + 0008	DFICKM	[9]
					CHPOS	[8:3]
					SLI_SCHMDA	[2:0]
Memory Type Register	DBMEMKINDA	R/W	0x0000 0000	DBSC(AXI) + 0020	DDCGA	[3:0]
SDRAM Configuration Setting Register {m_1} {n_2}	DBMEMCONF{m_1} {n_2}A	R/W	0x0000 0000	DBSC(AXI) + 0000 + (0x10 × {m_1}) + (0x4 × {n_2}) + 0x030	DENS{m_1}{n_2}A	[31:30]
					AWRW{m_1}{n_2}A	[28:24]
					AWBG{m_1}{n_2}A	[21:20]
					AWBK{m_1}{n_2}A	[18:16]
					AWCL{m_1}{n_2}A	[11:8]
					DW{m_1}{n_2}A	[1:0]
SDRAM Configuration Setting Register 00	DBMEMCONF00A	R/W	0x0000 0000	DBSC(AXI) + 0030	DENS00A	[31:30]
					AWRW00A	[28:24]
					AWBG00A	[21:20]
					AWBK00A	[18:16]
					AWCL00A	[11:8]
					DW00A	[1:0]
SDRAM Configuration Setting Register 01	DBMEMCONF01A	R/W	0x0000 0000	DBSC(AXI) + 0034	DENS01A	[31:30]
					AWRW01A	[28:24]
					AWBG01A	[21:20]
					AWBK01A	[18:16]
					AWCL01A	[11:8]
					DW01A	[1:0]

Register Name	Abbreviation	R/W	Value after Reset	Address	Bit Name	Bit
SDRAM Configuration Setting Register 10	DBMEMCONF10A	R/W	0x0000 0000	DBSC(AXI) + 0040	DENS10A	[31:30]
					AWRW10A	[28:24]
					AWBG10A	[21:20]
					AWBK10A	[18:16]
					AWCL10A	[11:8]
					DW10A	[1:0]
SDRAM Configuration Setting Register 11	DBMEMCONF11A	R/W	0x0000 0000	DBSC(AXI) + 0044	DENS11A	[31:30]
					AWRW11A	[28:24]
					AWBG11A	[21:20]
					AWBK11A	[18:16]
					AWCL11A	[11:8]
					DW11A	[1:0]
DBSC System Register 0	DBSYSCNT0A	R/W	0x0000 0000	DBSC(AXI) + 0100	REGLOCKA	[15:0]
SDRAM Access Enable Register	DBACEN	R/W	0x0000 0000	DBSC(AXI) + 0200	ACCEN	[0]
SDRAM Operation Setting Register	DBBLA	R/W	0x0000 0000	DBSC(AXI) + 0400	BLA	[1:0]
CAM Unit Operation Setting Register	DBBCAMDIS	R/W	0x0000 0000	DBSC(AXI) + 09FC	RESRDIS	[0]
Read/Write Scheduling Setting Register 1	DBSCHRW1	R/W	0x0000 0000	DBSC(AXI) + 1024	SCTRFCAB	[7:0]
Schedule Timing Setting Register 0	DBSCHFCTST0	R/W	0x0000 0000	DBSC(AXI) + 1040	SCACTACT	[31:24]
					SCRDACT	[23:16]
					SCWRACT	[15:8]
					SCPREACT	[7:0]
Schedule Timing Setting Register 1	DBSCHFCTST1	R/W	0x0000 0000	DBSC(AXI) + 1044	SCRDWR	[31:24]
					SCWRRD	[23:16]
					SCACTRDWR	[15:8]
					SCASYNCOFS	[7:0]
DBSC5 System Configuration Register 1 (for DFI domain)	DBSYSCONF1	R/W	0x0000 0000	DBSC(DFI) + 0000	DDRCKR	[17:16]
					FREQRATIO	[1:0]
DBSC5 System Configuration Register 2	DBSYSCONF2	R/W	0x0000 0000	DBSC(DFI) + 0004	SLI_SCHMDD	[2:0]
PHY Type Configuration Register	DBPHYCONF0	R/W	0x0000 0000	DBSC(DFI) + 0008	PHYTYPE	[1:0]
Memory Type Register	DBMEMKIND	R/W	0x0000 0000	DBSC(DFI) + 0020	DDCG	[3:0]

Register Name	Abbreviation	R/W	Value after Reset	Address	Bit Name	Bit
SDRAM Configuration Setting Register {m_1}{n_2}	DBMEMCONF{m_1}{n_2}	R/W	0x0000 0000	DBSC(DFI) + 0000 + (0x10 × {m_1}) + (0x4 × {n_2}) + 0x030	DENS{m_1}{n_2}	[31:30]
					AWRW{m_1}{n_2}	[28:24]
					AWBG{m_1}{n_2}	[21:20]
					AWBK{m_1}{n_2}	[18:16]
					AWCL{m_1}{n_2}	[11:8]
					DW{m_1}{n_2}	[1:0]
SDRAM Configuration Setting Register 00	DBMEMCONF00	R/W	0x0000 0000	DBSC(DFI) + 0030	DENS00	[31:30]
					AWRW00	[28:24]
					AWBG00	[21:20]
					AWBK00	[18:16]
					AWCL00	[11:8]
					DW00	[1:0]
SDRAM Configuration Setting Register 01	DBMEMCONF01	R/W	0x0000 0000	DBSC(DFI) + 0034	DENS01	[31:30]
					AWRW01	[28:24]
					AWBG01	[21:20]
					AWBK01	[18:16]
					AWCL01	[11:8]
					DW01	[1:0]
SDRAM Configuration Setting Register 10	DBMEMCONF10	R/W	0x0000 0000	DBSC(DFI) + 0040	DENS10	[31:30]
					AWRW10	[28:24]
					AWBG10	[21:20]
					AWBK10	[18:16]
					AWCL10	[11:8]
					DW10	[1:0]
SDRAM Configuration Setting Register 11	DBMEMCONF11	R/W	0x0000 0000	DBSC(DFI) + 0044	DENS11	[31:30]
					AWRW11	[28:24]
					AWBG11	[21:20]
					AWBK11	[18:16]
					AWCL11	[11:8]
					DW11	[1:0]
DBSC System Register 0	DBSYSCNT0	R/W	0x0000 0000	DBSC(DFI) + 0100	REGLOCK	[15:0]
Auto-Refresh Enable Register	DBRFEN	R/W	0x0000 0000	DBSC(DFI) + 0204	ARFEN	[0]
Manual Command-Issuing Register	DBCMD	R/W	0x0000 0000	DBSC(DFI) + 0208	OPC	[31:24]
					CH	[23:20]
					RANK	[18:16]
					ARG	[15:0]
Operation Completion Waiting Register	DBWAIT	R	0x0000 0000	DBSC(DFI) + 0210	BUSY	[0]

Register Name	Abbreviation	R/W	Value after Reset	Address	Bit Name	Bit
SDRAM Timing Register 0	DBTR0	R/W	0x0000 0000	DBSC(DFI) + 0300	CL	[7:0]
SDRAM Timing Register 1	DBTR1	R/W	0x0000 0000	DBSC(DFI) + 0304	CWL	[7:0]
SDRAM Timing Register 2	DBTR2	R/W	0x0000 0000	DBSC(DFI) + 0308	AL	[7:0]
SDRAM Timing Register 3	DBTR3	R/W	0x0000 0000	DBSC(DFI) + 030C	TRCD	[7:0]
SDRAM Timing Register 4	DBTR4	R/W	0x0000 0000	DBSC(DFI) + 0310	TRPA	[23:16]
					TRP	[7:0]
SDRAM Timing Register 5	DBTR5	R/W	0x0000 0000	DBSC(DFI) + 0314	TRC	[7:0]
SDRAM Timing Register 6	DBTR6	R/W	0x0000 0000	DBSC(DFI) + 0318	TRAS	[7:0]
SDRAM Timing Register 7	DBTR7	R/W	0x0000 0000	DBSC(DFI) + 031C	TRRD_S	[23:16]
					TRRD	[7:0]
SDRAM Timing Register 8	DBTR8	R/W	0x0000 0000	DBSC(DFI) + 0320	TFAW	[7:0]
SDRAM Timing Register 9	DBTR9	R/W	0x0000 0000	DBSC(DFI) + 0324	TRDPR	[7:0]
SDRAM Timing Register 10	DBTR10	R/W	0x0000 0000	DBSC(DFI) + 0328	TWR	[7:0]
SDRAM Timing Register 11	DBTR11	R/W	0x0000 0000	DBSC(DFI) + 032C	TRDWR	[7:0]
SDRAM Timing Register 12	DBTR12	R/W	0x0000 0000	DBSC(DFI) + 0330	TWRRD_S	[23:16]
					TWRRD	[7:0]
SDRAM Timing Register 13	DBTR13	R/W	0x0000 0000	DBSC(DFI) + 0334	TRFC/TRFCAB	[15:0]
SDRAM Timing Register 14	DBTR14	R/W	0x0000 0000	DBSC(DFI) + 0338	TCKEHDLL	[23:16]
					TCKEH	[7:0]
SDRAM Timing Register 15	DBTR15	R/W	0x0000 0000	DBSC(DFI) + 033C	TESPD	[31:24]
					TCKESR	[23:16]
					TCKEL	[7:0]
SDRAM Timing Register 16	DBTR16	R/W	0x0000 0000	DBSC(DFI) + 0340	DQIENLTNCY	[31:24]
					DQL	[23:16]
					DQENLTNCY	[15:8]
					WDQL	[7:0]
SDRAM Timing Register 17	DBTR17	R/W	0x0000 0000	DBSC(DFI) + 0344	TMODRD	[31:24]
					TMOD	[23:16]
SDRAM Timing Register 18	DBTR18	R/W	0x0000 0000	DBSC(DFI) + 0348	RODTL	[26:24]
					RODTA	[18:16]
					WODTL	[10:8]
					WODTA	[2:0]
SDRAM Timing Register 19	DBTR19	R/W	0x0000 0000	DBSC(DFI) + 034C	TZQCL	[31:16]
					TZQCS	[7:0]

Register Name	Abbreviation	R/W	Value after Reset	Address	Bit Name	Bit
SDRAM Timing Register 20	DBTR20	R/W	0x0000 0000	DBSC(DFI) + 0350	TXSDLL	[31:16]
					TXS	[15:0]
SDRAM Timing Register 21	DBTR21	R/W	0x0000 0000	DBSC(DFI) + 0354	TCCD_S	[23:16]
					TCCD	[7:0]
SDRAM Timing Register 22	DBTR22	R/W	0x0000 0000	DBSC(DFI) + 0358	TZQCAL	[31:16]
					TZQLAT	[7:0]
SDRAM Timing Register 23	DBTR23	R/W	0x0000 0000	DBSC(DFI) + 035C	RRSPC	[1:0]
SDRAM Timing Register 24	DBTR24	R/W	0x0000 0000	DBSC(DFI) + 0360	RDCSGAP	[31:24]
					RDCSLAT	[23:16]
					WRCSGAP	[15:8]
					WRCSLAT	[7:0]
SDRAM Operation Setting Register	DBBL	R/W	0x0000 0000	DBSC(DFI) + 0400	BL	[1:0]
Refresh Configuration Register 1	DBRFCNF1	R/W	0x0000 0000	DBSC(DFI) + 0414	REFPMAX	[31:16]
					REFINT	[15:0]
Refresh Configuration Register 2	DBRFCNF2	R/W	0x0000 0000	DBSC(DFI) + 0418	REFPMIN	[19:16]
					REFINTS	[1:0]
SDRAM Calibration Configuration Register	DBCALCNF	R/W	0x0000 0000	DBSC(DFI) + 0424	CALEN	[24]
					CALINT	[15:0]
Multirank Operation Setting Register 2	DBRNK2	R/W	0x0000 0000	DBSC(DFI) + 0438	RKRR1	[7:4]
					RKRR0	[3:0]
Multirank Operation Setting Register 3	DBRNK3	R/W	0x0000 0000	DBSC(DFI) + 043C	RKRW1	[7:4]
					RKRW0	[3:0]
Multirank Operation Setting Register 4	DBRNK4	R/W	0x0000 0000	DBSC(DFI) + 0440	RKWR1	[7:4]
					RKWR0	[3:0]
Multirank Operation Setting Register 5	DBRNK5	R/W	0x0000 0000	DBSC(DFI) + 0444	RKWW1	[7:4]
					RKWW0	[3:0]
DBI Configuration Register	DBDBICNT	R/W	0x0000 0000	DBSC(DFI) + 0518	DBIRDEN	[1]
					DBIWREN	[0]
DFI PHY Master Control Register	DBDFIPMSTRCNF	R/W	0x0000 0000	DBSC(DFI) + 0520	WTMODE	[5:4]
					PMSTREN	[0]
DFI Control Update Configuration Register	DBDFICUPDCNF	R/W	0x0000 0000	DBSC(DFI) + 0540	CUPDREQMAX	[31:24]
					CUPDREQMIN	[23:16]
					CUPDEN	[0]
DFI Status Interface Input Register {m_1}	DBDFISTAT{m_1}	R	0x0000 0000	DBSC(DFI) + 0600 + (0x40 × {m_1})	DFIINITCOMPL{m_1}	[0]
DFI Status Interface Input Register 0	DBDFISTAT0	R	0x0000 0000	DBSC(DFI) + 0600	DFIINITCOMPL0	[0]

Register Name	Abbreviation	R/W	Value after Reset	Address	Bit Name	Bit
DFI Status Interface Output Register {m_1}	DBDFICNT{m_1}	R/W	0x0000 0000	DBSC(DFI) + 0604 + (0x40 × {m_1})	DFIFREQUENCY{m_1}	[28:24]
					DFIBYTEDIS{m_1}	[23:16]
					DFIFREQFSP{m_1}	[13:12]
					DFICLKDIS{m_1}	[11:8]
					DFIFREQRATIO{m_1}	[5:4]
					DFIINITSTART{m_1}	[0]
DFI Status Interface Output Register 0	DBDFICNT0	R/W	0x0000 0000	DBSC(DFI) + 0604	DFIFREQUENCY0	[28:24]
					DFIBYTEDIS0	[23:16]
					DFIFREQFSP0	[13:12]
					DFICLKDIS0	[11:8]
					DFIFREQRATIO0	[5:4]
					DFIINITSTART0	[0]
PHY Unit Control Register {m_1}2	DBPDCNT{m_1}2	R/W	0x0000 0000	DBSC(DFI) + 0618 + (0x40 × {m_1})	CNTREG{m_1}2	[31:0]
PHY Unit Control Register 02	DBPDCNT02	R/W	0x0000 0000	DBSC(DFI) + 0618	CNTREG02	[31:0]
PHY Unit Lock Register {m_1}	DBPDLK{m_1}	R/W	0x0000 0000	DBSC(DFI) + 0620 + (0x40 × {m_1})	PLOCK{m_1}	[31:0]
PHY Unit Lock Register 0	DBPDLK0	R/W	0x0000 0000	DBSC(DFI) + 0620	PLOCK0	[31:0]
PHY Unit Register Address {m_1}	DBPDRGA{m_1}	R/W	0x0000 0000	DBSC(DFI) + 0624 + (0x40 × {m_1})	PRA{m_1}	[15:0]
PHY Unit Register Address 0	DBPDRGA0	R/W	0x0000 0000	DBSC(DFI) + 0624	PRA0	[15:0]
PHY Unit Register Access {m_1}	DBPDRGD{m_1}	R/W	Undefined	DBSC(DFI) + 0628 + (0x40 × {m_1})	PRD{m_1}	[31:0]
PHY Unit Register Access 0	DBPDRGD0	R/W	Undefined	DBSC(DFI) + 0628	PRD0	[31:0]
PHY Unit Register Mask{m_1}	DBPDRGM{m_1}	R/W	0x0000 0000	DBSC(DFI) + 062C + (0x40 × {m_1})	PRM{m_1}	[3:0]
PHY Unit Register Mask 0	DBPDRGM0	R/W	0x0000 0000	DBSC(DFI) + 062C	PRM0	[3:0]
PHY Status Register 00	DBPDSTAT00	R	0x0000 0000	DBSC(DFI) + 0630	CNTSTAT00	[31:0]
PHY Status Register 01	DBPDSTAT01	R	0x0000 0000	DBSC(DFI) + 0634	CNTSTAT01	[7:0]
DFI Status Interface Input Register 1	DBDFISTAT1	R	0x0000 0000	DBSC(DFI) + 0640	DFIINITCOMPL1	[0]

Register Name	Abbreviation	R/W	Value after Reset	Address	Bit Name	Bit
DFI Status Interface Output Register 1	DBDFICNT1	R/W	0x0000 0000	DBSC(DFI) + 0644	DFIFREQUENCY1	[28:24]
					DFIBYTEDIS1	[23:16]
					DFIFREQFSP1	[13:12]
					DFICLKDIS1	[11:8]
					DFIFREQRATIO1	[5:4]
					DFIINITSTART1	[0]
PHY Unit Control Register 12	DBPDCNT12	R/W	0x0000 0000	DBSC(DFI) + 0658	FREQCHGACK1	[15:0]
PHY Unit Lock Register 1	DBPDLK1	R/W	0x0000 0000	DBSC(DFI) + 0660	PLOCK1	[31:0]
PHY Unit Register Address 1	DBPDRGA1	R/W	0x0000 0000	DBSC(DFI) + 0664	PRA1	[15:0]
PHY Unit Register Access 1	DBPDRGD1	R/W	Undefined	DBSC(DFI) + 0668	PRD1	[31:0]
PHY Unit Register Mask 1	DBPDRGM1	R/W	0x0000 0000	DBSC(DFI) + 066C	PRM1	[3:0]
PHY Status Register 10	DBPDSTAT10	R	0x0000 0000	DBSC(DFI) + 0670	CNTSTAT10	[31:0]
PHY Status Register 11	DBPDSTAT11	R	0x0000 0000	DBSC(DFI) + 0674	CNTSTAT11	[7:0]

5.2 List of PHY Registers

The correspondences between “Bit Name” (PHY parameter), “Register Name”, and “Bit” for PHY registers are explained in this section. Initial values for each PHY parameter and register are also listed. The address offsets of PHY registers used in the succeeding tables are summarized in Table 5-2. The actual correspondences between “Bit Name” (PHY parameter), “Register Name/Address”, “Bit” and their initial values are listed in Table 5-3. Finally, the names, addresses, and initial values of registers are listed in Table 5-4.

Note: These initial values are overridden as described in section 4.2.2.

Table 5-2 Address Offset of PHY Registers

Address offset	V4M
DDR_PHY_SLICE_OFS	0x1000
DDR_PHY_ADR_V_OFS	0x1200
DDR_PHY_ADR_G_OFS	0x1300
DDR_PI_OFS	0x800

Table 5-3 Correspondence between “Bit Name” (PHY parameter), “Register Name/Address”, “Bit” and their Initial Values

Register addresses are calculated as “Address Offset + n” in the following ways:

DDR_PHY_SLICE_REGSET_OFS + slice * (0x100) + n (slice = 0,1),
DDR_PHY_ADR_[V|G]_REGSET_OFS + n,
DDR_PI_REGSET_OFS + n.

Register names are obtained by replacing “REGSET_OFS” under “Address Offset” column with the values under “n[dec]”.

The registers at address offset DDR_PHY_SLICE_REGSET_OFS consist of four sets of registers for the same functions. This corresponds to the slice index “slice”, which runs from 0 to 1 and corresponds to the byte-lane numbers within a memory channel.

		V4M		
Bit Name	Address offset	n [hex]	Bit	Initial value [hex]
PHY_CLK_WR_BYPASS_SLAVE_DELAY	DDR_PHY_SLICE_OFS	0	[9:0]	370
PHY_LP4_BOOT_RX_PCLK_CLK_SEL	DDR_PHY_SLICE_OFS	0	[18:16]	3
PHY_LP4_BOOT_PAD_DSLICE_IO_CFG	DDR_PHY_SLICE_OFS	0	[29:24]	30
SC_PHY_CDC_FIFO_POINTER_MANUAL_SYNC	DDR_PHY_SLICE_OFS	1	[0]	0
PHY_IO_PAD_DELAY_TIMING_BYPASS	DDR_PHY_SLICE_OFS	1	[10:8]	0
PHY_CLK_WRDQS_SLAVE_DELAY_BYPASS	DDR_PHY_SLICE_OFS	1	[24:16]	000
PHY_RX_CAL_ALL_DLY_BYPASS	DDR_PHY_SLICE_OFS	2	[5:0]	02
PHY_WRITE_PATH_LAT_ADD_BYPASS	DDR_PHY_SLICE_OFS	2	[10:8]	0
PHY_RDDQS_GATE_BYPASS_SLAVE_DELAY	DDR_PHY_SLICE_OFS	2	[24:16]	1FF
PHY_BYPASS_TWO_CYC_PREAMBLE	DDR_PHY_SLICE_OFS	3	[1:0]	3
PHY_CLK_BYPASS_OVERRIDE	DDR_PHY_SLICE_OFS	3	[8]	0
PHY_RDDQ_CLOCK_GATE	DDR_PHY_SLICE_OFS	3	[16]	1
PHY_SW_WRDQ0_SHIFT	DDR_PHY_SLICE_OFS	3	[29:24]	00
PHY_SW_WRDQ1_SHIFT	DDR_PHY_SLICE_OFS	4	[5:0]	00
PHY_SW_WRDQ2_SHIFT	DDR_PHY_SLICE_OFS	4	[13:8]	00
PHY_SW_WRDQ3_SHIFT	DDR_PHY_SLICE_OFS	4	[21:16]	00
PHY_SW_WRDQ4_SHIFT	DDR_PHY_SLICE_OFS	4	[29:24]	00
PHY_SW_WRDQ5_SHIFT	DDR_PHY_SLICE_OFS	5	[5:0]	00

		V4M		
Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PHY_SW_WRDQ6_SHIFT	DDR_PHY_SLICE_OFS	5	[13:8]	00
PHY_SW_WRDQ7_SHIFT	DDR_PHY_SLICE_OFS	5	[21:16]	00
PHY_SW_WRECC_SHIFT	DDR_PHY_SLICE_OFS	5	[29:24]	00
PHY_SW_WRDM_SHIFT	DDR_PHY_SLICE_OFS	6	[5:0]	00
PHY_SW_WRDQS_SHIFT	DDR_PHY_SLICE_OFS	6	[11:8]	0
PHY_PER_RANK_CS_MAP	DDR_PHY_SLICE_OFS	6	[17:16]	3
PHY_PER_CS_TRAINING_MULTICAST_EN	DDR_PHY_SLICE_OFS	6	[24]	1
PHY_PER_CS_TRAINING_INDEX	DDR_PHY_SLICE_OFS	7	[0]	0
PHY_LP4_BOOT_RDDATA_EN_IE_DLY	DDR_PHY_SLICE_OFS	7	[9:8]	0
PHY_LP4_BOOT_RDDATA_EN_DLY	DDR_PHY_SLICE_OFS	7	[20:16]	01
PHY_LP4_BOOT_RDDATA_EN_TSEL_DLY	DDR_PHY_SLICE_OFS	7	[28:24]	00
PHY_LP4_BOOT_RPTR_UPDATE	DDR_PHY_SLICE_OFS	8	[3:0]	4
PHY_LP4_BOOT_RDDQS_LATENCY_ADJUST	DDR_PHY_SLICE_OFS	8	[12:8]	00
PHY_LP4_BOOT_WRPATH_GATE_DISABLE	DDR_PHY_SLICE_OFS	8	[17:16]	3
PHY_LP4_BOOT_RDDATA_EN_OE_DLY	DDR_PHY_SLICE_OFS	8	[28:24]	01
PHY_GATE_DELAY_COMP_DISABLE	DDR_PHY_SLICE_OFS	9	[0]	0
PHY_CTRL_LPBK_EN	DDR_PHY_SLICE_OFS	9	[9:8]	0
PHY_LPBK_CONTROL	DDR_PHY_SLICE_OFS	9	[24:16]	000
PHY_LPBK_DFX_TIMEOUT_EN	DDR_PHY_SLICE_OFS	A	[0]	1
PHY_AUTO_TIMING_MARGIN_CONTROL	DDR_PHY_SLICE_OFS	B	[31:0]	00000000
PHY_AUTO_TIMING_MARGIN_OBS	DDR_PHY_SLICE_OFS	C	[27:0]	0000000
PHY_DQ_IDLE	DDR_PHY_SLICE_OFS	D	[8:0]	000
PHY_PRBS_PATTERN_START	DDR_PHY_SLICE_OFS	D	[22:16]	01
PHY_PRBS_PATTERN_MASK	DDR_PHY_SLICE_OFS	E	[8:0]	000
PHY_REGULATOR_NSLEEP_IN	DDR_PHY_SLICE_OFS	E	[16]	1
PHY_VREF_INITIAL_STEPSIZE	DDR_PHY_SLICE_OFS	E	[31:24]	08
PHY_RDLVL_BEST_THRSHLD	DDR_PHY_SLICE_OFS	F	[3:0]	2
PHY_RDLVL_PER_VREF_THRSHLD	DDR_PHY_SLICE_OFS	F	[13:8]	20
PHY_RDLVL_VREF_OUTLIER	DDR_PHY_SLICE_OFS	F	[18:16]	0
PHY_RDLVL_VREF_DELTA	DDR_PHY_SLICE_OFS	F	[27:24]	0
PHY_RDLVL_BEST_VREF_LOWER_OBS	DDR_PHY_SLICE_OFS	10	[8:0]	000
PHY_RDLVL_BEST_VREF_UPPER_OBS	DDR_PHY_SLICE_OFS	10	[27:16]	000
PHY_VREF_ALL_DQ_TRN	DDR_PHY_SLICE_OFS	11	[0]	0
PHY_VREF_TRN_DQ	DDR_PHY_SLICE_OFS	11	[15:8]	01
PHY_VREF_TAP_TRN_START	DDR_PHY_SLICE_OFS	11	[22:16]	0F
PHY_VREF_TAP_TRN_STEP	DDR_PHY_SLICE_OFS	11	[27:24]	4
PHY_VREF_TAP_TRN_END	DDR_PHY_SLICE_OFS	12	[6:0]	4F
PHY_DFE_ERR_LOOP_CNT	DDR_PHY_SLICE_OFS	12	[15:8]	03
PHY_DFE_COEFF_LOOP_CNT	DDR_PHY_SLICE_OFS	12	[23:16]	04
PHY_TAP1_COEFF_CNT	DDR_PHY_SLICE_OFS	12	[28:24]	14
PHY_TAP1_COEFF_CNVG_THRESH	DDR_PHY_SLICE_OFS	13	[2:0]	2
PHY_VREF_ERR_THRESHOLD	DDR_PHY_SLICE_OFS	13	[15:8]	01
PHY_VREF_ERR_STEP	DDR_PHY_SLICE_OFS	13	[20:16]	02
PHY_VREF_COEFF_STEP	DDR_PHY_SLICE_OFS	13	[28:24]	04

		V4M		
Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PHY_TAP_COEFF_STEP	DDR_PHY_SLICE_OFS	14	[3:0]	4
PHY_DFE_TAP1_CTRL	DDR_PHY_SLICE_OFS	14	[10:8]	4
PHY_TAP1_COEFF_THRSHLD_CODE	DDR_PHY_SLICE_OFS	14	[23:16]	04
PHY_TAP1_COEFF_THRSHLD	DDR_PHY_SLICE_OFS	14	[31:24]	10
PHY_DFE_UPDATE_POLARITY	DDR_PHY_SLICE_OFS	15	[1:0]	0
PHY_TAP1_SERIAL_STATIC	DDR_PHY_SLICE_OFS	15	[9:8]	0
PHY_TAP1_TRN_MASK	DDR_PHY_SLICE_OFS	15	[24:16]	000
PHY_WCKDCALVL_DATA_OBS	DDR_PHY_SLICE_OFS	16	[1:0]	0
PHY_WCKDCA_EN	DDR_PHY_SLICE_OFS	16	[8]	0
PHY_WCKDCA_AVG_EN	DDR_PHY_SLICE_OFS	16	[16]	0
PHY_WCKWR_TOG_EN	DDR_PHY_SLICE_OFS	16	[24]	0
PHY_VREF_TRAIN_OBS	DDR_PHY_SLICE_OFS	17	[8:0]	000
PHY_RDDQS_DQ_BYPASS_SLAVE_DELAY	DDR_PHY_SLICE_OFS	17	[24:16]	0FF
PHY_GATE_ERROR_DELAY_SELECT	DDR_PHY_SLICE_OFS	18	[3:0]	8
SC_PHY_SNAP_OBS_REGS	DDR_PHY_SLICE_OFS	18	[8]	0
PHY_GATE_SMPL1_SLAVE_DELAY	DDR_PHY_SLICE_OFS	18	[23:16]	CE
PHY_GATE_SMPL2_SLAVE_DELAY	DDR_PHY_SLICE_OFS	18	[31:24]	18
ON_FLY_GATE_ADJUST_EN	DDR_PHY_SLICE_OFS	19	[3:0]	F
PHY_GATE_TRACKING_OBS	DDR_PHY_SLICE_OFS	1A	[31:0]	00000000
PHY_LPDDR	DDR_PHY_SLICE_OFS	1B	[0]	1
PHY_WCK_ACTIVE_RANK	DDR_PHY_SLICE_OFS	1B	[9:8]	0
PHY_WCK_PAD_SEL	DDR_PHY_SLICE_OFS	1B	[16]	0
SC_PHY_WCK_CALC	DDR_PHY_SLICE_OFS	1B	[24]	0
PHY_WCK_SLV_DLY_OBS	DDR_PHY_SLICE_OFS	1C	[8:0]	000
PHY_MEM_CLASS	DDR_PHY_SLICE_OFS	1C	[18:16]	6
PHY_DFI40_POLARITY	DDR_PHY_SLICE_OFS	1C	[24]	0
PHY_SLAVE_LOOP_CNT_UPDATE	DDR_PHY_SLICE_OFS	1D	[2:0]	0
PHY_SW_FIFO_PTR_RST_DISABLE	DDR_PHY_SLICE_OFS	1D	[8]	0
PHY_MASTER_DLY_LOCK_OBS_SELECT	DDR_PHY_SLICE_OFS	1D	[19:16]	0
PHY_RDDQ_ENC_OBS_SELECT	DDR_PHY_SLICE_OFS	1D	[27:24]	0
PHY_RDDQS_DQ_ENC_OBS_SELECT	DDR_PHY_SLICE_OFS	1E	[3:0]	0
PHY_WR_ENC_OBS_SELECT	DDR_PHY_SLICE_OFS	1E	[11:8]	0
PHY_WR_SHIFT_OBS_SELECT	DDR_PHY_SLICE_OFS	1E	[19:16]	0
PHY_FIFO_PTR_OBS_SELECT	DDR_PHY_SLICE_OFS	1E	[27:24]	0
PHY_LVL_DEBUG_MODE	DDR_PHY_SLICE_OFS	1F	[0]	0
SC_PHY_LVL_DEBUG_CONT	DDR_PHY_SLICE_OFS	1F	[8]	0
PHY_WRLVL_ALGO	DDR_PHY_SLICE_OFS	1F	[17:16]	0
PHY_WRLVL_LAT_UPDATE_DISABLE	DDR_PHY_SLICE_OFS	1F	[24]	0
PHY_WRLVL_PER_START	DDR_PHY_SLICE_OFS	20	[6:0]	40
PHY_WRLVL_CAPTURE_CNT	DDR_PHY_SLICE_OFS	20	[13:8]	08
PHY_WRLVL_UPDT_WAIT_CNT	DDR_PHY_SLICE_OFS	20	[19:16]	8
PHY_DQ_MASK	DDR_PHY_SLICE_OFS	20	[31:24]	00
PHY_GTLVL_PER_START	DDR_PHY_SLICE_OFS	21	[7:0]	00
PHY_GTLVL_CAPTURE_CNT	DDR_PHY_SLICE_OFS	21	[13:8]	00

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Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PHY_GTLVL_UPDT_WAIT_CNT	DDR_PHY_SLICE_OFS	21	[19:16]	4
PHY_RDLVL_CAPTURE_CNT	DDR_PHY_SLICE_OFS	21	[29:24]	08
PHY_RDLVL_UPDT_WAIT_CNT	DDR_PHY_SLICE_OFS	22	[3:0]	4
PHY_RDLVL_RDDQS_DQ_OBS_SELECT	DDR_PHY_SLICE_OFS	22	[12:8]	00
PHY_RDLVL_PERIODIC_OBS_SELECT	DDR_PHY_SLICE_OFS	22	[23:16]	00
PHY_RDLVL_DATA_MASK	DDR_PHY_SLICE_OFS	22	[31:24]	00
PHY_WDQLVL_CLK_JITTER_TOLERANCE	DDR_PHY_SLICE_OFS	23	[7:0]	30
PHY_WDQLVL_BURST_CNT	DDR_PHY_SLICE_OFS	23	[13:8]	10
PHY_WDQLVL_DQDM_SLV_DLY_JUMP_OFFSET	DDR_PHY_SLICE_OFS	23	[25:16]	040
PHY_WDQLVL_UPDT_WAIT_CNT	DDR_PHY_SLICE_OFS	24	[3:0]	C
PHY_WDQLVL_DQDM_OBS_SELECT	DDR_PHY_SLICE_OFS	24	[11:8]	0
PHY_WDQLVL_PERIODIC_OBS_SELECT	DDR_PHY_SLICE_OFS	24	[23:16]	00
PHY_WDQLVL_BEST_THRSHLD	DDR_PHY_SLICE_OFS	24	[26:24]	2
PHY_WDQLVL_PER_VREF_THRSHLD	DDR_PHY_SLICE_OFS	25	[5:0]	20
SC_PHY_WDQLVL_CLR_PREV_RESULTS	DDR_PHY_SLICE_OFS	25	[8]	0
PHY_WDQLVL_DATADM_MASK	DDR_PHY_SLICE_OFS	25	[24:16]	000
PHY_WDQLVL_ECC_MASK	DDR_PHY_SLICE_OFS	26	[0]	1
PHY_CALVL_VREF_DRIVING_SLICE	DDR_PHY_SLICE_OFS	26	[8]	1
PHY_BYTE_MODE	DDR_PHY_SLICE_OFS	26	[16]	0
SC_PHY_MANUAL_CLEAR	DDR_PHY_SLICE_OFS	26	[29:24]	00
PHY_MASTER_DELAY_LOCK_ERROR_CNT_OBS	DDR_PHY_SLICE_OFS	27	[7:0]	00
PHY_FIFO_PTR_OBS	DDR_PHY_SLICE_OFS	27	[23:8]	0000
PHY_LPBK_RESULT_OBS	DDR_PHY_SLICE_OFS	28	[31:0]	00000000
PHY_LPBK_ERROR_COUNT_OBS	DDR_PHY_SLICE_OFS	29	[15:0]	0000
PHY_MASTER_DLY_LOCK_OBS	DDR_PHY_SLICE_OFS	29	[26:16]	000
PHY_RDDQ_SLV_DLY_ENC_OBS	DDR_PHY_SLICE_OFS	2A	[6:0]	00
PHY_RDDQS_BASE_SLV_DLY_ENC_OBS	DDR_PHY_SLICE_OFS	2A	[14:8]	00
PHY_MEAS_DLY_STEP_VALUE	DDR_PHY_SLICE_OFS	2A	[23:16]	00
PHY_RDDQS_DQ_RISE_ADDER_SLV_DLY_ENC_OBS	DDR_PHY_SLICE_OFS	2A	[31:24]	00
PHY_RDDQS_DQ_FALL_ADDER_SLV_DLY_ENC_OBS	DDR_PHY_SLICE_OFS	2B	[7:0]	00
PHY_RDDQS_GATE_SLV_DLY_ENC_OBS	DDR_PHY_SLICE_OFS	2B	[18:8]	000
PHY_DDL_DLY_INFO_OBS	DDR_PHY_SLICE_OFS	2B	[25:24]	0
PHY_WR_ADDER_SLV_DLY_ENC_OBS	DDR_PHY_SLICE_OFS	2C	[9:0]	000
PHY_WR_SHIFT_OBS	DDR_PHY_SLICE_OFS	2C	[18:16]	0
PHY_WRLVL_HARD0_DELAY_OBS	DDR_PHY_SLICE_OFS	2D	[9:0]	000
PHY_WRLVL_HARD1_DELAY_OBS	DDR_PHY_SLICE_OFS	2D	[25:16]	000
PHY_WRLVL_STATUS_OBS	DDR_PHY_SLICE_OFS	2E	[27:0]	0000000
PHY_GATE_SMPL1_SLV_DLY_ENC_OBS	DDR_PHY_SLICE_OFS	2F	[9:0]	000
PHY_GATE_SMPL2_SLV_DLY_ENC_OBS	DDR_PHY_SLICE_OFS	2F	[25:16]	000
PHY_WRLVL_ERROR_OBS	DDR_PHY_SLICE_OFS	30	[1:0]	0
PHY_GTLVL_HARD0_DELAY_OBS	DDR_PHY_SLICE_OFS	30	[20:8]	0000
PHY_GTLVL_HARD1_DELAY_OBS	DDR_PHY_SLICE_OFS	31	[12:0]	0000
PHY_GTLVL_STATUS_OBS	DDR_PHY_SLICE_OFS	32	[17:0]	00000
PHY_RDLVL_CLK_JITTER_TOLERANCE	DDR_PHY_SLICE_OFS	33	[8:0]	030

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Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PHY_RDLVL_RDDQS_DQ_LE_DLY_OBS	DDR_PHY_SLICE_OFS	33	[24:16]	000
PHY_RDLVL_RDDQS_DQ_TE_DLY_OBS	DDR_PHY_SLICE_OFS	34	[8:0]	000
PHY_RDLVL_STATUS_OBS	DDR_PHY_SLICE_OFS	35	[31:0]	00000000
PHY_RDLVL_PERIODIC_OBS	DDR_PHY_SLICE_OFS	36	[31:0]	00000000
PHY_WDQLVL_DQDM_LE_DLY_OBS	DDR_PHY_SLICE_OFS	37	[10:0]	000
PHY_WDQLVL_DQDM_TE_DLY_OBS	DDR_PHY_SLICE_OFS	37	[26:16]	000
PHY_WDQLVL_STATUS_OBS	DDR_PHY_SLICE_OFS	38	[31:0]	00000000
PHY_WDQLVL_PERIODIC_OBS	DDR_PHY_SLICE_OFS	39	[31:0]	00000000
PHY_DDL_MODE_LOW	DDR_PHY_SLICE_OFS	3A	[31:0]	00000000
PHY_DDL_MODE_UPPER	DDR_PHY_SLICE_OFS	3B	[9:0]	000
PHY_DDL_ENABLE	DDR_PHY_SLICE_OFS	3B	[16]	0
PHY_DDL_TEST_OBS	DDR_PHY_SLICE_OFS	3C	[31:0]	00000000
PHY_DDL_TRACK_UPD_THRESHOLD	DDR_PHY_SLICE_OFS	3D	[7:0]	04
PHY_LP4_WDQS_OE_EXTEND	DDR_PHY_SLICE_OFS	3D	[8]	1
PHY_RX_CAL_DQS	DDR_PHY_SLICE_OFS	3D	[22:16]	00
PHY_RX_CAL_FDBK	DDR_PHY_SLICE_OFS	3D	[30:24]	00
PHY_PAD_RX_BIAS_EN	DDR_PHY_SLICE_OFS	3E	[10:0]	7FF
PHY_STATIC_TOG_DISABLE	DDR_PHY_SLICE_OFS	3E	[20:16]	1F
PHY_DFE_INIT_FALL_DATA	DDR_PHY_SLICE_OFS	3E	[24]	0
PHY_DFE_EN	DDR_PHY_SLICE_OFS	3F	[2:0]	0
PHY_DATA_DC_CAL_SAMPLE_WAIT	DDR_PHY_SLICE_OFS	3F	[15:8]	08
PHY_DATA_DC_CAL_TIMEOUT	DDR_PHY_SLICE_OFS	3F	[23:16]	80
PHY_DATA_DC_WEIGHT	DDR_PHY_SLICE_OFS	3F	[25:24]	0
PHY_DATA_DC_ADJUST_START	DDR_PHY_SLICE_OFS	40	[5:0]	20
PHY_DATA_DC_ADJUST_SAMPLE_CNT	DDR_PHY_SLICE_OFS	40	[15:8]	10
PHY_DATA_DC_ADJUST_THRSHLD	DDR_PHY_SLICE_OFS	40	[23:16]	06
PHY_DATA_DC_ADJUST_DIRECT	DDR_PHY_SLICE_OFS	40	[24]	0
PHY_DATA_DC_CAL_POLARITY	DDR_PHY_SLICE_OFS	41	[0]	0
PHY_DATA_DC_CAL_START	DDR_PHY_SLICE_OFS	41	[8]	0
PHY_DATA_DC_SW_RANK	DDR_PHY_SLICE_OFS	41	[17:16]	1
PHY_FDBK_PWR_CTRL	DDR_PHY_SLICE_OFS	41	[26:24]	4
PHY_SLV_DLY_CTRL_GATE_DISABLE	DDR_PHY_SLICE_OFS	42	[0]	0
PHY_RDPATH_GATE_DISABLE	DDR_PHY_SLICE_OFS	42	[8]	0
PHY_DCC_RXCAL_CTRL_GATE_DISABLE	DDR_PHY_SLICE_OFS	42	[16]	0
PHY_SLICE_PWR_RDC_DISABLE	DDR_PHY_SLICE_OFS	42	[25:24]	0
PHY_DQ_TSEL_ENABLE	DDR_PHY_SLICE_OFS	43	[2:0]	1
PHY_WCKDCA_UPD_EN	DDR_PHY_SLICE_OFS	43	[8]	0
PHY_REGULATOR_CONTROL	DDR_PHY_SLICE_OFS	43	[31:16]	CE02
PHY_REGULATOR_EN_CNT	DDR_PHY_SLICE_OFS	44	[5:0]	07
PHY_RX_DFE_EN	DDR_PHY_SLICE_OFS	44	[9:8]	0
PHY_LP4_BOOT_PHY_RX_DFE_EN	DDR_PHY_SLICE_OFS	44	[17:16]	0
PHY_DQ_TSEL_SELECT	DDR_PHY_SLICE_OFS	45	[15:0]	7706
PHY_DQS_TSEL_ENABLE	DDR_PHY_SLICE_OFS	45	[18:16]	1
PHY_DQS_TSEL_SELECT	DDR_PHY_SLICE_OFS	46	[15:0]	7706

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Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PHY_TWO_CYC_PREAMBLE	DDR_PHY_SLICE_OFS	46	[17:16]	3
PHY_WCK_FREQ_RATIO	DDR_PHY_SLICE_OFS	46	[24]	0
PHY_LP4_BOOT_WCK_FREQ_RATIO	DDR_PHY_SLICE_OFS	47	[0]	0
PHY_WCK_SETTING_SOURCE	DDR_PHY_SLICE_OFS	47	[9:8]	0
PHY_WR_LINK_ECC_EN	DDR_PHY_SLICE_OFS	47	[16]	0
PHY_PST_AMBLE	DDR_PHY_SLICE_OFS	47	[27:24]	0
PHY_VREF_INITIAL_START_POINT	DDR_PHY_SLICE_OFS	48	[8:0]	06C
PHY_VREF_INITIAL_STOP_POINT	DDR_PHY_SLICE_OFS	48	[24:16]	08C
PHY_VREF_TRAINING_CTRL	DDR_PHY_SLICE_OFS	49	[1:0]	1
PHY_RDLVL_FINAL_VREF_OFFSET	DDR_PHY_SLICE_OFS	49	[11:8]	0
PHY_NTP_WDQ_STEP_SIZE	DDR_PHY_SLICE_OFS	49	[23:16]	10
PHY_NTP_WDQ_START	DDR_PHY_SLICE_OFS	4A	[9:0]	100
PHY_NTP_WDQ_STOP	DDR_PHY_SLICE_OFS	4A	[25:16]	3FF
PHY_NTP_WDQ_BIT_EN	DDR_PHY_SLICE_OFS	4B	[7:0]	01
PHY_WDQLVL_DVW_MIN	DDR_PHY_SLICE_OFS	4B	[16:8]	06E
PHY_SW_WDQLVL_DVW_MIN_EN	DDR_PHY_SLICE_OFS	4B	[24]	0
PHY_WDQLVL_PER_START_OFFSET	DDR_PHY_SLICE_OFS	4C	[4:0]	01
PHY_FAST_LVL_EN	DDR_PHY_SLICE_OFS	4C	[11:8]	3
PHY_PAD_TX_DCD	DDR_PHY_SLICE_OFS	4C	[20:16]	00
PHY_PAD_RX_DCD_0	DDR_PHY_SLICE_OFS	4C	[28:24]	00
PHY_PAD_RX_DCD_1	DDR_PHY_SLICE_OFS	4D	[4:0]	00
PHY_PAD_RX_DCD_2	DDR_PHY_SLICE_OFS	4D	[12:8]	00
PHY_PAD_RX_DCD_3	DDR_PHY_SLICE_OFS	4D	[20:16]	00
PHY_PAD_RX_DCD_4	DDR_PHY_SLICE_OFS	4D	[28:24]	00
PHY_PAD_RX_DCD_5	DDR_PHY_SLICE_OFS	4E	[4:0]	00
PHY_PAD_RX_DCD_6	DDR_PHY_SLICE_OFS	4E	[12:8]	00
PHY_PAD_RX_DCD_7	DDR_PHY_SLICE_OFS	4E	[20:16]	00
PHY_PAD_DM_RX_DCD	DDR_PHY_SLICE_OFS	4E	[28:24]	00
PHY_PAD_DQS_RX_DCD	DDR_PHY_SLICE_OFS	4F	[4:0]	00
PHY_PAD_FDBK_RX_DCD	DDR_PHY_SLICE_OFS	4F	[12:8]	00
PHY_PAD_DSLICE_IO_CFG	DDR_PHY_SLICE_OFS	4F	[21:16]	00
PHY_RDDQ0_SLAVE_DELAY	DDR_PHY_SLICE_OFS	50	[8:0]	038
PHY_RDDQ1_SLAVE_DELAY	DDR_PHY_SLICE_OFS	50	[24:16]	038
PHY_RDDQ2_SLAVE_DELAY	DDR_PHY_SLICE_OFS	51	[8:0]	038
PHY_RDDQ3_SLAVE_DELAY	DDR_PHY_SLICE_OFS	51	[24:16]	038
PHY_RDDQ4_SLAVE_DELAY	DDR_PHY_SLICE_OFS	52	[8:0]	038
PHY_RDDQ5_SLAVE_DELAY	DDR_PHY_SLICE_OFS	52	[24:16]	038
PHY_RDDQ6_SLAVE_DELAY	DDR_PHY_SLICE_OFS	53	[8:0]	038
PHY_RDDQ7_SLAVE_DELAY	DDR_PHY_SLICE_OFS	53	[24:16]	038
PHY_RDDM_SLAVE_DELAY	DDR_PHY_SLICE_OFS	54	[8:0]	038
PHY_GT_RDDQLVL_EN	DDR_PHY_SLICE_OFS	54	[16]	0
PHY_RX_CAL_ALL_DLY	DDR_PHY_SLICE_OFS	54	[29:24]	09
PHY_RX_PCLK_CLK_SEL	DDR_PHY_SLICE_OFS	55	[2:0]	3
PHY_DATA_DC_CAL_CLK_SEL	DDR_PHY_SLICE_OFS	55	[10:8]	5

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Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PHY_DQ_OE_TIMING	DDR_PHY_SLICE_OFS	55	[23:16]	51
PHY_DQ_TSEL_RD_TIMING	DDR_PHY_SLICE_OFS	55	[31:24]	90
PHY_DQ_TSEL_WR_TIMING	DDR_PHY_SLICE_OFS	56	[7:0]	61
PHY_DQS_OE_TIMING	DDR_PHY_SLICE_OFS	56	[15:8]	61
PHY_IO_PAD_DELAY_TIMING	DDR_PHY_SLICE_OFS	56	[18:16]	0
PHY_DQS_TSEL_RD_TIMING	DDR_PHY_SLICE_OFS	56	[31:24]	70
PHY_DQS_IO_UPDATE_TIMING	DDR_PHY_SLICE_OFS	57	[6:0]	31
PHY_DQ_IO_UPDATE_TIMING	DDR_PHY_SLICE_OFS	57	[11:8]	5
PHY_DQS_OE_RD_TIMING	DDR_PHY_SLICE_OFS	57	[23:16]	C0
PHY_DQS_TSEL_WR_TIMING	DDR_PHY_SLICE_OFS	57	[31:24]	41
PHY_VREF_SETTING_TIME	DDR_PHY_SLICE_OFS	58	[15:0]	0064
PHY_PAD_VREF_CTRL_DQ	DDR_PHY_SLICE_OFS	58	[29:16]	2680
PHY_PAD_VREF_H_CTRL_DQ	DDR_PHY_SLICE_OFS	59	[13:0]	0080
PHY_PER_CS_TRAINING_EN	DDR_PHY_SLICE_OFS	59	[16]	1
PHY_DQ_IE_TIMING	DDR_PHY_SLICE_OFS	59	[31:24]	C0
PHY_DQS_IE_TIMING	DDR_PHY_SLICE_OFS	5A	[7:0]	C0
PHY_RDDATA_EN_IE_DLY	DDR_PHY_SLICE_OFS	5A	[9:8]	0
PHY_IE_MODE	DDR_PHY_SLICE_OFS	5A	[17:16]	1
PHY_DBI_MODE	DDR_PHY_SLICE_OFS	5A	[24]	1
PHY_LP_DBI_TRAIN	DDR_PHY_SLICE_OFS	5B	[0]	1
PHY_RDDATA_EN_TSEL_DLY	DDR_PHY_SLICE_OFS	5B	[12:8]	0C
PHY_RDDATA_EN_OE_DLY	DDR_PHY_SLICE_OFS	5B	[20:16]	0E
PHY_SW_MASTER_MODE	DDR_PHY_SLICE_OFS	5B	[27:24]	0
PHY_MASTER_DELAY_LOCK_MODE	DDR_PHY_SLICE_OFS	5C	[2:0]	0
PHY_MASTER_DELAY_LESS_STEP	DDR_PHY_SLICE_OFS	5C	[10:8]	2
PHY_MASTER_DELAY_THRESHOLD_FACTOR	DDR_PHY_SLICE_OFS	5C	[18:16]	3
PHY_MASTER_DELAY_START	DDR_PHY_SLICE_OFS	5D	[10:0]	010
PHY_MASTER_DELAY_STEP	DDR_PHY_SLICE_OFS	5D	[21:16]	10
PHY_MASTER_DELAY_WAIT	DDR_PHY_SLICE_OFS	5D	[31:24]	42
PHY_MASTER_DELAY_HALF_MEASURE	DDR_PHY_SLICE_OFS	5E	[7:0]	3E
PHY_RPTR_UPDATE	DDR_PHY_SLICE_OFS	5E	[11:8]	8
PHY_WRLVL_DLY_STEP	DDR_PHY_SLICE_OFS	5E	[23:16]	06
PHY_WRLVL_DLY_FINE_STEP	DDR_PHY_SLICE_OFS	5E	[27:24]	1
PHY_WRLVL_RESP_WAIT_CNT	DDR_PHY_SLICE_OFS	5F	[5:0]	27
PHY_GTLVL_DLY_STEP	DDR_PHY_SLICE_OFS	5F	[11:8]	6
PHY_GTLVL_RESP_WAIT_CNT	DDR_PHY_SLICE_OFS	5F	[20:16]	0F
PHY_GTLVL_BACK_STEP	DDR_PHY_SLICE_OFS	60	[9:0]	0C8
PHY_GTLVL_FINAL_STEP	DDR_PHY_SLICE_OFS	60	[25:16]	0E6
PHY_GTLVL_0_WIDTH_THRSHLD	DDR_PHY_SLICE_OFS	61	[6:0]	40
PHY_GTLVL_0_WIDTH_CHK_EN	DDR_PHY_SLICE_OFS	61	[8]	1
PHY_WDQLVL_DLY_STEP	DDR_PHY_SLICE_OFS	61	[23:16]	10
PHY_WDQLVL_QTR_DLY_STEP	DDR_PHY_SLICE_OFS	61	[27:24]	1
PHY_TOGGLE_PRE_SUPPORT	DDR_PHY_SLICE_OFS	62	[0]	0
PHY_RDLVL_DLY_STEP	DDR_PHY_SLICE_OFS	62	[11:8]	0

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Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PHY_RDLVL_MAX_EDGE	DDR_PHY_SLICE_OFS	63	[8:0]	19B
PHY_RDLVL_HALF_MODE_MAX_EDGE	DDR_PHY_SLICE_OFS	64	[8:0]	000
PHY_RDLVL_DVW_MIN	DDR_PHY_SLICE_OFS	65	[8:0]	068
PHY_SW_RDLVL_DVW_MIN_EN	DDR_PHY_SLICE_OFS	65	[16]	0
PHY_RDLVL_PER_START_OFFSET	DDR_PHY_SLICE_OFS	65	[28:24]	05
PHY_WRPATH_GATE_DISABLE	DDR_PHY_SLICE_OFS	66	[1:0]	0
PHY_WRPATH_GATE_TIMING	DDR_PHY_SLICE_OFS	66	[10:8]	4
PHY_DATA_DC_INIT_DISABLE	DDR_PHY_SLICE_OFS	66	[17:16]	0
PHY_DATA_DC_DQS_INIT_SLV_DELAY	DDR_PHY_SLICE_OFS	67	[8:0]	000
PHY_DATA_DC_DQ_INIT_SLV_DELAY	DDR_PHY_SLICE_OFS	67	[25:16]	140
PHY_DATA_DC_WRLVL_ENABLE	DDR_PHY_SLICE_OFS	68	[0]	1
PHY_DATA_DC_WDQLVL_ENABLE	DDR_PHY_SLICE_OFS	68	[9:8]	3
PHY_DATA_DC_DM_CLK_SE_THRSHLD	DDR_PHY_SLICE_OFS	68	[23:16]	80
PHY_DATA_DC_DM_CLK_DIFF_THRSHLD	DDR_PHY_SLICE_OFS	68	[31:24]	80
PHY_WDQ_OSC_DELTA	DDR_PHY_SLICE_OFS	69	[6:0]	10
PHY_MEAS_DLY_STEP_ENABLE	DDR_PHY_SLICE_OFS	69	[13:8]	22
PHY_RDDATA_EN_DLY	DDR_PHY_SLICE_OFS	69	[20:16]	0E
PHY_DQ_DM_SWIZZLE0	DDR_PHY_SLICE_OFS	6A	[31:0]	76543210
PHY_DQ_DM_SWIZZLE1	DDR_PHY_SLICE_OFS	6B	[3:0]	8
PHY_CLK_WRDQ0_SLAVE_DELAY	DDR_PHY_SLICE_OFS	6C	[10:0]	250
PHY_CLK_WRDQ1_SLAVE_DELAY	DDR_PHY_SLICE_OFS	6C	[26:16]	250
PHY_CLK_WRDQ2_SLAVE_DELAY	DDR_PHY_SLICE_OFS	6D	[10:0]	250
PHY_CLK_WRDQ3_SLAVE_DELAY	DDR_PHY_SLICE_OFS	6D	[26:16]	250
PHY_CLK_WRDQ4_SLAVE_DELAY	DDR_PHY_SLICE_OFS	6E	[10:0]	250
PHY_CLK_WRDQ5_SLAVE_DELAY	DDR_PHY_SLICE_OFS	6E	[26:16]	250
PHY_CLK_WRDQ6_SLAVE_DELAY	DDR_PHY_SLICE_OFS	6F	[10:0]	250
PHY_CLK_WRDQ7_SLAVE_DELAY	DDR_PHY_SLICE_OFS	6F	[26:16]	250
PHY_CLK_WRECC_SLAVE_DELAY	DDR_PHY_SLICE_OFS	70	[10:0]	250
PHY_CLK_WRDM_SLAVE_DELAY	DDR_PHY_SLICE_OFS	70	[26:16]	250
PHY_CLK_WRDQS_SLAVE_DELAY	DDR_PHY_SLICE_OFS	71	[8:0]	000
PHY_WRITE_PATH_LAT_DEC	DDR_PHY_SLICE_OFS	71	[16]	0
PHY_WRITE_PATH_LAT_ADJ	DDR_PHY_SLICE_OFS	71	[25:24]	0
PHY_RDDQS_DQ0_RISE_SLAVE_DELAY	DDR_PHY_SLICE_OFS	72	[8:0]	050
PHY_RDDQS_DQ0_FALL_SLAVE_DELAY	DDR_PHY_SLICE_OFS	72	[24:16]	050
PHY_RDDQS_DQ1_RISE_SLAVE_DELAY	DDR_PHY_SLICE_OFS	73	[8:0]	050
PHY_RDDQS_DQ1_FALL_SLAVE_DELAY	DDR_PHY_SLICE_OFS	73	[24:16]	050
PHY_RDDQS_DQ2_RISE_SLAVE_DELAY	DDR_PHY_SLICE_OFS	74	[8:0]	050
PHY_RDDQS_DQ2_FALL_SLAVE_DELAY	DDR_PHY_SLICE_OFS	74	[24:16]	050
PHY_RDDQS_DQ3_RISE_SLAVE_DELAY	DDR_PHY_SLICE_OFS	75	[8:0]	050
PHY_RDDQS_DQ3_FALL_SLAVE_DELAY	DDR_PHY_SLICE_OFS	75	[24:16]	050
PHY_RDDQS_DQ4_RISE_SLAVE_DELAY	DDR_PHY_SLICE_OFS	76	[8:0]	050
PHY_RDDQS_DQ4_FALL_SLAVE_DELAY	DDR_PHY_SLICE_OFS	76	[24:16]	050
PHY_RDDQS_DQ5_RISE_SLAVE_DELAY	DDR_PHY_SLICE_OFS	77	[8:0]	050
PHY_RDDQS_DQ5_FALL_SLAVE_DELAY	DDR_PHY_SLICE_OFS	77	[24:16]	050

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Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PHY_RDDQS_DQ6_RISE_SLAVE_DELAY	DDR_PHY_SLICE_OFS	78	[8:0]	050
PHY_RDDQS_DQ6_FALL_SLAVE_DELAY	DDR_PHY_SLICE_OFS	78	[24:16]	050
PHY_RDDQS_DQ7_RISE_SLAVE_DELAY	DDR_PHY_SLICE_OFS	79	[8:0]	050
PHY_RDDQS_DQ7_FALL_SLAVE_DELAY	DDR_PHY_SLICE_OFS	79	[24:16]	050
PHY_RDDQS_DM_RISE_SLAVE_DELAY	DDR_PHY_SLICE_OFS	7A	[8:0]	050
PHY_RDDQS_DM_FALL_SLAVE_DELAY	DDR_PHY_SLICE_OFS	7A	[24:16]	050
PHY_RDDQS_GATE_SLAVE_DELAY	DDR_PHY_SLICE_OFS	7B	[8:0]	0E1
PHY_RDDQS_LATENCY_ADJUST	DDR_PHY_SLICE_OFS	7B	[20:16]	05
PHY_WRITE_PATH_LAT_ADD	DDR_PHY_SLICE_OFS	7B	[26:24]	0
PHY_WRITE_PATH_LAT_FRAC	DDR_PHY_SLICE_OFS	7C	[7:0]	00
PHY_GTLVL_RDDQS_SLV_DLY_START	DDR_PHY_SLICE_OFS	7C	[16:8]	000
PHY_WRLVL_EARLY_FORCE_ZERO	DDR_PHY_SLICE_OFS	7C	[24]	0
PHY_GTLVL_LAT_ADJ_START	DDR_PHY_SLICE_OFS	7D	[4:0]	0A
PHY_WDQLVL_DQDM_SLV_DLY_START	DDR_PHY_SLICE_OFS	7D	[17:8]	100
PHY_NTP_WRLAT_START	DDR_PHY_SLICE_OFS	7D	[27:24]	8
PHY_NTP_PASS	DDR_PHY_SLICE_OFS	7E	[0]	0
PHY_RDLVL_RDDQS_DQ_SLV_DLY_START	DDR_PHY_SLICE_OFS	7E	[16:8]	000
PHY_DATA_DC_DQS_CLK_ADJUST	DDR_PHY_SLICE_OFS	7F	[7:0]	20
PHY_DATA_DC_DQ0_CLK_ADJUST	DDR_PHY_SLICE_OFS	7F	[15:8]	20
PHY_DATA_DC_DQ1_CLK_ADJUST	DDR_PHY_SLICE_OFS	7F	[23:16]	20
PHY_DATA_DC_DQ2_CLK_ADJUST	DDR_PHY_SLICE_OFS	7F	[31:24]	20
PHY_DATA_DC_DQ3_CLK_ADJUST	DDR_PHY_SLICE_OFS	80	[7:0]	20
PHY_DATA_DC_DQ4_CLK_ADJUST	DDR_PHY_SLICE_OFS	80	[15:8]	20
PHY_DATA_DC_DQ5_CLK_ADJUST	DDR_PHY_SLICE_OFS	80	[23:16]	20
PHY_DATA_DC_DQ6_CLK_ADJUST	DDR_PHY_SLICE_OFS	80	[31:24]	20
PHY_DATA_DC_DQ7_CLK_ADJUST	DDR_PHY_SLICE_OFS	81	[7:0]	20
PHY_DATA_DC_DM_CLK_ADJUST	DDR_PHY_SLICE_OFS	81	[15:8]	20
PHY_DATA_DC_ECC_CLK_ADJUST	DDR_PHY_SLICE_OFS	81	[23:16]	20
PHY_DATA_DC_RDQS_CLK_ADJUST	DDR_PHY_SLICE_OFS	81	[31:24]	20
PHY_DSLICE_PAD_BOOSTPN_SETTING	DDR_PHY_SLICE_OFS	82	[15:0]	0000
PHY_DSLICE_PAD_RX_CTLE_SETTING	DDR_PHY_SLICE_OFS	82	[21:16]	00
PHY_DQ_FFE_TAP	DDR_PHY_SLICE_OFS	82	[27:24]	0
PHY_DQS_FFE_TAP	DDR_PHY_SLICE_OFS	83	[3:0]	0
PHY_RX_CAL_DQ0	DDR_PHY_SLICE_OFS	83	[25:8]	00000
PHY_RX_CAL_DQ1	DDR_PHY_SLICE_OFS	84	[17:0]	00000
PHY_RX_CAL_DQ2	DDR_PHY_SLICE_OFS	85	[17:0]	00000
PHY_RX_CAL_DQ3	DDR_PHY_SLICE_OFS	86	[17:0]	00000
PHY_RX_CAL_DQ4	DDR_PHY_SLICE_OFS	87	[17:0]	00000
PHY_RX_CAL_DQ5	DDR_PHY_SLICE_OFS	88	[17:0]	00000
PHY_RX_CAL_DQ6	DDR_PHY_SLICE_OFS	89	[17:0]	00000
PHY_RX_CAL_DQ7	DDR_PHY_SLICE_OFS	8A	[17:0]	00000
PHY_RX_CAL_DM	DDR_PHY_SLICE_OFS	8B	[17:0]	00000
PHY_ADR_CALVL_START	DDR_PHY_ADR_V_OFS	0	[9:0]	000
PHY_ADR_CALVL_COARSE_DLY	DDR_PHY_ADR_V_OFS	0	[25:16]	040

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Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PHY_CALVL_BEST_THRSHLD	DDR_PHY_ADR_V_OFS	1	[2:0]	2
PHY_CALVL_PER_VREF_THRSHLD	DDR_PHY_ADR_V_OFS	1	[13:8]	20
PHY_ADR_CALVL_QTR	DDR_PHY_ADR_V_OFS	1	[25:16]	020
PHY_ADR_CALVL_SWIZZLE0	DDR_PHY_ADR_V_OFS	2	[31:0]	76543210
PHY_ADR_CSLVL_TRAIN_MASK	DDR_PHY_ADR_V_OFS	3	[6:0]	01
PHY_ADR_MEAS_DLY_STEP_VALUE	DDR_PHY_ADR_V_OFS	3	[15:8]	00
PHY_ADR_MEAS_DLY_STEP_ENABLE	DDR_PHY_ADR_V_OFS	3	[16]	1
PHY_ADR_ADDR_SEL	DDR_PHY_ADR_V_OFS	4	[27:0]	6543210
PHY_ADR_BYTE_MODE	DDR_PHY_ADR_V_OFS	5	[0]	0
PHY_ADR_CA_TRAIN_MODE_1	DDR_PHY_ADR_V_OFS	5	[8]	1
PHY_ADR_MEM_CLASS	DDR_PHY_ADR_V_OFS	5	[18:16]	6
PHY_ADR_CALVL_RANK_CTRL	DDR_PHY_ADR_V_OFS	5	[25:24]	3
PHY_ADR_CALVL_RESP_WAIT_CNT	DDR_PHY_ADR_V_OFS	6	[3:0]	0
PHY_ADR_CALVL_PERIODIC_START_OFFSET	DDR_PHY_ADR_V_OFS	6	[16:8]	010
PHY_ADR_CALVL_DEBUG_MODE	DDR_PHY_ADR_V_OFS	6	[24]	0
SC_PHY_ADR_CALVL_DEBUG_CONT	DDR_PHY_ADR_V_OFS	7	[0]	0
SC_PHY_ADR_CALVL_ERROR_CLR	DDR_PHY_ADR_V_OFS	7	[8]	0
PHY_ADR_CALVL_OBS_SELECT	DDR_PHY_ADR_V_OFS	7	[20:16]	00
PHY_ADR_CALVL_CH0_OBS0	DDR_PHY_ADR_V_OFS	8	[31:0]	00000000
PHY_ADR_CALVL_CH1_OBS0	DDR_PHY_ADR_V_OFS	9	[31:0]	00000000
PHY_ADR_CALVL_OBS1	DDR_PHY_ADR_V_OFS	A	[31:0]	00000000
PHY_ADR_CALVL_OBS2	DDR_PHY_ADR_V_OFS	B	[31:0]	00000000
PHY_SW_ACBIT0_SHIFT_0	DDR_PHY_ADR_V_OFS	C	[3:0]	0
PHY_SW_ACBIT1_SHIFT_0	DDR_PHY_ADR_V_OFS	C	[11:8]	0
PHY_SW_ACBIT2_SHIFT_0	DDR_PHY_ADR_V_OFS	C	[19:16]	0
PHY_SW_ACBIT3_SHIFT_0	DDR_PHY_ADR_V_OFS	C	[27:24]	0
PHY_SW_ACBIT0_SHIFT_1	DDR_PHY_ADR_V_OFS	D	[3:0]	0
PHY_SW_ACBIT1_SHIFT_1	DDR_PHY_ADR_V_OFS	D	[11:8]	0
PHY_SW_ACBIT2_SHIFT_1	DDR_PHY_ADR_V_OFS	D	[19:16]	0
PHY_SW_ACBIT3_SHIFT_1	DDR_PHY_ADR_V_OFS	D	[27:24]	0
PHY_SW_ACBIT0_SHIFT_2	DDR_PHY_ADR_V_OFS	E	[3:0]	0
PHY_SW_ACBIT1_SHIFT_2	DDR_PHY_ADR_V_OFS	E	[11:8]	0
PHY_SW_ACBIT2_SHIFT_2	DDR_PHY_ADR_V_OFS	E	[19:16]	0
PHY_SW_ACBIT3_SHIFT_2	DDR_PHY_ADR_V_OFS	E	[27:24]	0
PHY_ADR_CALVL_TRAIN_MASK	DDR_PHY_ADR_V_OFS	F	[6:0]	3F
PHY_ADR_SW_CALVL_DVW_MIN	DDR_PHY_ADR_V_OFS	F	[16:8]	080
PHY_ADR_SW_CALVL_DVW_MIN_EN	DDR_PHY_ADR_V_OFS	F	[24]	0
PHY_ADR_CALVL_DLY_STEP	DDR_PHY_ADR_V_OFS	10	[3:0]	1
PHY_ADR_CALVL_CAPTURE_CNT	DDR_PHY_ADR_V_OFS	11	[3:0]	3
PHY_PAD_ADR_IO_CFG	DDR_PHY_ADR_V_OFS	11	[15:8]	00
PHY_ADRCTL_MANUAL_CLEAR	DDR_PHY_ADR_V_OFS	11	[17:16]	0
PHY_ADRCTL_MASTER_DELAY_LOCK_ERROR_CNT_OBS	DDR_PHY_ADR_V_OFS	11	[31:24]	00
PHY_ADRCTL_MASTER_DLY_LOCK_OBS_SELECT	DDR_PHY_ADR_V_OFS	12	[3:0]	0
PHY_ADRCTL_MASTER_DLY_LOCK_OBS	DDR_PHY_ADR_V_OFS	12	[18:8]	000

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Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PHY_ADRCTL_SLAVE_LOOP_CNT_UPDATE	DDR_PHY_ADR_V_OFS	12	[26:24]	0
PHY_ADRCTL_SNAP_OBS_REGS	DDR_PHY_ADR_V_OFS	13	[0]	0
PHY_ADRCTL_LPDDR	DDR_PHY_ADR_V_OFS	13	[8]	0
PHY_ADRCTL_SW_TXPWR_CTRL_0	DDR_PHY_ADR_V_OFS	13	[19:16]	F
PHY_SW_TXIO_CTRL_0	DDR_PHY_ADR_V_OFS	13	[27:24]	0
PHY_ADRCTL_SW_TXPWR_CTRL_1	DDR_PHY_ADR_V_OFS	14	[3:0]	F
PHY_SW_TXIO_CTRL_1	DDR_PHY_ADR_V_OFS	14	[11:8]	0
PHY_ADRCTL_SW_TXPWR_CTRL_2	DDR_PHY_ADR_V_OFS	14	[19:16]	3
PHY_CS_ACS_ALLOCATION_BIT0_2	DDR_PHY_ADR_V_OFS	14	[25:24]	1
PHY_CS_ACS_ALLOCATION_BIT1_2	DDR_PHY_ADR_V_OFS	15	[1:0]	2
PHY_CS_ACS_ALLOCATION_BIT2_2	DDR_PHY_ADR_V_OFS	15	[9:8]	3
PHY_CS_ACS_ALLOCATION_BIT3_2	DDR_PHY_ADR_V_OFS	15	[17:16]	3
PHY_SW_TXIO_CTRL_2	DDR_PHY_ADR_V_OFS	15	[27:24]	0
PHY_ADRCTL_STATIC_TOG_DISABLE	DDR_PHY_ADR_V_OFS	16	[3:0]	F
PHY_ADRCTL_MANUAL_UPDATE	DDR_PHY_ADR_V_OFS	16	[8]	0
PHY_AC_LPBK_ERR_CLEAR	DDR_PHY_ADR_V_OFS	16	[16]	0
PHY_AC_LPBK_OBS_SELECT	DDR_PHY_ADR_V_OFS	16	[25:24]	0
PHY_AC_LPBK_ENABLE	DDR_PHY_ADR_V_OFS	17	[2:0]	0
PHY_AC_PRBS_PATTERN_START	DDR_PHY_ADR_V_OFS	17	[14:8]	01
PHY_AC_PRBS_PATTERN_MASK	DDR_PHY_ADR_V_OFS	17	[19:16]	0
PHY_AC_LPBK_RESULT_OBS	DDR_PHY_ADR_V_OFS	18	[31:0]	00000000
PHY_AC_CLK_LPBK_OBS_SELECT	DDR_PHY_ADR_V_OFS	19	[0]	0
PHY_AC_CLK_LPBK_ENABLE	DDR_PHY_ADR_V_OFS	19	[8]	0
PHY_AC_CLK_LPBK_CONTROL	DDR_PHY_ADR_V_OFS	19	[21:16]	00
PHY_AC_CLK_LPBK_RESULT_OBS	DDR_PHY_ADR_V_OFS	1A	[15:0]	0000
PHY_AC_PWR_RDC_DISABLE	DDR_PHY_ADR_V_OFS	1A	[18:16]	0
PHY_AC_SLV_DLY_CTRL_GATE_DISABLE	DDR_PHY_ADR_V_OFS	1A	[24]	0
PHY_DDL_AC_ENABLE	DDR_PHY_ADR_V_OFS	1B	[2:0]	0
PHY_DDL_AC_MODE_LOW	DDR_PHY_ADR_V_OFS	1C	[31:0]	00000000
PHY_DDL_AC_MODE_UPPER	DDR_PHY_ADR_V_OFS	1D	[9:0]	000
PHY_DDL_AC_TRACK_UPD_THRESHOLD	DDR_PHY_ADR_V_OFS	1D	[23:16]	04
PHY_CSLVL_START	DDR_PHY_ADR_V_OFS	1E	[9:0]	200
PHY_CSLVL_COARSE_DLY	DDR_PHY_ADR_V_OFS	1E	[25:16]	02A
PHY_CSLVL_DEBUG_MODE	DDR_PHY_ADR_V_OFS	1F	[0]	0
SC_PHY_CSLVL_DEBUG_CONT	DDR_PHY_ADR_V_OFS	1F	[8]	0
SC_PHY_CSLVL_ERROR_CLR	DDR_PHY_ADR_V_OFS	1F	[16]	0
PHY_CSLVL_OBS0	DDR_PHY_ADR_V_OFS	20	[31:0]	00000000
PHY_CSLVL_OBS1	DDR_PHY_ADR_V_OFS	21	[31:0]	00000000
PHY_CSLVL_OBS2	DDR_PHY_ADR_V_OFS	22	[31:0]	00000000
PHY_CSLVL_ENABLE	DDR_PHY_ADR_V_OFS	23	[0]	1
PHY_CSLVL_FAST_EN	DDR_PHY_ADR_V_OFS	23	[8]	1
PHY_CSLVL_QTR	DDR_PHY_ADR_V_OFS	23	[25:16]	020
PHY_CSLVL_COARSE_CAPTURE_CNT	DDR_PHY_ADR_V_OFS	24	[3:0]	3
PHY_CSLVL_COARSE_CHK	DDR_PHY_ADR_V_OFS	24	[17:8]	02C

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Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PHY_CSLVL_PERIODIC_START_OFFSET	DDR_PHY_ADR_V_OFS	24	[31:24]	10
PHY_CSLVL_CS_MAP	DDR_PHY_ADR_V_OFS	25	[1:0]	3
SC_PHY_ACS_CDC_FIFO_POINTER_MANUAL_SYNC	DDR_PHY_ADR_V_OFS	25	[10:8]	0
PHY_AC_BYPASS_SLAVE_DELAY	DDR_PHY_ADR_V_OFS	25	[25:16]	080
PHY_ADR_CLK_WR_BYPASS_SLAVE_DELAY	DDR_PHY_ADR_V_OFS	26	[9:0]	080
PHY_SW_AC_BYPASS_SHIFT	DDR_PHY_ADR_V_OFS	26	[19:16]	1
PHY_AC_BYPASS_OVERRIDE	DDR_PHY_ADR_V_OFS	26	[24]	0
PHY_CLK_DC_CAL_SAMPLE_WAIT	DDR_PHY_ADR_V_OFS	27	[7:0]	08
PHY_CLK_DC_CAL_TIMEOUT	DDR_PHY_ADR_V_OFS	27	[15:8]	80
PHY_CLK_DC_WEIGHT	DDR_PHY_ADR_V_OFS	27	[17:16]	0
PHY_CLK_DC_FREQ_CHG_ADJ	DDR_PHY_ADR_V_OFS	27	[24]	0
PHY_CLK_DC_ADJUST_START	DDR_PHY_ADR_V_OFS	28	[5:0]	20
PHY_CLK_DC_ADJUST_SAMPLE_CNT	DDR_PHY_ADR_V_OFS	28	[15:8]	10
PHY_CLK_DC_ADJUST_THRSHLD	DDR_PHY_ADR_V_OFS	28	[23:16]	08
PHY_CLK_DC_ADJUST_DIRECT	DDR_PHY_ADR_V_OFS	28	[24]	0
PHY_CLK_DC_CAL_POLARITY	DDR_PHY_ADR_V_OFS	29	[0]	0
PHY_CLK_DC_CAL_START	DDR_PHY_ADR_V_OFS	29	[8]	0
PHY_CLK_DC_ADJUST_0	DDR_PHY_ADR_V_OFS	29	[23:16]	20
PHY_CLK_DC_INIT_DISABLE	DDR_PHY_ADR_V_OFS	29	[24]	0
PHY_MEMCLK_SW_TXPWR_CTRL	DDR_PHY_ADR_V_OFS	2A	[0]	1
PHY_MEMCLK_SW_TXIO_CTRL	DDR_PHY_ADR_V_OFS	2A	[8]	0
PHY_MEMCLK_STATIC_TOG_DISABLE	DDR_PHY_ADR_V_OFS	2A	[16]	1
PHY_AC_DCC_RXCAL_CTRL_GATE_DISABLE	DDR_PHY_ADR_V_OFS	2A	[24]	0
PHY_AC_LPBK_CONTROL	DDR_PHY_ADR_V_OFS	2B	[8:0]	000
PHY_ADRCTL_SW_MASTER_MODE	DDR_PHY_ADR_V_OFS	2B	[19:16]	0
PHY_ADRCTL_MASTER_DELAY_LOCK_MODE	DDR_PHY_ADR_V_OFS	2B	[26:24]	0
PHY_ADRCTL_MASTER_DELAY_LESS_STEP	DDR_PHY_ADR_V_OFS	2C	[2:0]	2
PHY_ADRCTL_MASTER_DELAY_THRESHOLD_FACTOR	DDR_PHY_ADR_V_OFS	2C	[10:8]	3
PHY_ADRCTL_MASTER_DELAY_START	DDR_PHY_ADR_V_OFS	2C	[26:16]	010
PHY_ADRCTL_MASTER_DELAY_STEP	DDR_PHY_ADR_V_OFS	2D	[5:0]	08
PHY_ADRCTL_MASTER_DELAY_WAIT	DDR_PHY_ADR_V_OFS	2D	[15:8]	42
PHY_ADRCTL_MASTER_DELAY_HALF_MEASURE	DDR_PHY_ADR_V_OFS	2D	[23:16]	3E
PHY_ACBIT0_SLAVE_DELAY_0	DDR_PHY_ADR_V_OFS	2E	[9:0]	180
PHY_ACBIT1_SLAVE_DELAY_0	DDR_PHY_ADR_V_OFS	2E	[25:16]	180
PHY_ACBIT2_SLAVE_DELAY_0	DDR_PHY_ADR_V_OFS	2F	[9:0]	180
PHY_ACBIT3_SLAVE_DELAY_0	DDR_PHY_ADR_V_OFS	2F	[25:16]	180
PHY_ACBIT0_SLAVE_DELAY_1	DDR_PHY_ADR_V_OFS	30	[9:0]	180
PHY_ACBIT1_SLAVE_DELAY_1	DDR_PHY_ADR_V_OFS	30	[25:16]	180
PHY_ACBIT2_SLAVE_DELAY_1	DDR_PHY_ADR_V_OFS	31	[9:0]	180
PHY_ACBIT3_SLAVE_DELAY_1	DDR_PHY_ADR_V_OFS	31	[25:16]	180
PHY_ACBIT0_SLAVE_DELAY_2	DDR_PHY_ADR_V_OFS	32	[9:0]	180
PHY_ACBIT1_SLAVE_DELAY_2	DDR_PHY_ADR_V_OFS	33	[9:0]	180
PHY_ACBIT2_SLAVE_DELAY_2	DDR_PHY_ADR_V_OFS	34	[9:0]	180
PHY_ACBIT3_SLAVE_DELAY_2	DDR_PHY_ADR_V_OFS	35	[9:0]	180

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Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PHY_ACBIT0_IS_TRAINED_2	DDR_PHY_ADR_V_OFS	36	[0]	0
PHY_ACBIT1_IS_TRAINED_2	DDR_PHY_ADR_V_OFS	37	[0]	0
PHY_ACBIT2_IS_TRAINED_2	DDR_PHY_ADR_V_OFS	38	[0]	0
PHY_ACBIT3_IS_TRAINED_2	DDR_PHY_ADR_V_OFS	39	[0]	0
PHY_CLK_DC_DM_THRSHLD	DDR_PHY_ADR_V_OFS	3A	[7:0]	80
PHY_CLK_DC_CAL_CLK_SEL	DDR_PHY_ADR_V_OFS	3A	[10:8]	5
PHY_CSLVL_DLY_STEP	DDR_PHY_ADR_V_OFS	3A	[19:16]	1
PHY_SW_CSLVL_DVW_MIN	DDR_PHY_ADR_V_OFS	3B	[8:0]	040
PHY_SW_CSLVL_DVW_MIN_EN	DDR_PHY_ADR_V_OFS	3B	[16]	0
PHY_CSLVL_CAPTURE_CNT	DDR_PHY_ADR_V_OFS	3B	[27:24]	3
PHY_LVL_MEAS_DLY_STEP_ENABLE	DDR_PHY_ADR_V_OFS	3C	[0]	1
PHY_FREQ_SEL	DDR_PHY_ADR_G_OFS	0	[2:0]	0
PHY_FREQ_SEL_FROM_REGIF	DDR_PHY_ADR_G_OFS	1	[0]	0
PHY_FREQ_SEL_MULTICAST_EN	DDR_PHY_ADR_G_OFS	1	[8]	1
PHY_FREQ_SEL_INDEX	DDR_PHY_ADR_G_OFS	1	[17:16]	0
PHY_FREQ_RATIO_FROM_REGIF	DDR_PHY_ADR_G_OFS	2	[0]	1
PHY_RPTR_RESET_ENABLE	DDR_PHY_ADR_G_OFS	3	[0]	0
PHY_LP4_BOOT_RX_PCLK_ACS_SELECT	DDR_PHY_ADR_G_OFS	3	[10:8]	0
PHY_LP4_BOOT_PAD_ACS_IO_CFG	DDR_PHY_ADR_G_OFS	3	[29:16]	2380
PHY_LP4_BOOT_PAD_CAL_IO_CFG_0	DDR_PHY_ADR_G_OFS	4	[17:0]	00000
SC_PHY_MANUAL_UPDATE	DDR_PHY_ADR_G_OFS	4	[24]	0
PHY_MANUAL_UPDATE_PHYUPD_ENABLE	DDR_PHY_ADR_G_OFS	5	[0]	1
PHY_IF_CLK_INVERT_FOR_LOW_FREQ	DDR_PHY_ADR_G_OFS	5	[8]	1
PHY_LP4_BOOT_DISABLE	DDR_PHY_ADR_G_OFS	5	[16]	0
PHY_DFI_PHYUPD_TYPE	DDR_PHY_ADR_G_OFS	5	[25:24]	1
SC_PHY_UPDATE_CLK_CAL_VALUES	DDR_PHY_ADR_G_OFS	6	[0]	0
PHY_CONTINUOUS_CLK_CAL_UPDATE	DDR_PHY_ADR_G_OFS	6	[8]	0
SC_PHY_UPDATE_WCK_CAL_VALUES	DDR_PHY_ADR_G_OFS	6	[16]	0
PHY_CONTINUOUS_WCK_CAL_UPDATE	DDR_PHY_ADR_G_OFS	6	[24]	1
PHY_TOP_PWR_RDC_DISABLE	DDR_PHY_ADR_G_OFS	7	[0]	0
PHY_USER_DEF_REG_AC_0	DDR_PHY_ADR_G_OFS	8	[31:0]	00000000
PHY_USER_DEF_REG_AC_1	DDR_PHY_ADR_G_OFS	9	[31:0]	00000000
PHY_USER_DEF_REG_AC_2	DDR_PHY_ADR_G_OFS	A	[31:0]	00000000
PHY_USER_DEF_REG_AC_3	DDR_PHY_ADR_G_OFS	B	[31:0]	00000000
PHY_TOP_STATIC_TOG_DISABLE	DDR_PHY_ADR_G_OFS	C	[0]	1
PHY_BYTE_DISABLE_STATIC_TOG_DISABLE	DDR_PHY_ADR_G_OFS	C	[8]	1
PHY_STATIC_TOG_CONTROL	DDR_PHY_ADR_G_OFS	C	[31:16]	0004
PHY_LP4_BOOT_PLL_BYPASS	DDR_PHY_ADR_G_OFS	D	[0]	0
PHY_CLK_SWITCH_OBS	DDR_PHY_ADR_G_OFS	E	[31:0]	00000000
PHY_PLL_WAIT	DDR_PHY_ADR_G_OFS	F	[7:0]	64
PHY_SW_PLL_BYPASS	DDR_PHY_ADR_G_OFS	10	[0]	0
PHY_SET_DFI_INPUT_0	DDR_PHY_ADR_G_OFS	11	[3:0]	0
PHY_SET_DFI_INPUT_1	DDR_PHY_ADR_G_OFS	11	[11:8]	0
PHY_SET_DFI_INPUT_2	DDR_PHY_ADR_G_OFS	11	[19:16]	0

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Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PHY_SET_DFI_INPUT_RST_PAD	DDR_PHY_ADR_G_OFS	11	[24]	0
PHY_LP4_BOOT_PLL_CTRL	DDR_PHY_ADR_G_OFS	12	[13:0]	1D42
PHY_LP4_BOOT_PLL_CTRL_8X	DDR_PHY_ADR_G_OFS	12	[29:16]	3B42
PHY_PLL_CTRL_OVERRIDE	DDR_PHY_ADR_G_OFS	13	[15:0]	0124
PHY_USE_PLL_DSKEWCALLOCK	DDR_PHY_ADR_G_OFS	13	[16]	1
PHY_PLL_SPO_CAL_CTRL_0	DDR_PHY_ADR_G_OFS	14	[9:0]	052
PHY_PLL_SPO_CAL_CTRL_1	DDR_PHY_ADR_G_OFS	14	[25:16]	052
PHY_PLL_SPO_CAL_CTRL_2	DDR_PHY_ADR_G_OFS	15	[9:0]	052
SC_PHY_PLL_SPO_CAL_SNAP_OBS	DDR_PHY_ADR_G_OFS	15	[18:16]	0
PHY_PLL_OBS_0	DDR_PHY_ADR_G_OFS	16	[15:0]	0000
PHY_PLL_SPO_CAL_OBS_0	DDR_PHY_ADR_G_OFS	17	[16:0]	00000
PHY_PLL_DESKEWCALIN_0	DDR_PHY_ADR_G_OFS	18	[11:0]	001
PHY_LP4_BOOT_PLL_DESKEWCALIN_0	DDR_PHY_ADR_G_OFS	18	[27:16]	001
PHY_PLL_OBS_1	DDR_PHY_ADR_G_OFS	19	[15:0]	0000
PHY_PLL_SPO_CAL_OBS_1	DDR_PHY_ADR_G_OFS	1A	[16:0]	00000
PHY_PLL_DESKEWCALIN_1	DDR_PHY_ADR_G_OFS	1B	[11:0]	001
PHY_LP4_BOOT_PLL_DESKEWCALIN_1	DDR_PHY_ADR_G_OFS	1B	[27:16]	001
PHY_PLL_OBS_2	DDR_PHY_ADR_G_OFS	1C	[15:0]	0000
PHY_PLL_SPO_CAL_OBS_2	DDR_PHY_ADR_G_OFS	1D	[16:0]	00000
PHY_PLL_DESKEWCALIN_2	DDR_PHY_ADR_G_OFS	1E	[11:0]	001
PHY_LP4_BOOT_PLL_DESKEWCALIN_2	DDR_PHY_ADR_G_OFS	1E	[27:16]	001
PHY_PLL_TESTOUT_SEL	DDR_PHY_ADR_G_OFS	1F	[1:0]	2
PHY_LP4_BOOT_LOW_FREQ_SEL	DDR_PHY_ADR_G_OFS	1F	[8]	1
PHY_TCKSRE_WAIT	DDR_PHY_ADR_G_OFS	1F	[19:16]	5
PHY_LP_CTRL_WAKEUP	DDR_PHY_ADR_G_OFS	1F	[29:24]	07
PHY_LP_DATA_WAKEUP	DDR_PHY_ADR_G_OFS	20	[5:0]	07
PHY_LP_LS_IDLE_CTRL_WAKEUP	DDR_PHY_ADR_G_OFS	20	[13:8]	03
PHY_LP_LS_IDLE_DATA_WAKEUP	DDR_PHY_ADR_G_OFS	20	[21:16]	03
PHY_LS_IDLE_EN	DDR_PHY_ADR_G_OFS	20	[24]	1
PHY_LP_CTRLUPD_CNTR_CFG	DDR_PHY_ADR_G_OFS	21	[9:0]	094
PHY_DS_EXIT_CTRL	DDR_PHY_ADR_G_OFS	22	[16:0]	04096
PHY_PAD_FDBK_TERM	DDR_PHY_ADR_G_OFS	23	[15:0]	0820
PHY_PAD_DATA_TERM	DDR_PHY_ADR_G_OFS	23	[27:16]	820
PHY_PAD_DQS_TERM	DDR_PHY_ADR_G_OFS	24	[11:0]	820
PHY_PAD_RDQS_TERM	DDR_PHY_ADR_G_OFS	24	[27:16]	820
PHY_PAD_ADDR_TERM	DDR_PHY_ADR_G_OFS	25	[15:0]	0820
PHY_PAD_CMD_TERM	DDR_PHY_ADR_G_OFS	25	[31:16]	0820
PHY_PAD_CLK_TERM	DDR_PHY_ADR_G_OFS	26	[12:0]	0820
PHY_PAD_CKE_TERM	DDR_PHY_ADR_G_OFS	26	[31:16]	0820
PHY_PAD_RST_TERM	DDR_PHY_ADR_G_OFS	27	[15:0]	0820
PHY_PAD_CS_TERM	DDR_PHY_ADR_G_OFS	27	[31:16]	0820
PHY_TST_CLK_PAD_CTRL	DDR_PHY_ADR_G_OFS	28	[31:0]	004103B8
PHY_TST_CLK_PAD_CTRL2	DDR_PHY_ADR_G_OFS	29	[23:0]	00003F
PHY_TST_CLK_PAD_CTRL3	DDR_PHY_ADR_G_OFS	2A	[22:0]	090006

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Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PHY_TST_CLK_PAD_CTRL4	DDR_PHY_ADR_G_OFS	2B	[26:0]	0000000
PHY_CAL_MODE_0	DDR_PHY_ADR_G_OFS	2C	[12:0]	0490
PHY_CAL_CLEAR_0	DDR_PHY_ADR_G_OFS	2C	[16]	0
PHY_CAL_START_0	DDR_PHY_ADR_G_OFS	2C	[24]	0
PHY_CAL_INTERVAL_COUNT_0	DDR_PHY_ADR_G_OFS	2D	[31:0]	00000000
PHY_CAL_SAMPLE_WAIT_0	DDR_PHY_ADR_G_OFS	2E	[7:0]	08
PHY_LP4_BOOT_CAL_CLK_SELECT_0	DDR_PHY_ADR_G_OFS	2E	[10:8]	1
PHY_CAL_RESULT_OBS_0	DDR_PHY_ADR_G_OFS	2F	[23:0]	000000
PHY_CAL_RESULT2_OBS_0	DDR_PHY_ADR_G_OFS	30	[23:0]	000000
PHY_CAL_RESULT4_OBS_0	DDR_PHY_ADR_G_OFS	31	[23:0]	000000
PHY_CAL_RESULT5_OBS_0	DDR_PHY_ADR_G_OFS	32	[23:0]	000000
PHY_CAL_RESULT6_OBS_0	DDR_PHY_ADR_G_OFS	33	[23:0]	000000
PHY_CAL_RESULT7_OBS_0	DDR_PHY_ADR_G_OFS	34	[23:0]	000000
PHY_CAL_CPTR_CNT_0	DDR_PHY_ADR_G_OFS	34	[30:24]	03
PHY_CAL_PU_FINE_ADJ_0	DDR_PHY_ADR_G_OFS	35	[7:0]	00
PHY_CAL_PD_FINE_ADJ_0	DDR_PHY_ADR_G_OFS	35	[15:8]	00
PHY_CAL_DBG_CFG_0	DDR_PHY_ADR_G_OFS	35	[16]	0
SC_PHY_PAD_DBG_CONT_0	DDR_PHY_ADR_G_OFS	35	[24]	0
PHY_CAL_RESULT3_OBS_0	DDR_PHY_ADR_G_OFS	36	[31:0]	00000000
PHY_ADRCTL_PVT_MAP_0	DDR_PHY_ADR_G_OFS	37	[8:0]	002
PHY_CAL_SLOPE_ADJ_0	DDR_PHY_ADR_G_OFS	38	[19:0]	41020
PHY_CAL_SLOPE_ADJ_PASS2_0	DDR_PHY_ADR_G_OFS	39	[19:0]	41020
PHY_CAL_TWO_PASS_CFG_0	DDR_PHY_ADR_G_OFS	3A	[24:0]	1C98C98
PHY_CAL_SW_CAL_CFG_0	DDR_PHY_ADR_G_OFS	3B	[22:0]	400000
PHY_CAL_RANGE_PASS1_PU_MAX_DELTA_0	DDR_PHY_ADR_G_OFS	3B	[29:24]	3F
PHY_CAL_RANGE_PASS1_PD_MAX_DELTA_0	DDR_PHY_ADR_G_OFS	3C	[5:0]	3F
PHY_CAL_RANGE_PASS2_PU_MAX_DELTA_0	DDR_PHY_ADR_G_OFS	3C	[13:8]	3F
PHY_CAL_RANGE_PASS2_PD_MAX_DELTA_0	DDR_PHY_ADR_G_OFS	3C	[21:16]	3F
PHY_CAL_RANGE_PASS1_PU_MIN_DELTA_0	DDR_PHY_ADR_G_OFS	3C	[29:24]	00
PHY_CAL_RANGE_PASS1_PD_MIN_DELTA_0	DDR_PHY_ADR_G_OFS	3D	[5:0]	00
PHY_CAL_RANGE_PASS2_PU_MIN_DELTA_0	DDR_PHY_ADR_G_OFS	3D	[13:8]	00
PHY_CAL_RANGE_PASS2_PD_MIN_DELTA_0	DDR_PHY_ADR_G_OFS	3D	[21:16]	00
PHY_PAD_ATB_CTRL	DDR_PHY_ADR_G_OFS	3E	[15:0]	0000
PHY_DATA_BYTE_ORDER_SEL	DDR_PHY_ADR_G_OFS	3F	[31:0]	76543210
PHY_DATA_BYTE_ORDER_SEL_HIGH	DDR_PHY_ADR_G_OFS	40	[7:0]	98
PHY_DFI_DATA_BYTE_DISABLE	DDR_PHY_ADR_G_OFS	40	[9:8]	0
PHY_LPDDR5_CONNECT	DDR_PHY_ADR_G_OFS	40	[16]	0
PHY_LPDDR5_DFI_ADDR_SEL	DDR_PHY_ADR_G_OFS	40	[24]	0
PHY_INIT_UPDATE_CONFIG	DDR_PHY_ADR_G_OFS	41	[2:0]	7
PHY_ERR_MASK_EN	DDR_PHY_ADR_G_OFS	41	[11:8]	0
PHY_ERR_STATUS	DDR_PHY_ADR_G_OFS	41	[18:16]	0
PHY_ERROR_INFO_TOP	DDR_PHY_ADR_G_OFS	41	[27:24]	0
PHY_ERROR_INFO_DS0	DDR_PHY_ADR_G_OFS	42	[0]	0
PHY_ERROR_INFO_DS1	DDR_PHY_ADR_G_OFS	42	[8]	0

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Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PHY_DS0_DQS_ERR_COUNTER	DDR_PHY_ADR_G_OFS	43	[31:0]	00000000
PHY_DS1_DQS_ERR_COUNTER	DDR_PHY_ADR_G_OFS	44	[31:0]	00000000
PHY_DLL_RST_EN	DDR_PHY_ADR_G_OFS	45	[1:0]	2
PHY_AC_INIT_COMPLETE_OBS	DDR_PHY_ADR_G_OFS	45	[18:8]	000
PHY_DS_INIT_COMPLETE_OBS	DDR_PHY_ADR_G_OFS	45	[25:24]	0
PHY_UPDATE_MASK	DDR_PHY_ADR_G_OFS	46	[0]	0
PHY_ACBIT_SLV_DLY_ENC_OBS_SELECT	DDR_PHY_ADR_G_OFS	46	[12:8]	00
PHY_ACBIT_SHIFT_OBS_SELECT	DDR_PHY_ADR_G_OFS	46	[19:16]	0
PHY_ACBIT_SLV_DLY_ENC_OBS	DDR_PHY_ADR_G_OFS	47	[9:0]	000
PHY_ACBIT_DDL_DLY_INFO_OBS	DDR_PHY_ADR_G_OFS	47	[17:16]	0
PHY_ACBIT_SHIFT_OBS	DDR_PHY_ADR_G_OFS	47	[26:24]	0
PHY_LP_LS_MSTR_PAUSE	DDR_PHY_ADR_G_OFS	48	[15:0]	017F
PHY_PAD_CAL_IO_CFG_0	DDR_PHY_ADR_G_OFS	49	[17:0]	00000
PHY_PAD_ACS_IO_CFG	DDR_PHY_ADR_G_OFS	4A	[13:0]	2380
PHY_PAD_ACS_RX_PCLK_CLK_SEL	DDR_PHY_ADR_G_OFS	4A	[18:16]	3
PHY_TOP_WCK_FREQ_RATIO	DDR_PHY_ADR_G_OFS	4A	[24]	0
PHY_TOP_LP4_BOOT_WCK_FREQ_RATIO	DDR_PHY_ADR_G_OFS	4B	[0]	0
PHY_TOP_WCK_FREQ_RATIO_USE_LP4_PRESTART	DDR_PHY_ADR_G_OFS	4B	[8]	1
PHY_PLL_BYPASS	DDR_PHY_ADR_G_OFS	4C	[0]	0
PHY_PLL_CTRL	DDR_PHY_ADR_G_OFS	4D	[13:0]	1142
PHY_PLL_CTRL_8X	DDR_PHY_ADR_G_OFS	4D	[29:16]	3142
PHY_LOW_FREQ_SEL	DDR_PHY_ADR_G_OFS	4E	[0]	0
PHY_PAD_VREF_CTRL_AC	DDR_PHY_ADR_G_OFS	4E	[21:8]	2480
PHY_PAD_VREF_H_CTRL_AC	DDR_PHY_ADR_G_OFS	4F	[13:0]	0080
PHY_PAD_FDBK_DRIVE	DDR_PHY_ADR_G_OFS	50	[29:0]	0004BF77
PHY_PAD_FDBK_DRIVE2	DDR_PHY_ADR_G_OFS	51	[20:0]	000006
PHY_PAD_DATA_DRIVE	DDR_PHY_ADR_G_OFS	52	[27:0]	000027F
PHY_PAD_DQS_DRIVE	DDR_PHY_ADR_G_OFS	53	[29:0]	0000027F
PHY_PAD_RDQS_DRIVE	DDR_PHY_ADR_G_OFS	54	[29:0]	0000027F
PHY_PAD_ADDR_DRIVE	DDR_PHY_ADR_G_OFS	55	[29:0]	00027F00
PHY_PAD_ADDR_DRIVE2	DDR_PHY_ADR_G_OFS	56	[29:0]	00CC0000
PHY_PAD_CMD_DRIVE	DDR_PHY_ADR_G_OFS	57	[29:0]	00027F00
PHY_PAD_CMD_DRIVE2	DDR_PHY_ADR_G_OFS	58	[29:0]	00CC0000
PHY_PAD_CLK_DRIVE	DDR_PHY_ADR_G_OFS	59	[31:0]	00027F77
PHY_PAD_CLK_DRIVE2	DDR_PHY_ADR_G_OFS	5A	[19:0]	00000
PHY_PAD_CKE_DRIVE	DDR_PHY_ADR_G_OFS	5B	[29:0]	00033F00
PHY_PAD_CKE_DRIVE2	DDR_PHY_ADR_G_OFS	5C	[29:0]	00EE0000
PHY_PAD_RST_DRIVE	DDR_PHY_ADR_G_OFS	5D	[29:0]	00027F00
PHY_PAD_RST_DRIVE2	DDR_PHY_ADR_G_OFS	5E	[29:0]	00EE0000
PHY_PAD_CS_DRIVE	DDR_PHY_ADR_G_OFS	5F	[29:0]	00027F00
PHY_PAD_CS_DRIVE2	DDR_PHY_ADR_G_OFS	60	[29:0]	00CC0000
PHY_CAL_CLK_SELECT_0	DDR_PHY_ADR_G_OFS	61	[2:0]	6
PHY_CAL_VREF_SWITCH_TIMER_0	DDR_PHY_ADR_G_OFS	61	[15:8]	01
PHY_CAL_SETTLING_PRD_0	DDR_PHY_ADR_G_OFS	61	[22:16]	20

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Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PHY_SLICE_MULTICAST_EN	DDR_PHY_ADR_G_OFS	61	[24]	0
PI_START	DDR_PI_OFS	0	[0]	0
PI_DRAM_CLASS	DDR_PI_OFS	0	[11:8]	B
PI_VERSION	DDR_PI_OFS	1	[31:0]	00000000
PI_VERSION_1	DDR_PI_OFS	2	[31:0]	00000000
PI_RELEASE_DFI	DDR_PI_OFS	3	[0]	0
PI_NORMAL_LVL_SEQ	DDR_PI_OFS	3	[8]	1
PI_INIT_LVL_EN	DDR_PI_OFS	3	[16]	1
PI_NOTCARE_PHYUPD	DDR_PI_OFS	3	[24]	0
PI_TCMD_GAP	DDR_PI_OFS	4	[15:0]	0004
PI_TRAIN_ALL_FREQ_REQ	DDR_PI_OFS	4	[24]	0
PI_DFI_VERSION	DDR_PI_OFS	5	[0]	1
PI_DFI_PHYMSTR_TYPE	DDR_PI_OFS	5	[9:8]	0
PI_DFI_PHYMSTR_CS_STATE_R	DDR_PI_OFS	5	[16]	0
PI_DFI_PHYMSTR_STATE_SEL_R	DDR_PI_OFS	5	[24]	0
PI_TDFI_PHYMSTR_MAX	DDR_PI_OFS	6	[31:0]	00000000
PI_TDFI_PHYMSTR_RESP	DDR_PI_OFS	7	[19:0]	00000
PI_TDFI_PHYUPD_RESP	DDR_PI_OFS	8	[19:0]	00000
PI_TDFI_PHYUPD_MAX	DDR_PI_OFS	9	[31:0]	00000000
PI_TPHYMSTR_RESP	DDR_PI_OFS	A	[31:0]	FFFFFFFF
PI_INIT_DFS_CALVL_ONLY	DDR_PI_OFS	B	[0]	0
PI_FSP_FREQ_EN	DDR_PI_OFS	B	[8]	0
PI_FSP0_FREQ	DDR_PI_OFS	B	[20:16]	01
PI_FSP1_FREQ	DDR_PI_OFS	B	[28:24]	02
PI_FSP2_FREQ	DDR_PI_OFS	C	[4:0]	03
PI_FREQ_MAP	DDR_PI_OFS	D	[31:0]	00000005
PI_INIT_WORK_FREQ	DDR_PI_OFS	E	[4:0]	02
PI_INIT_DFS_DISABLE_MAP	DDR_PI_OFS	F	[31:0]	00000000
PI_BOOT_FROM_WORK_FREQ	DDR_PI_OFS	10	[0]	1
PI_SW_RST_N	DDR_PI_OFS	10	[8]	1
PI_CS_MAP	DDR_PI_OFS	15	[9:8]	3
PI_MC_CS_MAP	DDR_PI_OFS	15	[17:16]	3
PI_SRX_LVL_TARGET_CS_EN	DDR_PI_OFS	15	[24]	0
PI_BYPASS_MC_CKE	DDR_PI_OFS	16	[1:0]	0
PI_VRCG_EN	DDR_PI_OFS	16	[10:8]	7
PI_UNMAP_CS	DDR_PI_OFS	16	[16]	1
PI_UNMAP_RESET	DDR_PI_OFS	16	[24]	1
PI_MCAREF_FORWARD_ONLY	DDR_PI_OFS	17	[0]	1
PI_ON_DFIBUS	DDR_PI_OFS	17	[16]	0
PI_DATA_RETENTION	DDR_PI_OFS	17	[24]	0
PI_AREF_WINDOW_SW	DDR_PI_OFS	18	[0]	1
PI_SWLVL_LOAD	DDR_PI_OFS	18	[8]	0
PI_SWLVL_OP_DONE	DDR_PI_OFS	18	[16]	0
PI_SW_WRLVL_RESP_0	DDR_PI_OFS	18	[24]	0

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Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PI_SW_WRLVL_RESP_1	DDR_PI_OFS	19	[0]	0
PI_SW_RDLVL_RESP_0	DDR_PI_OFS	19	[9:8]	0
PI_SW_RDLVL_RESP_1	DDR_PI_OFS	19	[17:16]	0
PI_SW_CALVL_RESP_0	DDR_PI_OFS	19	[25:24]	0
PI_SW_LEVELING_MODE	DDR_PI_OFS	1A	[2:0]	0
PI_SWLVL_START	DDR_PI_OFS	1A	[8]	0
PI_SWLVL_EXIT	DDR_PI_OFS	1A	[16]	0
PI_SWLVL_WR_SLICE_0	DDR_PI_OFS	1A	[24]	0
PI_SWLVL_RD_SLICE_0	DDR_PI_OFS	1B	[0]	0
PI_SWLVL_VREF_UPDATE_SLICE_0	DDR_PI_OFS	1B	[8]	0
PI_SW_WDQLVL_RESP_0	DDR_PI_OFS	1B	[17:16]	0
PI_SWLVL_WR_SLICE_1	DDR_PI_OFS	1B	[24]	0
PI_SWLVL_RD_SLICE_1	DDR_PI_OFS	1C	[0]	0
PI_SWLVL_VREF_UPDATE_SLICE_1	DDR_PI_OFS	1C	[8]	0
PI_SW_WDQLVL_RESP_1	DDR_PI_OFS	1C	[17:16]	0
PI_SWLVL_SM2_START	DDR_PI_OFS	1C	[24]	0
PI_SWLVL_SM2_WR	DDR_PI_OFS	1D	[0]	0
PI_SWLVL_SM2_RD	DDR_PI_OFS	1D	[8]	0
PI_SEQUENTIAL_LVL_REQ	DDR_PI_OFS	1D	[16]	0
PI_SWLVL_REQ	DDR_PI_OFS	1E	[12:0]	0000
PI_DFS_PERIOD_EN	DDR_PI_OFS	1E	[16]	0
PI_SRE_PERIOD_EN	DDR_PI_OFS	1E	[24]	0
PI_DFI40_POLARITY	DDR_PI_OFS	1F	[0]	0
PI_WRLVL_REQ	DDR_PI_OFS	1F	[8]	0
PI_WRLVL_CS_SW	DDR_PI_OFS	1F	[17:16]	1
PI_WLDQSEN	DDR_PI_OFS	1F	[29:24]	05
PI_WLMRD	DDR_PI_OFS	20	[5:0]	28
PI_WRLVL_INTERVAL	DDR_PI_OFS	20	[23:8]	0000
PI_WRLVL_PERIODIC	DDR_PI_OFS	20	[24]	0
PI_WRLVL_ON_SREF_EXIT	DDR_PI_OFS	21	[0]	0
PI_WRLVL_DISABLE_DFS	DDR_PI_OFS	21	[8]	0
PI_WRLVL_RESP_MASK	DDR_PI_OFS	21	[17:16]	0
PI_WRLVL_ROTATE	DDR_PI_OFS	21	[24]	0
PI_WRLVL_CS_MAP	DDR_PI_OFS	22	[1:0]	3
PI_WRLVL_ERROR_STATUS	DDR_PI_OFS	22	[8]	0
PI_TDFI_WRLVL_EN	DDR_PI_OFS	22	[23:16]	32
PI_TDFI_WRLVL_RESP	DDR_PI_OFS	23	[31:0]	00000000
PI_TDFI_WRLVL_MAX	DDR_PI_OFS	24	[31:0]	00000000
PI_WRLVL_STROBE_NUM	DDR_PI_OFS	25	[4:0]	02
PI_WRLVL_EN_OFF_TIMING	DDR_PI_OFS	25	[15:8]	20
PI_WRLVL_WCKON	DDR_PI_OFS	25	[19:16]	2
PI_WRLVL_CKON2OFF	DDR_PI_OFS	25	[31:24]	04
PI_WRLVL_CKOFF	DDR_PI_OFS	26	[15:0]	0100
PI_WRLVL_CKOFF2ON	DDR_PI_OFS	26	[23:16]	04

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Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PI_WRLVL_NO_WCK_SWITCH	DDR_PI_OFS	26	[24]	1
PI_TODTH_WR	DDR_PI_OFS	27	[3:0]	1
PI_TODTH_RD	DDR_PI_OFS	27	[11:8]	1
PI_RDLVL_REQ	DDR_PI_OFS	27	[16]	0
PI_RDLVL_GATE_REQ	DDR_PI_OFS	27	[24]	0
PI_RDLVL_CS_SW	DDR_PI_OFS	28	[1:0]	1
PI_RDLVL_PAT_0	DDR_PI_OFS	29	[31:0]	000000AA
PI_RDLVL_PAT_1	DDR_PI_OFS	2A	[31:0]	00000055
PI_RDLVL_PAT_2	DDR_PI_OFS	2B	[31:0]	000000B5
PI_RDLVL_PAT_3	DDR_PI_OFS	2C	[31:0]	0000004A
PI_RDLVL_PAT_4	DDR_PI_OFS	2D	[31:0]	00000056
PI_RDLVL_PAT_5	DDR_PI_OFS	2E	[31:0]	000000A9
PI_RDLVL_PAT_6	DDR_PI_OFS	2F	[31:0]	000000A9
PI_RDLVL_PAT_7	DDR_PI_OFS	30	[31:0]	000000B5
PI_RDLVL_SEQ_EN	DDR_PI_OFS	31	[3:0]	0
PI_RDLVL_PERIODIC	DDR_PI_OFS	31	[8]	0
PI_RDLVL_ON_SREF_EXIT	DDR_PI_OFS	31	[16]	0
PI_RDLVL_DISABLE_DFS	DDR_PI_OFS	31	[24]	0
PI_RDLVL_GATE_PERIODIC	DDR_PI_OFS	32	[0]	0
PI_RDLVL_GATE_ON_SREF_EXIT	DDR_PI_OFS	32	[8]	0
PI_RDLVL_GATE_DISABLE_DFS	DDR_PI_OFS	32	[16]	0
PI_RDLVL_ROTATE	DDR_PI_OFS	32	[24]	1
PI_RDLVL_GATE_ROTATE	DDR_PI_OFS	33	[0]	0
PI_RDLVL_CS_MAP	DDR_PI_OFS	33	[9:8]	3
PI_RDLVL_GATE_CS_MAP	DDR_PI_OFS	33	[17:16]	3
PI_TDFI_RDLVL_RR	DDR_PI_OFS	34	[9:0]	01A
PI_TDFI_RDLVL_RESP	DDR_PI_OFS	35	[31:0]	000007D0
PI_RDLVL_RESP_MASK	DDR_PI_OFS	36	[1:0]	0
PI_TDFI_RDLVL_EN	DDR_PI_OFS	36	[15:8]	03
PI_TDFI_RDLVL_MAX	DDR_PI_OFS	37	[31:0]	00000000
PI_RDLVL_ERROR_STATUS	DDR_PI_OFS	38	[0]	0
PI_RDLVL_INTERVAL	DDR_PI_OFS	38	[23:8]	0000
PI_RDLVL_GATE_INTERVAL	DDR_PI_OFS	39	[15:0]	0000
PI_RDLVL_PATTERN_START	DDR_PI_OFS	39	[19:16]	0
PI_RDLVL_PATTERN_NUM	DDR_PI_OFS	39	[27:24]	1
PI_RDLVL_STROBE_NUM	DDR_PI_OFS	3A	[4:0]	01
PI_RDLVL_GATE_STROBE_NUM	DDR_PI_OFS	3A	[12:8]	01
PI_RDDCM_LVL_ON_SREF_EXIT	DDR_PI_OFS	3A	[16]	0
PI_WRDCM_LVL_ON_SREF_EXIT	DDR_PI_OFS	3A	[24]	0
PI_DRAMDCA_LVL_ON_SREF_EXIT	DDR_PI_OFS	3B	[0]	0
PI_RDDCM_LVL_INTERVAL	DDR_PI_OFS	3B	[23:8]	0000
PI_WRDCM_LVL_INTERVAL	DDR_PI_OFS	3C	[15:0]	0000
PI_DRAMDCA_LVL_INTERVAL	DDR_PI_OFS	3C	[31:16]	0000
PI_RDDCM_LVL_DISABLE_DFS	DDR_PI_OFS	3D	[0]	0

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Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PI_WRDCM_LVL_DISABLE_DFS	DDR_PI_OFS	3D	[8]	0
PI_DRAMDCA_LVL_DISABLE_DFS	DDR_PI_OFS	3D	[16]	0
PI_DCMLVL_RESP_MASK	DDR_PI_OFS	3D	[25:24]	0
PI_DRAMDCA_BYTE_MASK	DDR_PI_OFS	3E	[1:0]	0
PI_DRAMDCA_FLIP_MASK	DDR_PI_OFS	3E	[9:8]	2
PI_RDDCM_LVL_ROTATE	DDR_PI_OFS	3E	[16]	0
PI_WRDCM_LVL_ROTATE	DDR_PI_OFS	3E	[24]	0
PI_DRAMDCA_LVL_ROTATE	DDR_PI_OFS	3F	[0]	0
PI_RDDCM_LVL_CS_MAP	DDR_PI_OFS	3F	[9:8]	3
PI_WRDCM_LVL_CS_MAP	DDR_PI_OFS	3F	[17:16]	3
PI_DRAMDCA_LVL_CS_MAP	DDR_PI_OFS	3F	[25:24]	3
PI_RDDCM_LVL_REQ	DDR_PI_OFS	40	[0]	0
PI_WRDCM_LVL_REQ	DDR_PI_OFS	40	[8]	0
PI_DRAMDCA_LVL_REQ	DDR_PI_OFS	40	[16]	0
PI_DCMLVL_CS_SW	DDR_PI_OFS	40	[25:24]	1
PI_RDDCM_LVL_EN_F0	DDR_PI_OFS	41	[1:0]	0
PI_WRDCM_LVL_EN_F0	DDR_PI_OFS	41	[9:8]	0
PI_DRAMDCA_LVL_EN_F0	DDR_PI_OFS	41	[17:16]	0
PI_RDDCM_LVL_EN_F1	DDR_PI_OFS	41	[25:24]	0
PI_WRDCM_LVL_EN_F1	DDR_PI_OFS	42	[1:0]	0
PI_DRAMDCA_LVL_EN_F1	DDR_PI_OFS	42	[9:8]	0
PI_RDDCM_LVL_EN_F2	DDR_PI_OFS	42	[17:16]	0
PI_WRDCM_LVL_EN_F2	DDR_PI_OFS	42	[25:24]	0
PI_DRAMDCA_LVL_EN_F2	DDR_PI_OFS	43	[1:0]	0
PI_DRAMDCA_START	DDR_PI_OFS	43	[11:8]	0
PI_DRAMDCA_AVG_ROUND	DDR_PI_OFS	43	[16]	1
PI_DRAMDCA_MINUS_RANGE	DDR_PI_OFS	43	[27:24]	7
PI_DRAMDCA_PLUS_RANGE	DDR_PI_OFS	44	[3:0]	7
PI_RD_PREAMBLE_TRAINING_EN	DDR_PI_OFS	44	[8]	1
PI_REG_DIMM_ENABLE	DDR_PI_OFS	44	[16]	0
PI_TDFI_RDDATA_EN	DDR_PI_OFS	45	[8:0]	000
PI_TDFI_PHY_WRLAT	DDR_PI_OFS	45	[24:16]	000
PI_CALVL_REQ	DDR_PI_OFS	46	[0]	0
PI_CALVL_CS_SW	DDR_PI_OFS	46	[9:8]	1
PI_CALVL_SEQ_EN	DDR_PI_OFS	46	[25:24]	3
PI_CALVL_PERIODIC	DDR_PI_OFS	47	[0]	0
PI_CALVL_ON_SREF_EXIT	DDR_PI_OFS	47	[8]	0
PI_CALVL_DISABLE_DFS	DDR_PI_OFS	47	[16]	0
PI_CALVL_ROTATE	DDR_PI_OFS	47	[24]	0
PI_CALVL_CS_MAP	DDR_PI_OFS	48	[1:0]	3
PI_TDFI_CALVL_EN	DDR_PI_OFS	48	[15:8]	17
PI_TDFI_CALVL_RESP	DDR_PI_OFS	49	[31:0]	00000000
PI_TDFI_CALVL_MAX	DDR_PI_OFS	4A	[31:0]	00000000
PI_CALVL_RESP_MASK	DDR_PI_OFS	4B	[0]	0

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Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PI_CALVL_ERROR_STATUS	DDR_PI_OFS	4B	[9:8]	0
PI_CALVL_INTERVAL	DDR_PI_OFS	4B	[31:16]	0000
PI_TCACKEL	DDR_PI_OFS	4C	[4:0]	0A
PI_TCAMRD	DDR_PI_OFS	4C	[14:8]	14
PI_TCACKEH	DDR_PI_OFS	4C	[20:16]	0A
PI_TCAEXT	DDR_PI_OFS	4C	[28:24]	0A
PI_CA_TRAIN_VREF_EN	DDR_PI_OFS	4D	[0]	1
PI_CALVL_VREF_INITIAL_STEPSIZE	DDR_PI_OFS	4D	[11:8]	4
PI_CALVL_VREF_NORMAL_STEPSIZE	DDR_PI_OFS	4D	[19:16]	2
PI_TDFI_INIT_START_MIN	DDR_PI_OFS	4D	[31:24]	10
PI_CALVL_STROBE_NUM	DDR_PI_OFS	4E	[4:0]	02
PI_SW_CA_TRAIN_VREF	DDR_PI_OFS	4E	[14:8]	00
PI_CALVL_PAT_0	DDR_PI_OFS	4E	[22:16]	00
PI_CALVL_PAT_1	DDR_PI_OFS	4E	[30:24]	00
PI_CALVL_PAT_2	DDR_PI_OFS	4F	[6:0]	00
PI_CALVL_PAT_3	DDR_PI_OFS	4F	[14:8]	00
PI_CALVL_PAT_NUM	DDR_PI_OFS	4F	[17:16]	1
PI_CALVL_MODE	DDR_PI_OFS	4F	[24]	0
PI_CLKDISABLE_2_INIT_START	DDR_PI_OFS	50	[7:0]	04
PI_INIT_STARTORCOMPLETE_2_CLKDISABLE	DDR_PI_OFS	50	[15:8]	04
PI_DRAM_CLK_DISABLE_DEASSERT_SEL	DDR_PI_OFS	50	[16]	0
PI_TDFI_INIT_COMPLETE_MIN	DDR_PI_OFS	50	[31:24]	0B
PI_TCKCKEH	DDR_PI_OFS	51	[3:0]	8
PI_TCKCKEL_F0	DDR_PI_OFS	51	[11:8]	5
PI_TCKCKEL_F1	DDR_PI_OFS	51	[19:16]	5
PI_TCKCKEL_F2	DDR_PI_OFS	51	[27:24]	B
PI_MC_DFS_PI_SET_VREF_ENABLE	DDR_PI_OFS	52	[0]	0
PI_WDQLVL_VREF_EN	DDR_PI_OFS	52	[11:8]	1
PI_WDQLVL_BST_NUM	DDR_PI_OFS	52	[18:16]	1
PI_WDQLVL_RESP_MASK	DDR_PI_OFS	52	[25:24]	0
PI_WDQLVL_ROTATE	DDR_PI_OFS	53	[0]	1
PI_WDQLVL_CS_MAP	DDR_PI_OFS	53	[9:8]	3
PI_WDQLVL_VREF_INITIAL_STEPSIZE	DDR_PI_OFS	53	[20:16]	02
PI_WDQLVL_VREF_NORMAL_STEPSIZE	DDR_PI_OFS	53	[28:24]	02
PI_WDQLVL_PERIODIC	DDR_PI_OFS	54	[0]	0
PI_WDQLVL_PERIODIC_NUM	DDR_PI_OFS	54	[15:8]	10
PI_WDQLVL_REQ	DDR_PI_OFS	54	[16]	0
PI_WDQLVL_CS_SW	DDR_PI_OFS	54	[25:24]	1
PI_TDFI_WDQLVL_EN	DDR_PI_OFS	55	[7:0]	34
PI_TDFI_WDQLVL_RESP	DDR_PI_OFS	56	[31:0]	00000000
PI_TDFI_WDQLVL_MAX	DDR_PI_OFS	57	[31:0]	00000000
PI_WDQLVL_INTERVAL	DDR_PI_OFS	58	[15:0]	0000
PI_WDQLVL_ON_SREF_EXIT	DDR_PI_OFS	58	[16]	0
PI_WDQLVL_DISABLE_DFS	DDR_PI_OFS	58	[24]	0

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Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PI_WDQLVL_ERROR_STATUS	DDR_PI_OFS	59	[1:0]	0
PI_WDQLVL_NEED_SAVE_RESTORE	DDR_PI_OFS	59	[9:8]	0
PI_WDQLVL_DM_LEVEL_EN	DDR_PI_OFS	59	[19:16]	0
PI_WDQLVL_DRAM_LVL_START_ADDR	DDR_PI_OFS	5A	[31:0]	00000000
PI_WDQLVL_DRAM_LVL_START_ADDR_1	DDR_PI_OFS	5B	[3:0]	0
PI_NO_MEMORY_DM	DDR_PI_OFS	5B	[8]	0
PI_TDFI_WDQLVL_WW	DDR_PI_OFS	5B	[25:16]	008
PI_SWLVL_SM2_DM_NIBBLE_START	DDR_PI_OFS	5C	[0]	0
PI_WDQLVL_NIBBLE_MODE	DDR_PI_OFS	5C	[8]	0
PI_USER_PATT0	DDR_PI_OFS	5D	[31:0]	55AA55AA
PI_USER_PATT1	DDR_PI_OFS	5E	[31:0]	33CC33CC
PI_USER_PATT2	DDR_PI_OFS	5F	[31:0]	0FF00FF0
PI_USER_PATT3	DDR_PI_OFS	60	[31:0]	0F0FF0F0
PI_USER_PATT4	DDR_PI_OFS	61	[15:0]	8E38
PI_PRBS23_0_SEED	DDR_PI_OFS	62	[22:0]	000001
PI_PRBS23_1_SEED	DDR_PI_OFS	63	[22:0]	000002
PI_PRBS15_0_SEED	DDR_PI_OFS	64	[14:0]	0001
PI_PRBS15_1_SEED	DDR_PI_OFS	64	[30:16]	0002
PI_PRBS11_0_SEED	DDR_PI_OFS	65	[10:0]	001
PI_PRBS11_1_SEED	DDR_PI_OFS	65	[26:16]	002
PI_PRBS8_0_SEED	DDR_PI_OFS	66	[7:0]	01
PI_PRBS8_1_SEED	DDR_PI_OFS	66	[15:8]	02
PI_PRBS7_0_SEED	DDR_PI_OFS	66	[22:16]	01
PI_PRBS7_1_SEED	DDR_PI_OFS	66	[30:24]	02
PI_PRBS_LENGTH	DDR_PI_OFS	67	[23:0]	00000F
PI_PRBS_LENGTH_DIV_F0	DDR_PI_OFS	67	[28:24]	00
PI_PRBS_LENGTH_DIV_F1	DDR_PI_OFS	68	[4:0]	00
PI_PRBS_LENGTH_DIV_F2	DDR_PI_OFS	68	[12:8]	00
PI_PRBS_LENGTH_DIV_ADV_F0	DDR_PI_OFS	68	[20:16]	00
PI_PRBS_LENGTH_DIV_ADV_F1	DDR_PI_OFS	68	[28:24]	00
PI_PRBS_LENGTH_DIV_ADV_F2	DDR_PI_OFS	69	[4:0]	00
PI_RD_B2B_INTERVAL_F0	DDR_PI_OFS	69	[31:8]	000000
PI_RD_B2B_INTERVAL_F1	DDR_PI_OFS	6A	[23:0]	000000
PI_RD_B2B_INTERVAL_F2	DDR_PI_OFS	6B	[23:0]	000000
PI_WDQLVL_CWL_DIFF_F0	DDR_PI_OFS	6B	[24]	0
PI_WDQLVL_CWL_F0	DDR_PI_OFS	6C	[2:0]	0
PI_NORMAL_CWL_F0	DDR_PI_OFS	6C	[10:8]	0
PI_WDQLVL_CWL_DIFF_F1	DDR_PI_OFS	6C	[16]	0
PI_WDQLVL_CWL_F1	DDR_PI_OFS	6C	[26:24]	0
PI_NORMAL_CWL_F1	DDR_PI_OFS	6D	[2:0]	0
PI_WDQLVL_CWL_DIFF_F2	DDR_PI_OFS	6D	[8]	0
PI_WDQLVL_CWL_F2	DDR_PI_OFS	6D	[18:16]	0
PI_NORMAL_CWL_F2	DDR_PI_OFS	6D	[26:24]	0
PI_PRBS_EVEN_BYTE_LANE_OFFSET	DDR_PI_OFS	6E	[31:0]	00000000

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Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PI_PRBS_ODD_BYTE_LANE_OFFSET	DDR_PI_OFS	6F	[31:0]	00000000
PI_PRBS_EVEN_BYTE_LANE_OFFSET_ADV	DDR_PI_OFS	70	[31:0]	00000000
PI_PRBS_ODD_BYTE_LANE_OFFSET_ADV	DDR_PI_OFS	71	[31:0]	00000000
PI_CUSTOM_PATT0	DDR_PI_OFS	72	[15:0]	9999
PI_CUSTOM_PATT1	DDR_PI_OFS	72	[31:16]	AAAA
PI_CUSTOM_PATT2	DDR_PI_OFS	73	[15:0]	9999
PI_CUSTOM_PATT3	DDR_PI_OFS	73	[31:16]	A593
PI_INVERT_PATT0	DDR_PI_OFS	74	[17:0]	00000
PI_INVERT_PATT1	DDR_PI_OFS	75	[17:0]	0AA55
PI_INVERT_PATT2	DDR_PI_OFS	76	[17:0]	06633
PI_INVERT_PATT3	DDR_PI_OFS	77	[17:0]	198CC
PI_FIX_PATT0	DDR_PI_OFS	78	[17:0]	00000
PI_FIX_PATT1	DDR_PI_OFS	79	[17:0]	3FFFF
PI_FIX_PATT2	DDR_PI_OFS	7A	[17:0]	06633
PI_FIX_PATT3	DDR_PI_OFS	7B	[17:0]	198CC
PI_DQ_TYPE_PATT0_EVEN	DDR_PI_OFS	7C	[26:0]	0000000
PI_DQ_TYPE_PATT1_EVEN	DDR_PI_OFS	7D	[26:0]	36DB6DB
PI_DQ_TYPE_PATT2_EVEN	DDR_PI_OFS	7E	[26:0]	0249249
PI_DQ_TYPE_PATT3_EVEN	DDR_PI_OFS	7F	[26:0]	5B6DB6D
PI_DQ_TYPE_PATT4_EVEN	DDR_PI_OFS	80	[26:0]	0000000
PI_DQ_TYPE_PATT5_EVEN	DDR_PI_OFS	81	[26:0]	0000000
PI_DQ_TYPE_PATT6_EVEN	DDR_PI_OFS	82	[26:0]	0000000
PI_DQ_TYPE_PATT7_EVEN	DDR_PI_OFS	83	[26:0]	0000000
PI_DQ_TYPE_PATT0_ODD	DDR_PI_OFS	84	[26:0]	0000000
PI_DQ_TYPE_PATT1_ODD	DDR_PI_OFS	85	[26:0]	36DB6DB
PI_DQ_TYPE_PATT2_ODD	DDR_PI_OFS	86	[26:0]	0249249
PI_DQ_TYPE_PATT3_ODD	DDR_PI_OFS	87	[26:0]	5B6DB6D
PI_DQ_TYPE_PATT4_ODD	DDR_PI_OFS	88	[26:0]	0000000
PI_DQ_TYPE_PATT5_ODD	DDR_PI_OFS	89	[26:0]	0000000
PI_DQ_TYPE_PATT6_ODD	DDR_PI_OFS	8A	[26:0]	0000000
PI_DQ_TYPE_PATT7_ODD	DDR_PI_OFS	8B	[26:0]	0000000
PI_RD_PATT_UI_IGNORE_F0	DDR_PI_OFS	8C	[7:0]	00
PI_RD_PATT_UI_IGNORE_F1	DDR_PI_OFS	8C	[15:8]	00
PI_RD_PATT_UI_IGNORE_F2	DDR_PI_OFS	8C	[23:16]	00
PI_RDWR_B2B_MODE	DDR_PI_OFS	8C	[24]	0
PI_RDWR_B2B_2ND_BANK	DDR_PI_OFS	8D	[3:0]	0
PI_WDQLVL_OSC_EN	DDR_PI_OFS	8D	[8]	0
PI_DQS_OSC_PERIOD_EN	DDR_PI_OFS	8D	[16]	0
PI_PARALLEL_WDQLVL_EN	DDR_PI_OFS	8D	[24]	1
PI_BANK_DIFF	DDR_PI_OFS	8E	[1:0]	1
PI_ROW_DIFF	DDR_PI_OFS	8E	[10:8]	1
PI_MR12_DATA_BEST_0_F0	DDR_PI_OFS	8E	[31:16]	0000
PI_MR12_DATA_BEST_0_F1	DDR_PI_OFS	8F	[15:0]	0000
PI_MR12_DATA_BEST_0_F2	DDR_PI_OFS	8F	[31:16]	0000

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Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PI_MR12_DATA_BEST_1_F0	DDR_PI_OFS	90	[15:0]	0000
PI_MR12_DATA_BEST_1_F1	DDR_PI_OFS	90	[31:16]	0000
PI_MR12_DATA_BEST_1_F2	DDR_PI_OFS	91	[15:0]	0000
PI_MR14_DATA_BEST_0_F0	DDR_PI_OFS	91	[31:16]	0000
PI_MR14_DATA_BEST_0_F1	DDR_PI_OFS	92	[15:0]	0000
PI_MR14_DATA_BEST_0_F2	DDR_PI_OFS	92	[31:16]	0000
PI_MR14_DATA_BEST_1_F0	DDR_PI_OFS	93	[15:0]	0000
PI_MR14_DATA_BEST_1_F1	DDR_PI_OFS	93	[31:16]	0000
PI_MR14_DATA_BEST_1_F2	DDR_PI_OFS	94	[15:0]	0000
PI_MR15_DATA_BEST_0_F0	DDR_PI_OFS	94	[23:16]	00
PI_MR15_DATA_BEST_0_F1	DDR_PI_OFS	95	[7:0]	00
PI_MR15_DATA_BEST_0_F2	DDR_PI_OFS	95	[23:16]	00
PI_MR15_DATA_BEST_1_F0	DDR_PI_OFS	96	[7:0]	00
PI_MR15_DATA_BEST_1_F1	DDR_PI_OFS	96	[23:16]	00
PI_MR15_DATA_BEST_1_F2	DDR_PI_OFS	97	[7:0]	00
PI_WDQLVL_BS_VREF_EN	DDR_PI_OFS	97	[16]	1
PI_WDQLVL_VREF_OUTLIER	DDR_PI_OFS	97	[26:24]	0
PI_WDQLVL_FINAL_VREF_OFFSET_F0	DDR_PI_OFS	98	[3:0]	0
PI_WDQLVL_FINAL_VREF_OFFSET_F1	DDR_PI_OFS	98	[11:8]	0
PI_WDQLVL_FINAL_VREF_OFFSET_F2	DDR_PI_OFS	98	[19:16]	0
PI_WDQLVL_BEST_VREF_LOWER_OBS_0_0_F0	DDR_PI_OFS	98	[31:24]	00
PI_WDQLVL_BEST_VREF_UPPER_OBS_0_0_F0	DDR_PI_OFS	99	[11:0]	000
PI_WDQLVL_BEST_VREF_LOWER_OBS_0_0_F1	DDR_PI_OFS	99	[23:16]	00
PI_WDQLVL_BEST_VREF_UPPER_OBS_0_0_F1	DDR_PI_OFS	9A	[11:0]	000
PI_WDQLVL_BEST_VREF_LOWER_OBS_0_0_F2	DDR_PI_OFS	9A	[23:16]	00
PI_WDQLVL_BEST_VREF_UPPER_OBS_0_0_F2	DDR_PI_OFS	9B	[11:0]	000
PI_WDQLVL_BEST_VREF_LOWER_OBS_1_0_F0	DDR_PI_OFS	9B	[23:16]	00
PI_WDQLVL_BEST_VREF_UPPER_OBS_1_0_F0	DDR_PI_OFS	9C	[11:0]	000
PI_WDQLVL_BEST_VREF_LOWER_OBS_1_0_F1	DDR_PI_OFS	9C	[23:16]	00
PI_WDQLVL_BEST_VREF_UPPER_OBS_1_0_F1	DDR_PI_OFS	9D	[11:0]	000
PI_WDQLVL_BEST_VREF_LOWER_OBS_1_0_F2	DDR_PI_OFS	9D	[23:16]	00
PI_WDQLVL_BEST_VREF_UPPER_OBS_1_0_F2	DDR_PI_OFS	9E	[11:0]	000
PI_WDQLVL_BEST_VREF_LOWER_OBS_0_1_F0	DDR_PI_OFS	9E	[23:16]	00
PI_WDQLVL_BEST_VREF_UPPER_OBS_0_1_F0	DDR_PI_OFS	9F	[11:0]	000
PI_WDQLVL_BEST_VREF_LOWER_OBS_0_1_F1	DDR_PI_OFS	9F	[23:16]	00
PI_WDQLVL_BEST_VREF_UPPER_OBS_0_1_F1	DDR_PI_OFS	A0	[11:0]	000
PI_WDQLVL_BEST_VREF_LOWER_OBS_0_1_F2	DDR_PI_OFS	A0	[23:16]	00
PI_WDQLVL_BEST_VREF_UPPER_OBS_0_1_F2	DDR_PI_OFS	A1	[11:0]	000
PI_WDQLVL_BEST_VREF_LOWER_OBS_1_1_F0	DDR_PI_OFS	A1	[23:16]	00
PI_WDQLVL_BEST_VREF_UPPER_OBS_1_1_F0	DDR_PI_OFS	A2	[11:0]	000
PI_WDQLVL_BEST_VREF_LOWER_OBS_1_1_F1	DDR_PI_OFS	A2	[23:16]	00
PI_WDQLVL_BEST_VREF_UPPER_OBS_1_1_F1	DDR_PI_OFS	A3	[11:0]	000
PI_WDQLVL_BEST_VREF_LOWER_OBS_1_1_F2	DDR_PI_OFS	A3	[23:16]	00
PI_WDQLVL_BEST_VREF_UPPER_OBS_1_1_F2	DDR_PI_OFS	A4	[11:0]	000

		V4M		
Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PI_CALVL_BS_VREF_EN	DDR_PI_OFS	A4	[16]	1
PI_CALVL_VREF_OUTLIER	DDR_PI_OFS	A4	[26:24]	0
PI_CALVL_FINAL_VREF_OFFSET_F0	DDR_PI_OFS	A5	[3:0]	0
PI_CALVL_FINAL_VREF_OFFSET_F1	DDR_PI_OFS	A5	[11:8]	0
PI_CALVL_FINAL_VREF_OFFSET_F2	DDR_PI_OFS	A5	[19:16]	0
PI_CALVL_BEST_VREF_LOWER_OBS_0_0_F0	DDR_PI_OFS	A5	[31:24]	00
PI_CALVL_BEST_VREF_UPPER_OBS_0_0_F0	DDR_PI_OFS	A6	[11:0]	000
PI_CALVL_BEST_VREF_LOWER_OBS_0_0_F1	DDR_PI_OFS	A6	[23:16]	00
PI_CALVL_BEST_VREF_UPPER_OBS_0_0_F1	DDR_PI_OFS	A7	[11:0]	000
PI_CALVL_BEST_VREF_LOWER_OBS_0_0_F2	DDR_PI_OFS	A7	[23:16]	00
PI_CALVL_BEST_VREF_UPPER_OBS_0_0_F2	DDR_PI_OFS	A8	[11:0]	000
PI_CALVL_BEST_VREF_LOWER_OBS_1_0_F0	DDR_PI_OFS	A8	[23:16]	00
PI_CALVL_BEST_VREF_UPPER_OBS_1_0_F0	DDR_PI_OFS	A9	[11:0]	000
PI_CALVL_BEST_VREF_LOWER_OBS_1_0_F1	DDR_PI_OFS	A9	[23:16]	00
PI_CALVL_BEST_VREF_UPPER_OBS_1_0_F1	DDR_PI_OFS	AA	[11:0]	000
PI_CALVL_BEST_VREF_LOWER_OBS_1_0_F2	DDR_PI_OFS	AA	[23:16]	00
PI_CALVL_BEST_VREF_UPPER_OBS_1_0_F2	DDR_PI_OFS	AB	[11:0]	000
PI_CALVL_BEST_VREF_LOWER_OBS_0_1_F0	DDR_PI_OFS	AB	[23:16]	00
PI_CALVL_BEST_VREF_UPPER_OBS_0_1_F0	DDR_PI_OFS	AC	[11:0]	000
PI_CALVL_BEST_VREF_LOWER_OBS_0_1_F1	DDR_PI_OFS	AC	[23:16]	00
PI_CALVL_BEST_VREF_UPPER_OBS_0_1_F1	DDR_PI_OFS	AD	[11:0]	000
PI_CALVL_BEST_VREF_LOWER_OBS_0_1_F2	DDR_PI_OFS	AD	[23:16]	00
PI_CALVL_BEST_VREF_UPPER_OBS_0_1_F2	DDR_PI_OFS	AE	[11:0]	000
PI_CALVL_BEST_VREF_LOWER_OBS_1_1_F0	DDR_PI_OFS	AE	[23:16]	00
PI_CALVL_BEST_VREF_UPPER_OBS_1_1_F0	DDR_PI_OFS	AF	[11:0]	000
PI_CALVL_BEST_VREF_LOWER_OBS_1_1_F1	DDR_PI_OFS	AF	[23:16]	00
PI_CALVL_BEST_VREF_UPPER_OBS_1_1_F1	DDR_PI_OFS	B0	[11:0]	000
PI_CALVL_BEST_VREF_LOWER_OBS_1_1_F2	DDR_PI_OFS	B0	[23:16]	00
PI_CALVL_BEST_VREF_UPPER_OBS_1_1_F2	DDR_PI_OFS	B1	[11:0]	000
PI_TCCD	DDR_PI_OFS	B1	[20:16]	08
PI_TRFC_TICK_PLUS_ADJ	DDR_PI_OFS	B1	[27:24]	0
PI_TRFC_TICK_MINUS_ADJ	DDR_PI_OFS	B2	[3:0]	0
PI_RL_TICK_PLUS_ADJ	DDR_PI_OFS	B2	[11:8]	2
PI_RL_TICK_MINUS_ADJ	DDR_PI_OFS	B2	[19:16]	0
PI_WL_TICK_PLUS_ADJ	DDR_PI_OFS	B2	[27:24]	2
PI_WL_TICK_MINUS_ADJ	DDR_PI_OFS	B3	[3:0]	0
PI_TMRR_TICK_PLUS_ADJ	DDR_PI_OFS	B3	[11:8]	1
PI_TMRR_TICK_MINUS_ADJ	DDR_PI_OFS	B3	[19:16]	0
PI_TMRD_TICK_PLUS_ADJ	DDR_PI_OFS	B3	[27:24]	1
PI_TMRD_TICK_MINUS_ADJ	DDR_PI_OFS	B4	[3:0]	0
PI_TRP_TICK_PLUS_ADJ	DDR_PI_OFS	B4	[11:8]	0
PI_TRP_TICK_MINUS_ADJ	DDR_PI_OFS	B4	[19:16]	0
PI_TRAS_TICK_PLUS_ADJ	DDR_PI_OFS	B4	[27:24]	1
PI_TRAS_TICK_MINUS_ADJ	DDR_PI_OFS	B5	[3:0]	0

		V4M		
Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PI_TRTP_TICK_PLUS_ADJ	DDR_PI_OFS	B5	[11:8]	2
PI_TRTP_TICK_MINUS_ADJ	DDR_PI_OFS	B5	[19:16]	0
PI_TWTR_TICK_PLUS_ADJ	DDR_PI_OFS	B5	[27:24]	2
PI_TWTR_TICK_MINUS_ADJ	DDR_PI_OFS	B6	[3:0]	0
PI_TWR_TICK_PLUS_ADJ	DDR_PI_OFS	B6	[11:8]	2
PI_TWR_TICK_MINUS_ADJ	DDR_PI_OFS	B6	[19:16]	0
PI_INT_STATUS	DDR_PI_OFS	B7	[31:0]	00000000
PI_INT_STATUS_1	DDR_PI_OFS	B8	[1:0]	0
PI_INT_ACK_0	DDR_PI_OFS	B9	[31:0]	00000000
PI_INT_ACK_1	DDR_PI_OFS	BA	[0]	0
PI_INT_MASK_0	DDR_PI_OFS	BB	[31:0]	00000000
PI_INT_MASK_1	DDR_PI_OFS	BC	[1:0]	0
PI_BSTLEN	DDR_PI_OFS	BC	[12:8]	04
PI_LONG_COUNT_MASK	DDR_PI_OFS	BC	[20:16]	00
PI_CMD_SWAP_EN	DDR_PI_OFS	BC	[24]	1
PI_ADDRESS_MUX_0	DDR_PI_OFS	BD	[2:0]	0
PI_ADDRESS_MUX_1	DDR_PI_OFS	BD	[10:8]	1
PI_ADDRESS_MUX_2	DDR_PI_OFS	BD	[18:16]	2
PI_ADDRESS_MUX_3	DDR_PI_OFS	BD	[26:24]	3
PI_ADDRESS_MUX_4	DDR_PI_OFS	BE	[2:0]	4
PI_ADDRESS_MUX_5	DDR_PI_OFS	BE	[10:8]	5
PI_ADDRESS_MUX_6	DDR_PI_OFS	BE	[18:16]	6
PI_DATA_BYTE_SWAP_EN	DDR_PI_OFS	BE	[24]	0
PI_DATA_BYTE_SWAP_SLICE0	DDR_PI_OFS	BF	[0]	0
PI_DATA_BYTE_SWAP_SLICE1	DDR_PI_OFS	BF	[8]	1
PI_CTRLUPD_REQ_PER_AREF_EN	DDR_PI_OFS	BF	[16]	1
PI_TDFI_CTRLUPD_MIN	DDR_PI_OFS	C0	[15:0]	0008
PI_UPDATE_ERROR_STATUS	DDR_PI_OFS	C0	[17:16]	0
PI_COL_DIFF	DDR_PI_OFS	C0	[27:24]	2
PI_BG_ROTATE_EN	DDR_PI_OFS	C1	[0]	0
PI_WR_DBI_EN	DDR_PI_OFS	C1	[8]	0
PI_RD_DBI_EN	DDR_PI_OFS	C1	[16]	0
PI_SELF_REFRESH_EN	DDR_PI_OFS	C1	[24]	0
PI_SREF_DSM_EN	DDR_PI_OFS	C2	[0]	1
PI_SREF_PD_EN	DDR_PI_OFS	C2	[8]	0
PI_PWRUP_SREFRESH_EXIT	DDR_PI_OFS	C2	[16]	0
PI_SRX_SEQ_EN	DDR_PI_OFS	C2	[24]	1
PI_SREF_ENTRY_REQ	DDR_PI_OFS	C3	[0]	0
PI_NO_PHY_IND_TRAIN_INIT	DDR_PI_OFS	C3	[8]	0
PI_NO_AUTO_MRR_INIT	DDR_PI_OFS	C3	[16]	0
PI_TRST_PWRON	DDR_PI_OFS	C4	[31:0]	0000000B
PI_CKE_INACTIVE	DDR_PI_OFS	C5	[31:0]	0000001C
PI_DLL_RST	DDR_PI_OFS	C6	[0]	0
PI_DRAM_INIT_EN	DDR_PI_OFS	C6	[8]	1

		V4M		
Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PI_DLL_RST_DELAY	DDR_PI_OFS	C6	[31:16]	0000
PI_DLL_RST_ADJ_DLY	DDR_PI_OFS	C7	[7:0]	00
PI_WRITE_MODEREG	DDR_PI_OFS	C8	[25:0]	0000000
PI_MRW_STATUS	DDR_PI_OFS	C9	[7:0]	00
PI_READ_MODEREG	DDR_PI_OFS	C9	[24:8]	00000
PI_PERIPHERAL_MRR_DATA_0	DDR_PI_OFS	CA	[23:0]	000000
PI_ZQ_REQ_PENDING	DDR_PI_OFS	CB	[8]	0
PI_MONITOR_SRC_SEL_0	DDR_PI_OFS	CC	[3:0]	0
PI_MONITOR_CAP_SEL_0	DDR_PI_OFS	CC	[8]	1
PI_MONITOR_0	DDR_PI_OFS	CC	[23:16]	00
PI_MONITOR_SRC_SEL_1	DDR_PI_OFS	CC	[27:24]	1
PI_MONITOR_CAP_SEL_1	DDR_PI_OFS	CD	[0]	1
PI_MONITOR_1	DDR_PI_OFS	CD	[15:8]	00
PI_MONITOR_SRC_SEL_2	DDR_PI_OFS	CD	[19:16]	2
PI_MONITOR_CAP_SEL_2	DDR_PI_OFS	CD	[24]	1
PI_MONITOR_2	DDR_PI_OFS	CE	[7:0]	00
PI_MONITOR_SRC_SEL_3	DDR_PI_OFS	CE	[11:8]	3
PI_MONITOR_CAP_SEL_3	DDR_PI_OFS	CE	[16]	1
PI_MONITOR_3	DDR_PI_OFS	CE	[31:24]	00
PI_MONITOR_SRC_SEL_4	DDR_PI_OFS	CF	[3:0]	4
PI_MONITOR_CAP_SEL_4	DDR_PI_OFS	CF	[8]	1
PI_MONITOR_4	DDR_PI_OFS	CF	[23:16]	00
PI_MONITOR_SRC_SEL_5	DDR_PI_OFS	CF	[27:24]	5
PI_MONITOR_CAP_SEL_5	DDR_PI_OFS	D0	[0]	1
PI_MONITOR_5	DDR_PI_OFS	D0	[15:8]	00
PI_MONITOR_SRC_SEL_6	DDR_PI_OFS	D0	[19:16]	6
PI_MONITOR_CAP_SEL_6	DDR_PI_OFS	D0	[24]	1
PI_MONITOR_6	DDR_PI_OFS	D1	[7:0]	00
PI_MONITOR_SRC_SEL_7	DDR_PI_OFS	D1	[11:8]	7
PI_MONITOR_CAP_SEL_7	DDR_PI_OFS	D1	[16]	1
PI_MONITOR_7	DDR_PI_OFS	D1	[31:24]	00
PI_MONITOR_STROBE	DDR_PI_OFS	D2	[7:0]	00
PI_DLL_LOCK	DDR_PI_OFS	D3	[0]	0
PI_FREQ_NUMBER_STATUS	DDR_PI_OFS	D3	[12:8]	00
PI_FREQ_RETENTION_NUM	DDR_PI_OFS	D3	[20:16]	00
PI_AREF_ENABLE_INIT	DDR_PI_OFS	D3	[24]	0
PI_PHYMSTR_TYPE	DDR_PI_OFS	D4	[1:0]	1
PI_POWER_REDUC_EN	DDR_PI_OFS	D4	[16]	1
PI_WRLVL_MAX_STROBE_PEND	DDR_PI_OFS	D9	[31:24]	01
PI_TREFBW_THR	DDR_PI_OFS	DA	[8:0]	008
PI_TREF_DIV4_SEL	DDR_PI_OFS	DA	[16]	0
PI_MC_SRX2PI_AREF_DISABLE	DDR_PI_OFS	DA	[24]	0
PI_CATR	DDR_PI_OFS	DC	[17:16]	1
PI_NO_CATR_READ	DDR_PI_OFS	DC	[24]	1

		V4M		
Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PI_MASK_INIT_COMPLETE	DDR_PI_OFS	DD	[0]	0
PI_DISCONNECT_MC	DDR_PI_OFS	DD	[8]	0
PI_NOTCARE_MC_INIT_START	DDR_PI_OFS	DD	[16]	0
PI_CMD_FREQ_RATIO	DDR_PI_OFS	DD	[25:24]	2
PI_MC_CMD_FREQ_RATIO	DDR_PI_OFS	DE	[1:0]	1
PI_DATA_FREQ_RATIO	DDR_PI_OFS	DE	[9:8]	2
PI_PHASE1_FLAG_DISABLE	DDR_PI_OFS	DE	[16]	0
PI_BYTE_MODE_EN	DDR_PI_OFS	DE	[24]	0
PI_WDQLVL_BYTE_MODE_EN	DDR_PI_OFS	DF	[0]	0
PI_WRDATA_EN_TUNE_PLUS	DDR_PI_OFS	DF	[11:8]	0
PI_WRDATA_EN_TUNE_MINUS	DDR_PI_OFS	DF	[19:16]	0
PI_RDDATA_EN_TUNE_PLUS	DDR_PI_OFS	DF	[27:24]	0
PI_RDDATA_EN_TUNE_MINUS	DDR_PI_OFS	E0	[3:0]	0
PI_WRDATA_TUNE_PLUS	DDR_PI_OFS	E0	[9:8]	3
PI_WRDATA_TUNE_MINUS	DDR_PI_OFS	E0	[17:16]	0
PI_AREF_TICK0	DDR_PI_OFS	E0	[31:24]	C8
PI_AREF_TICK0_VALID	DDR_PI_OFS	E1	[7:0]	DF
PI_AREF_TICK1	DDR_PI_OFS	E1	[15:8]	00
PI_AREF_TICK1_VALID	DDR_PI_OFS	E1	[23:16]	00
PI_AREF_CMD_COUNT	DDR_PI_OFS	E1	[26:24]	1
PI_SRE_TICK0	DDR_PI_OFS	E2	[7:0]	D8
PI_SRE_TICK0_VALID	DDR_PI_OFS	E2	[15:8]	DF
PI_SRE_TICK1	DDR_PI_OFS	E2	[23:16]	00
PI_SRE_TICK1_VALID	DDR_PI_OFS	E2	[31:24]	00
PI_SRE_CMD_COUNT	DDR_PI_OFS	E3	[2:0]	1
PI_SRX_TICK0	DDR_PI_OFS	E3	[15:8]	D4
PI_SRX_TICK0_VALID	DDR_PI_OFS	E3	[23:16]	DF
PI_SRX_TICK1	DDR_PI_OFS	E3	[31:24]	00
PI_SRX_TICK1_VALID	DDR_PI_OFS	E4	[7:0]	00
PI_SRX_CMD_COUNT	DDR_PI_OFS	E4	[10:8]	1
PI_FSPOP_FSPWR_TICK0	DDR_PI_OFS	E4	[23:16]	C6
PI_FSPOP_FSPWR_TICK0_VALID	DDR_PI_OFS	E4	[31:24]	DF
PI_FSPOP_FSPWR_TICK1	DDR_PI_OFS	E5	[7:0]	4D
PI_FSPOP_FSPWR_TICK1_VALID	DDR_PI_OFS	E5	[15:8]	DF
PI_TSDO_F0	DDR_PI_OFS	E5	[23:16]	02
PI_TSDO_F1	DDR_PI_OFS	E5	[31:24]	10
PI_TSDO_F2	DDR_PI_OFS	E6	[7:0]	2B
PI_TDELAY_RDWR_2_BUS_IDLE_F0	DDR_PI_OFS	E7	[7:0]	30
PI_TDELAY_RDWR_2_BUS_IDLE_F1	DDR_PI_OFS	E8	[7:0]	40
PI_TDELAY_RDWR_2_BUS_IDLE_F2	DDR_PI_OFS	E9	[7:0]	64
PI_ZQINIT_F0	DDR_PI_OFS	E9	[19:8]	200
PI_ZQINIT_F1	DDR_PI_OFS	EA	[11:0]	200
PI_ZQINIT_F2	DDR_PI_OFS	EA	[27:16]	200
PI_WRLAT_F0	DDR_PI_OFS	EB	[6:0]	04

		V4M		
Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PI_TWCKENL_WR_ADJ_F0	DDR_PI_OFS	EB	[13:8]	00
PI_TWCKENL_RD_ADJ_F0	DDR_PI_OFS	EB	[21:16]	00
PI_TWCKPRE_STATIC_F0	DDR_PI_OFS	EB	[29:24]	00
PI_TWCKPRE_TOGGLE_WR_F0	DDR_PI_OFS	EC	[5:0]	00
PI_TWCKPRE_TOGGLE_RD_F0	DDR_PI_OFS	EC	[13:8]	00
PI_WCK_ACTIVE_WR_F0	DDR_PI_OFS	EC	[22:16]	09
PI_WCK_ACTIVE_RD_F0	DDR_PI_OFS	EC	[30:24]	0B
PI_TWCKENL_FS_ADJ_F0	DDR_PI_OFS	ED	[5:0]	00
PI_CASLAT_F0	DDR_PI_OFS	ED	[14:8]	06
PI_WRLAT_F1	DDR_PI_OFS	ED	[22:16]	0C
PI_TWCKENL_WR_ADJ_F1	DDR_PI_OFS	ED	[29:24]	00
PI_TWCKENL_RD_ADJ_F1	DDR_PI_OFS	EE	[5:0]	00
PI_TWCKPRE_STATIC_F1	DDR_PI_OFS	EE	[13:8]	00
PI_TWCKPRE_TOGGLE_WR_F1	DDR_PI_OFS	EE	[21:16]	00
PI_TWCKPRE_TOGGLE_RD_F1	DDR_PI_OFS	EE	[29:24]	00
PI_WCK_ACTIVE_WR_F1	DDR_PI_OFS	EF	[6:0]	11
PI_WCK_ACTIVE_RD_F1	DDR_PI_OFS	EF	[14:8]	15
PI_TWCKENL_FS_ADJ_F1	DDR_PI_OFS	EF	[21:16]	00
PI_CASLAT_F1	DDR_PI_OFS	EF	[30:24]	10
PI_WRLAT_F2	DDR_PI_OFS	F0	[6:0]	12
PI_TWCKENL_WR_ADJ_F2	DDR_PI_OFS	F0	[13:8]	00
PI_TWCKENL_RD_ADJ_F2	DDR_PI_OFS	F0	[21:16]	00
PI_TWCKPRE_STATIC_F2	DDR_PI_OFS	F0	[29:24]	00
PI_TWCKPRE_TOGGLE_WR_F2	DDR_PI_OFS	F1	[5:0]	00
PI_TWCKPRE_TOGGLE_RD_F2	DDR_PI_OFS	F1	[13:8]	00
PI_WCK_ACTIVE_WR_F2	DDR_PI_OFS	F1	[22:16]	17
PI_WCK_ACTIVE_RD_F2	DDR_PI_OFS	F1	[30:24]	2D
PI_TWCKENL_FS_ADJ_F2	DDR_PI_OFS	F2	[5:0]	00
PI_CASLAT_F2	DDR_PI_OFS	F2	[14:8]	28
PI_TRFC_F0	DDR_PI_OFS	F2	[25:16]	015
PI_TREF_F0	DDR_PI_OFS	F3	[19:0]	000CF
PI_TRFC_F1	DDR_PI_OFS	F4	[9:0]	130
PI_TREF_F1	DDR_PI_OFS	F5	[19:0]	00C2E
PI_TRFC_F2	DDR_PI_OFS	F6	[9:0]	32B
PI_TREF_F2	DDR_PI_OFS	F7	[19:0]	02082
PI_TREF_OFFSET	DDR_PI_OFS	F7	[28:24]	10
PI_TDFI_CTRL_DELAY_F0	DDR_PI_OFS	F8	[3:0]	4
PI_TDFI_CTRL_DELAY_F1	DDR_PI_OFS	F8	[11:8]	4
PI_TDFI_CTRL_DELAY_F2	DDR_PI_OFS	F8	[19:16]	4
PI_WRLVL_WICA_EN	DDR_PI_OFS	F8	[24]	0
PI_WRLVL_EN_F0	DDR_PI_OFS	F9	[1:0]	0
PI_TDFI_WRLVL_WW_F0	DDR_PI_OFS	F9	[17:8]	021
PI_WRLVL_WCKOFF_F0	DDR_PI_OFS	F9	[31:24]	08
PI_WRLVL_EN_F1	DDR_PI_OFS	FA	[1:0]	1

		V4M		
Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PI_TDFI_WRLVL_WW_F1	DDR_PI_OFS	FA	[17:8]	01B
PI_WRLVL_WCKOFF_F1	DDR_PI_OFS	FA	[31:24]	0F
PI_WRLVL_EN_F2	DDR_PI_OFS	FB	[1:0]	1
PI_TDFI_WRLVL_WW_F2	DDR_PI_OFS	FB	[17:8]	021
PI_WRLVL_WCKOFF_F2	DDR_PI_OFS	FB	[31:24]	21
PI_TODTL_2CMD_F0	DDR_PI_OFS	FC	[7:0]	00
PI_ODT_EN_F0	DDR_PI_OFS	FC	[8]	0
PI_TODTL_2CMD_F1	DDR_PI_OFS	FC	[23:16]	00
PI_ODT_EN_F1	DDR_PI_OFS	FC	[24]	0
PI_TODTL_2CMD_F2	DDR_PI_OFS	FD	[7:0]	00
PI_ODT_EN_F2	DDR_PI_OFS	FD	[8]	0
PI_ODTLON_F0	DDR_PI_OFS	FD	[19:16]	0
PI_TODTON_MIN_F0	DDR_PI_OFS	FD	[27:24]	0
PI_ODTLON_F1	DDR_PI_OFS	FE	[3:0]	0
PI_TODTON_MIN_F1	DDR_PI_OFS	FE	[11:8]	0
PI_ODTLON_F2	DDR_PI_OFS	FE	[19:16]	0
PI_TODTON_MIN_F2	DDR_PI_OFS	FE	[27:24]	0
PI_RDLVL_EN_F0	DDR_PI_OFS	FF	[1:0]	0
PI_RDLVL_GATE_EN_F0	DDR_PI_OFS	FF	[9:8]	0
PI_RDLVL_EN_F1	DDR_PI_OFS	FF	[17:16]	1
PI_RDLVL_GATE_EN_F1	DDR_PI_OFS	FF	[25:24]	1
PI_RDLVL_EN_F2	DDR_PI_OFS	100	[1:0]	1
PI_RDLVL_GATE_EN_F2	DDR_PI_OFS	100	[9:8]	1
PI_RDLVL_RDDQ_EN_F0	DDR_PI_OFS	100	[19:16]	0
PI_RDLVL_VREF_EN_F0	DDR_PI_OFS	100	[27:24]	1
PI_RDLVL_PAT0_EN_F0	DDR_PI_OFS	101	[1:0]	0
PI_RDLVL_RXCAL_EN_F0	DDR_PI_OFS	101	[9:8]	0
PI_RDLVL_DFE_EN_F0	DDR_PI_OFS	101	[19:16]	0
PI_RDLVL_MULTI_EN_F0	DDR_PI_OFS	101	[27:24]	3
PI_RDLVL_RDDQ_EN_F1	DDR_PI_OFS	102	[3:0]	0
PI_RDLVL_VREF_EN_F1	DDR_PI_OFS	102	[11:8]	1
PI_RDLVL_PAT0_EN_F1	DDR_PI_OFS	102	[17:16]	0
PI_RDLVL_RXCAL_EN_F1	DDR_PI_OFS	102	[25:24]	0
PI_RDLVL_DFE_EN_F1	DDR_PI_OFS	103	[3:0]	0
PI_RDLVL_MULTI_EN_F1	DDR_PI_OFS	103	[11:8]	3
PI_RDLVL_RDDQ_EN_F2	DDR_PI_OFS	103	[19:16]	0
PI_RDLVL_VREF_EN_F2	DDR_PI_OFS	103	[27:24]	1
PI_RDLVL_PAT0_EN_F2	DDR_PI_OFS	104	[1:0]	0
PI_RDLVL_RXCAL_EN_F2	DDR_PI_OFS	104	[9:8]	0
PI_RDLVL_DFE_EN_F2	DDR_PI_OFS	104	[19:16]	0
PI_RDLVL_MULTI_EN_F2	DDR_PI_OFS	104	[27:24]	3
PI_RDLAT_ADJ_F0	DDR_PI_OFS	105	[8:0]	004
PI_RDLAT_ADJ_F1	DDR_PI_OFS	105	[24:16]	00A
PI_RDLAT_ADJ_F2	DDR_PI_OFS	106	[8:0]	019

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Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PI_WRLAT_ADJ_F0	DDR_PI_OFS	106	[22:16]	02
PI_WRLAT_ADJ_F1	DDR_PI_OFS	106	[30:24]	08
PI_WRLAT_ADJ_F2	DDR_PI_OFS	107	[6:0]	0E
PI_TDFI_PHY_WRDATA_F0	DDR_PI_OFS	107	[10:8]	2
PI_TDFI_PHY_WRDATA_F1	DDR_PI_OFS	107	[18:16]	4
PI_TDFI_PHY_WRDATA_F2	DDR_PI_OFS	107	[26:24]	4
PI_TDFI_CALVL_CC_F0	DDR_PI_OFS	108	[9:0]	034
PI_TDFI_CALVL_CAPTURE_F0	DDR_PI_OFS	108	[25:16]	00C
PI_TDFI_CALVL_CC_F1	DDR_PI_OFS	109	[9:0]	03B
PI_TDFI_CALVL_CAPTURE_F1	DDR_PI_OFS	109	[25:16]	013
PI_TDFI_CALVL_CC_F2	DDR_PI_OFS	10A	[9:0]	049
PI_TDFI_CALVL_CAPTURE_F2	DDR_PI_OFS	10A	[25:16]	021
PI_CALVL_EN_F0	DDR_PI_OFS	10B	[1:0]	1
PI_CALVL_EN_F1	DDR_PI_OFS	10B	[9:8]	1
PI_CALVL_EN_F2	DDR_PI_OFS	10B	[17:16]	1
PI_TMRZ_F0	DDR_PI_OFS	10B	[28:24]	01
PI_TCAENT_F0	DDR_PI_OFS	10C	[13:0]	000E
PI_TMRZ_F1	DDR_PI_OFS	10C	[20:16]	02
PI_TCAENT_F1	DDR_PI_OFS	10D	[13:0]	00C8
PI_TMRZ_F2	DDR_PI_OFS	10D	[20:16]	04
PI_TCAENT_F2	DDR_PI_OFS	10E	[13:0]	0216
PI_TDFI_CACSCA_F0	DDR_PI_OFS	10E	[20:16]	00
PI_TDFI_CASEL_F0	DDR_PI_OFS	10E	[28:24]	01
PI_TVREF_SHORT_F0	DDR_PI_OFS	10F	[9:0]	00F
PI_TVREF_LONG_F0	DDR_PI_OFS	10F	[25:16]	00F
PI_TVRCG_ENABLE_F0	DDR_PI_OFS	110	[9:0]	00C
PI_TVRCG_DISABLE_F0	DDR_PI_OFS	110	[25:16]	007
PI_TDFI_CACSCA_F1	DDR_PI_OFS	111	[4:0]	00
PI_TDFI_CASEL_F1	DDR_PI_OFS	111	[12:8]	01
PI_TVREF_SHORT_F1	DDR_PI_OFS	111	[25:16]	0C9
PI_TVREF_LONG_F1	DDR_PI_OFS	112	[9:0]	0C9
PI_TVRCG_ENABLE_F1	DDR_PI_OFS	112	[25:16]	0A1
PI_TVRCG_DISABLE_F1	DDR_PI_OFS	113	[9:0]	051
PI_TDFI_CACSCA_F2	DDR_PI_OFS	113	[20:16]	00
PI_TDFI_CASEL_F2	DDR_PI_OFS	113	[28:24]	01
PI_TVREF_SHORT_F2	DDR_PI_OFS	114	[9:0]	217
PI_TVREF_LONG_F2	DDR_PI_OFS	114	[25:16]	217
PI_TVRCG_ENABLE_F2	DDR_PI_OFS	115	[9:0]	1AC
PI_TVRCG_DISABLE_F2	DDR_PI_OFS	115	[25:16]	0D7
PI_CALVL_VREF_INITIAL_START_POINT_F0	DDR_PI_OFS	116	[6:0]	15
PI_CALVL_VREF_INITIAL_STOP_POINT_F0	DDR_PI_OFS	116	[14:8]	15
PI_CALVL_VREF_DELTA_F0	DDR_PI_OFS	116	[19:16]	0
PI_CALVL_VREF_INITIAL_START_POINT_F1	DDR_PI_OFS	116	[30:24]	15
PI_CALVL_VREF_INITIAL_STOP_POINT_F1	DDR_PI_OFS	117	[6:0]	15

		V4M		
Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PI_CALVL_VREF_DELTA_F1	DDR_PI_OFS	117	[11:8]	0
PI_CALVL_VREF_INITIAL_START_POINT_F2	DDR_PI_OFS	117	[22:16]	0B
PI_CALVL_VREF_INITIAL_STOP_POINT_F2	DDR_PI_OFS	117	[30:24]	1F
PI_CALVL_VREF_DELTA_F2	DDR_PI_OFS	118	[3:0]	0
PI_TDFI_CALVL_STROBE_F0	DDR_PI_OFS	118	[11:8]	6
PI_TXP_F0	DDR_PI_OFS	118	[20:16]	07
PI_TMRWCKEL_F0	DDR_PI_OFS	118	[31:24]	0A
PI_TCKELCK_F0	DDR_PI_OFS	119	[4:0]	0D
PI_TDFI_CALVL_STROBE_F1	DDR_PI_OFS	119	[11:8]	7
PI_TXP_F1	DDR_PI_OFS	119	[20:16]	09
PI_TMRWCKEL_F1	DDR_PI_OFS	119	[31:24]	0D
PI_TCKELCK_F1	DDR_PI_OFS	11A	[4:0]	0D
PI_TDFI_CALVL_STROBE_F2	DDR_PI_OFS	11A	[11:8]	A
PI_TXP_F2	DDR_PI_OFS	11A	[20:16]	13
PI_TMRWCKEL_F2	DDR_PI_OFS	11A	[31:24]	1F
PI_TCKELCK_F2	DDR_PI_OFS	11B	[4:0]	14
PI_TDFI_INIT_START_F0	DDR_PI_OFS	11B	[31:8]	000C00
PI_TDFI_INIT_COMPLETE_F0	DDR_PI_OFS	11C	[23:0]	001000
PI_TDFI_INIT_START_F1	DDR_PI_OFS	11D	[23:0]	000C00
PI_TDFI_INIT_COMPLETE_F1	DDR_PI_OFS	11E	[23:0]	001000
PI_TDFI_INIT_START_F2	DDR_PI_OFS	11F	[23:0]	000C00
PI_TDFI_INIT_COMPLETE_F2	DDR_PI_OFS	120	[23:0]	001000
PI_TCKEHDQS_F0	DDR_PI_OFS	120	[29:24]	02
PI_TFC_F0	DDR_PI_OFS	121	[9:0]	00E
PI_TCKEHDQS_F1	DDR_PI_OFS	121	[21:16]	16
PI_TFC_F1	DDR_PI_OFS	122	[9:0]	0C8
PI_TCKEHDQS_F2	DDR_PI_OFS	122	[21:16]	24
PI_TFC_F2	DDR_PI_OFS	123	[9:0]	216
PI_WDQLVL_NTP_VREF_START_POINT	DDR_PI_OFS	123	[22:16]	1A
PI_WDQLVL_NTP_VREF_STOP_POINT	DDR_PI_OFS	123	[30:24]	1E
PI_WDQLVL_NTP_VREF_STEPSIZE	DDR_PI_OFS	124	[4:0]	04
PI_NTP_MULT_TRAIN	DDR_PI_OFS	124	[8]	0
PI_TDFI_WDQLVL_WR_F0	DDR_PI_OFS	124	[25:16]	021
PI_TDFI_WDQLVL_RW_F0	DDR_PI_OFS	125	[9:0]	020
PI_WDQLVL_VREF_INITIAL_START_POINT_F0	DDR_PI_OFS	125	[22:16]	0E
PI_WDQLVL_VREF_INITIAL_STOP_POINT_F0	DDR_PI_OFS	125	[30:24]	22
PI_WDQLVL_VREF_DELTA_F0	DDR_PI_OFS	126	[3:0]	0
PI_WDQLVL_EN_F0	DDR_PI_OFS	126	[9:8]	0
PI_NTP_TRAIN_EN_F0	DDR_PI_OFS	126	[19:16]	1
PI_NORMAL_CL_F0	DDR_PI_OFS	126	[28:24]	00
PI_WDQLVL_RDLAT_ADJ_F0	DDR_PI_OFS	127	[8:0]	004
PI_WDQLVL_WRLAT_ADJ_F0	DDR_PI_OFS	127	[24:16]	002
PI_WDQLVL_TWCKENL_RD_ADJ_F0	DDR_PI_OFS	128	[5:0]	00
PI_TDFI_WDQLVL_WR_F1	DDR_PI_OFS	128	[17:8]	029

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Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PI_TDFI_WDQLVL_RW_F1	DDR_PI_OFS	129	[9:0]	02D
PI_WDQLVL_VREF_INITIAL_START_POINT_F1	DDR_PI_OFS	129	[22:16]	0E
PI_WDQLVL_VREF_INITIAL_STOP_POINT_F1	DDR_PI_OFS	129	[30:24]	22
PI_WDQLVL_VREF_DELTA_F1	DDR_PI_OFS	12A	[3:0]	0
PI_WDQLVL_EN_F1	DDR_PI_OFS	12A	[9:8]	3
PI_NTP_TRAIN_EN_F1	DDR_PI_OFS	12A	[19:16]	1
PI_NORMAL_CL_F1	DDR_PI_OFS	12A	[28:24]	00
PI_WDQLVL_RDLAT_ADJ_F1	DDR_PI_OFS	12B	[8:0]	008
PI_WDQLVL_WRLAT_ADJ_F1	DDR_PI_OFS	12B	[24:16]	008
PI_WDQLVL_TWCKENL_RD_ADJ_F1	DDR_PI_OFS	12C	[5:0]	00
PI_TDFI_WDQLVL_WR_F2	DDR_PI_OFS	12C	[17:8]	03D
PI_TDFI_WDQLVL_RW_F2	DDR_PI_OFS	12D	[9:0]	04C
PI_WDQLVL_VREF_INITIAL_START_POINT_F2	DDR_PI_OFS	12D	[22:16]	0E
PI_WDQLVL_VREF_INITIAL_STOP_POINT_F2	DDR_PI_OFS	12D	[30:24]	22
PI_WDQLVL_VREF_DELTA_F2	DDR_PI_OFS	12E	[3:0]	0
PI_WDQLVL_EN_F2	DDR_PI_OFS	12E	[9:8]	3
PI_NTP_TRAIN_EN_F2	DDR_PI_OFS	12E	[19:16]	1
PI_NORMAL_CL_F2	DDR_PI_OFS	12E	[28:24]	00
PI_WDQLVL_RDLAT_ADJ_F2	DDR_PI_OFS	12F	[8:0]	015
PI_WDQLVL_WRLAT_ADJ_F2	DDR_PI_OFS	12F	[24:16]	00E
PI_WDQLVL_TWCKENL_RD_ADJ_F2	DDR_PI_OFS	130	[5:0]	00
PI_RDLVL_ADVANCED_EN_F0	DDR_PI_OFS	130	[9:8]	0
PI_RDLVL_ADVANCED_EN_F1	DDR_PI_OFS	130	[17:16]	0
PI_RDLVL_ADVANCED_EN_F2	DDR_PI_OFS	130	[25:24]	0
PI_RDLVL_CS_ADV	DDR_PI_OFS	131	[1:0]	3
PI_WDQLVL_ADVANCED_EN_F0	DDR_PI_OFS	131	[9:8]	0
PI_WDQLVL_ADVANCED_EN_F1	DDR_PI_OFS	131	[17:16]	0
PI_WDQLVL_ADVANCED_EN_F2	DDR_PI_OFS	131	[25:24]	0
PI_TRTP_F0	DDR_PI_OFS	132	[7:0]	08
PI_TRP_F0	DDR_PI_OFS	132	[15:8]	04
PI_TRCD_F0	DDR_PI_OFS	132	[23:16]	04
PI_TCCD_L_F0	DDR_PI_OFS	132	[28:24]	00
PI_TWTR_S_F0	DDR_PI_OFS	133	[5:0]	09
PI_TWTR_L_F0	DDR_PI_OFS	133	[13:8]	09
PI_TCCD_S_F0	DDR_PI_OFS	133	[20:16]	00
PI_TWTR_F0	DDR_PI_OFS	133	[29:24]	09
PI_TWR_F0	DDR_PI_OFS	134	[7:0]	04
PI_TRAS_MAX_F0	DDR_PI_OFS	134	[23:8]	06C9
PI_TRAS_MIN_F0	DDR_PI_OFS	135	[8:0]	003
PI_TDQSCK_MAX_F0	DDR_PI_OFS	135	[19:16]	1
PI_TCCDMW_F0	DDR_PI_OFS	135	[29:24]	20
PI_TSR_F0	DDR_PI_OFS	136	[7:0]	03
PI_TMRD_F0	DDR_PI_OFS	136	[15:8]	0A
PI_TMRW_F0	DDR_PI_OFS	136	[23:16]	0A

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Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PI_TRTP_F1	DDR_PI_OFS	136	[31:24]	08
PI_TRP_F1	DDR_PI_OFS	137	[7:0]	11
PI_TRCD_F1	DDR_PI_OFS	137	[15:8]	0F
PI_TCCD_L_F1	DDR_PI_OFS	137	[20:16]	00
PI_TWTR_S_F1	DDR_PI_OFS	137	[29:24]	09
PI_TWTR_L_F1	DDR_PI_OFS	138	[5:0]	09
PI_TCCD_S_F1	DDR_PI_OFS	138	[12:8]	00
PI_TWTR_F1	DDR_PI_OFS	138	[21:16]	09
PI_TWR_F1	DDR_PI_OFS	138	[31:24]	10
PI_TRAS_MAX_F1	DDR_PI_OFS	139	[15:0]	62B8
PI_TRAS_MIN_F1	DDR_PI_OFS	139	[24:16]	022
PI_TDQSCK_MAX_F1	DDR_PI_OFS	13A	[3:0]	3
PI_TCCDMW_F1	DDR_PI_OFS	13A	[13:8]	20
PI_TSR_F1	DDR_PI_OFS	13A	[23:16]	0C
PI_TMRD_F1	DDR_PI_OFS	13A	[31:24]	0C
PI_TMRW_F1	DDR_PI_OFS	13B	[7:0]	0A
PI_TRTP_F2	DDR_PI_OFS	13B	[15:8]	10
PI_TRP_F2	DDR_PI_OFS	13B	[23:16]	2D
PI_TRCD_F2	DDR_PI_OFS	13B	[31:24]	27
PI_TCCD_L_F2	DDR_PI_OFS	13C	[4:0]	00
PI_TWTR_S_F2	DDR_PI_OFS	13C	[13:8]	17
PI_TWTR_L_F2	DDR_PI_OFS	13C	[21:16]	17
PI_TCCD_S_F2	DDR_PI_OFS	13C	[28:24]	00
PI_TWTR_F2	DDR_PI_OFS	13D	[5:0]	17
PI_TWR_F2	DDR_PI_OFS	13D	[15:8]	28
PI_TRAS_MAX_F2	DDR_PI_OFS	13D	[31:16]	752F
PI_TRAS_MIN_F2	DDR_PI_OFS	13E	[8:0]	05A
PI_TDQSCK_MAX_F2	DDR_PI_OFS	13E	[19:16]	8
PI_TCCDMW_F2	DDR_PI_OFS	13E	[29:24]	20
PI_TSR_F2	DDR_PI_OFS	13F	[7:0]	20
PI_TMRD_F2	DDR_PI_OFS	13F	[15:8]	1E
PI_TMRW_F2	DDR_PI_OFS	13F	[23:16]	16
PI_TDFI_CTRLUPD_MAX_F0	DDR_PI_OFS	140	[20:0]	00019E
PI_TDFI_CTRLUPD_INTERVAL_F0	DDR_PI_OFS	141	[31:0]	0000102C
PI_TDFI_CTRLUPD_MAX_F1	DDR_PI_OFS	142	[20:0]	00185C
PI_TDFI_CTRLUPD_INTERVAL_F1	DDR_PI_OFS	143	[31:0]	0000F398
PI_TDFI_CTRLUPD_MAX_F2	DDR_PI_OFS	144	[20:0]	004104
PI_TDFI_CTRLUPD_INTERVAL_F2	DDR_PI_OFS	145	[31:0]	00028A28
PI_TXSR_F0	DDR_PI_OFS	146	[15:0]	0016
PI_TXSR_F1	DDR_PI_OFS	146	[31:16]	0136
PI_TXSR_F2	DDR_PI_OFS	147	[15:0]	033B
PI_TEXCKE_F0	DDR_PI_OFS	147	[21:16]	03
PI_TEXCKE_F1	DDR_PI_OFS	147	[29:24]	03
PI_TEXCKE_F2	DDR_PI_OFS	148	[5:0]	04

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Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PI_TINIT_F0	DDR_PI_OFS	148	[31:8]	002AF8
PI_TINIT1_F0	DDR_PI_OFS	149	[23:0]	000000
PI_TINIT3_F0	DDR_PI_OFS	14A	[23:0]	006B6B
PI_TINIT4_F0	DDR_PI_OFS	14B	[23:0]	000005
PI_TINIT5_F0	DDR_PI_OFS	14C	[23:0]	00006E
PI_TXSNR_F0	DDR_PI_OFS	14D	[15:0]	0016
PI_TINIT_F1	DDR_PI_OFS	14E	[23:0]	027100
PI_TINIT1_F1	DDR_PI_OFS	14F	[23:0]	000000
PI_TINIT3_F1	DDR_PI_OFS	150	[23:0]	01ADAF
PI_TINIT4_F1	DDR_PI_OFS	151	[23:0]	000005
PI_TINIT5_F1	DDR_PI_OFS	152	[23:0]	000640
PI_TXSNR_F1	DDR_PI_OFS	153	[15:0]	0136
PI_TINIT_F2	DDR_PI_OFS	154	[23:0]	0681C8
PI_TINIT1_F2	DDR_PI_OFS	155	[23:0]	000000
PI_TINIT3_F2	DDR_PI_OFS	156	[23:0]	01ADAF
PI_TINIT4_F2	DDR_PI_OFS	157	[23:0]	000005
PI_TINIT5_F2	DDR_PI_OFS	158	[23:0]	0010A9
PI_TXSNR_F2	DDR_PI_OFS	159	[15:0]	033B
PI_TZQCAL_F0	DDR_PI_OFS	15A	[27:16]	037
PI_TZQLAT_F0	DDR_PI_OFS	15B	[6:0]	02
PI_TZQCAL_F1	DDR_PI_OFS	15C	[27:16]	320
PI_TZQLAT_F1	DDR_PI_OFS	15D	[6:0]	18
PI_TZQCAL_F2	DDR_PI_OFS	15E	[27:16]	855
PI_TZQLAT_F2	DDR_PI_OFS	15F	[6:0]	40
PI_ZQRESET_F0	DDR_PI_OFS	15F	[19:8]	003
PI_ZQRESET_F1	DDR_PI_OFS	160	[11:0]	028
PI_ZQRESET_F2	DDR_PI_OFS	160	[27:16]	06B
PI_WDQ_OSC_DELTA_INDEX_F0	DDR_PI_OFS	161	[3:0]	4
PI_WDQ_OSC_DELTA_INDEX_F1	DDR_PI_OFS	161	[11:8]	4
PI_WDQ_OSC_DELTA_INDEX_F2	DDR_PI_OFS	161	[19:16]	4
PI_TWCK2DQ7H_F0	DDR_PI_OFS	161	[28:24]	05
PI_TDQ7HWCK_F0	DDR_PI_OFS	162	[4:0]	03
PI_TDQ7LWCK_F0	DDR_PI_OFS	162	[12:8]	06
PI_TDQ72DQ_F0	DDR_PI_OFS	162	[25:16]	00E
PI_TCBTRTW_F0	DDR_PI_OFS	163	[5:0]	03
PI_TWCK2DQ7H_F1	DDR_PI_OFS	163	[12:8]	06
PI_TDQ7HWCK_F1	DDR_PI_OFS	163	[20:16]	04
PI_TDQ7LWCK_F1	DDR_PI_OFS	163	[28:24]	07
PI_TDQ72DQ_F1	DDR_PI_OFS	164	[9:0]	0C8
PI_TCBTRTW_F1	DDR_PI_OFS	164	[21:16]	10
PI_TWCK2DQ7H_F2	DDR_PI_OFS	164	[28:24]	0D
PI_TDQ7HWCK_F2	DDR_PI_OFS	165	[4:0]	0B
PI_TDQ7LWCK_F2	DDR_PI_OFS	165	[12:8]	0E
PI_TDQ72DQ_F2	DDR_PI_OFS	165	[25:16]	216

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Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PI_TCBTRTW_F2	DDR_PI_OFS	166	[5:0]	2B
PI_TDS_TRAIN_F0	DDR_PI_OFS	166	[11:8]	6
PI_TDH_TRAIN_F0	DDR_PI_OFS	166	[19:16]	4
PI_TDS_TRAIN_F1	DDR_PI_OFS	166	[27:24]	6
PI_TDH_TRAIN_F1	DDR_PI_OFS	167	[3:0]	4
PI_TDS_TRAIN_F2	DDR_PI_OFS	167	[11:8]	6
PI_TDH_TRAIN_F2	DDR_PI_OFS	167	[19:16]	4
PI_MC_TRFC_F0	DDR_PI_OFS	168	[9:0]	017
PI_MC_TRFC_F1	DDR_PI_OFS	168	[25:16]	132
PI_MC_TRFC_F2	DDR_PI_OFS	169	[9:0]	32D
PI_PHYMSTR_REQ_EXTEND_NUM_F0	DDR_PI_OFS	169	[19:16]	5
PI_REQ_EXTEND_MASK_CMD_EN_F0	DDR_PI_OFS	169	[24]	1
PI_PHYMSTR_REQ_EXTEND_NUM_F1	DDR_PI_OFS	16A	[3:0]	5
PI_REQ_EXTEND_MASK_CMD_EN_F1	DDR_PI_OFS	16A	[8]	1
PI_PHYMSTR_REQ_EXTEND_NUM_F2	DDR_PI_OFS	16A	[19:16]	5
PI_REQ_EXTEND_MASK_CMD_EN_F2	DDR_PI_OFS	16A	[24]	1
PI_CONTROL_CLEAR_LVL_REQ_DISABLE	DDR_PI_OFS	16B	[0]	0
PI_MC_DATA_FREQ_RATIO_F0	DDR_PI_OFS	16B	[9:8]	1
PI_MC_DATA_FREQ_RATIO_F1	DDR_PI_OFS	16B	[17:16]	1
PI_MC_DATA_FREQ_RATIO_F2	DDR_PI_OFS	16B	[25:24]	1
PI_PREAMBLE_SUPPORT_F0	DDR_PI_OFS	16C	[1:0]	3
PI_PREAMBLE_SUPPORT_F1	DDR_PI_OFS	16C	[9:8]	3
PI_PREAMBLE_SUPPORT_F2	DDR_PI_OFS	16C	[17:16]	3
PI_TMRR_F0	DDR_PI_OFS	16C	[27:24]	8
PI_TMRR_F1	DDR_PI_OFS	16D	[3:0]	8
PI_TMRR_F2	DDR_PI_OFS	16D	[11:8]	8
PI_TCASOFF_F0	DDR_PI_OFS	16D	[23:16]	01
PI_TDFI_WCK_STOP_F0	DDR_PI_OFS	16D	[31:24]	05
PI_TCASOFF_F1	DDR_PI_OFS	16E	[7:0]	01
PI_TDFI_WCK_STOP_F1	DDR_PI_OFS	16E	[15:8]	05
PI_TCASOFF_F2	DDR_PI_OFS	16E	[23:16]	01
PI_TDFI_WCK_STOP_F2	DDR_PI_OFS	16E	[31:24]	05
PI_LOW_FREQ_MARK_F0	DDR_PI_OFS	16F	[0]	1
PI_LOW_FREQ_MARK_F1	DDR_PI_OFS	16F	[8]	0
PI_LOW_FREQ_MARK_F2	DDR_PI_OFS	16F	[16]	0
PI_CKE_MUX_0	DDR_PI_OFS	16F	[25:24]	2
PI_CKE_MUX_1	DDR_PI_OFS	170	[1:0]	3
PI_CS_MUX_0	DDR_PI_OFS	170	[9:8]	0
PI_CS_MUX_1	DDR_PI_OFS	170	[17:16]	1
PI_MRSINGLE_DATA_0	DDR_PI_OFS	170	[31:24]	00
PI_MRSINGLE_DATA_1	DDR_PI_OFS	171	[7:0]	00
PI_ZQ_CAL_START_MAP_0	DDR_PI_OFS	171	[9:8]	1
PI_ZQ_CAL_LATCH_MAP_0	DDR_PI_OFS	171	[17:16]	1
PI_ZQ_CAL_START_MAP_1	DDR_PI_OFS	171	[25:24]	2

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Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PI_ZQ_CAL_LATCH_MAP_1	DDR_PI_OFS	172	[1:0]	2
PI_DQS_OSC_BASE_VALUE_0_0	DDR_PI_OFS	172	[23:8]	0000
PI_DQS_OSC_BASE_VALUE_1_0	DDR_PI_OFS	173	[15:0]	0000
PI_DQS_OSC_BASE_VALUE_0_1	DDR_PI_OFS	173	[31:16]	0000
PI_DQS_OSC_BASE_VALUE_1_1	DDR_PI_OFS	174	[15:0]	0000
PI_CALVL_SEQUENCER_EN	DDR_PI_OFS	174	[22:16]	7F
PI_POWER_ON_SEQ_MODE	DDR_PI_OFS	174	[25:24]	1
PI_CALVL_SEQ_MODE	DDR_PI_OFS	175	[1:0]	1
PI_WRLVL_SEQ_MODE	DDR_PI_OFS	175	[9:8]	1
PI_GTLVL_SEQ_MODE	DDR_PI_OFS	175	[17:16]	1
PI_RDLVL_SEQ_MODE	DDR_PI_OFS	175	[25:24]	1
PI_WDQLVL_SEQ_MODE	DDR_PI_OFS	176	[1:0]	1
PI_SEQ_PAUSE	DDR_PI_OFS	177	[31:0]	00000000
PI_SEQ_PAUSE_1	DDR_PI_OFS	178	[9:0]	000
PI_SEQ_CS	DDR_PI_OFS	178	[17:16]	0
PI_INIT_SEQ_MR_FREQ_SEL	DDR_PI_OFS	178	[28:24]	00
PI_SEQ_PAUSE_CONT	DDR_PI_OFS	179	[0]	0
PI_SEQ_DEC_SW_REQ	DDR_PI_OFS	179	[8]	0
PI_SEQ_DEC_SW_DATA	DDR_PI_OFS	17A	[26:0]	0000000
PI_SEQ_DEC_SW_CS	DDR_PI_OFS	17B	[1:0]	0
PI_SEQ_DEC_SW_DONE	DDR_PI_OFS	17B	[8]	0
PI_SW_SEQ_START	DDR_PI_OFS	17B	[16]	0
PI_DFS_ENTRY_SEQ_EN	DDR_PI_OFS	17B	[24]	1
PI_DFS_INITIALIZATION_SEQ_EN	DDR_PI_OFS	17C	[0]	1
PI_POWER_ON_SEQ_DFS_SEQ_EN	DDR_PI_OFS	17C	[8]	1
PI_DFS_INITIALIZATION_SEQ_AREF_EN	DDR_PI_OFS	17C	[16]	0
PI_DFS_INITIALIZATION_SEQ_NORMAL_LVL_EN	DDR_PI_OFS	17C	[24]	1
PI_DFS_SEQ_PRE_TIME_F0	DDR_PI_OFS	17D	[3:0]	0
PI_DFS_SEQ_PRE_TIME_F1	DDR_PI_OFS	17D	[11:8]	0
PI_DFS_SEQ_PRE_TIME_F2	DDR_PI_OFS	17D	[19:16]	0
PI_DFS_SEQ_POST_TIME_F0	DDR_PI_OFS	17D	[27:24]	0
PI_DFS_SEQ_POST_TIME_F1	DDR_PI_OFS	17E	[3:0]	0
PI_DFS_SEQ_POST_TIME_F2	DDR_PI_OFS	17E	[11:8]	0
PI_DFS_SEQ_MASK_PHYUPD	DDR_PI_OFS	17E	[16]	0
PI_WDQLVL_TRAIN_SEQ_0	DDR_PI_OFS	17F	[30:0]	08203020
PI_WDQLVL_TRAIN_SEQ_1	DDR_PI_OFS	180	[30:0]	28100020
PI_WDQLVL_TRAIN_SEQ_2	DDR_PI_OFS	181	[30:0]	08083020
PI_WDQLVL_TRAIN_SEQ_3	DDR_PI_OFS	182	[30:0]	08400020
PI_WDQLVL_TRAIN_SEQ_4	DDR_PI_OFS	183	[30:0]	08402020
PI_WDQLVL_TRAIN_SEQ_5	DDR_PI_OFS	184	[30:0]	08483020
PI_WDQLVL_TRAIN_SEQ_6	DDR_PI_OFS	185	[30:0]	10083020
PI_WDQLVL_TRAIN_SEQ_7	DDR_PI_OFS	186	[30:0]	20180020
PI_WDQLVL_TRAIN_SEQ_8	DDR_PI_OFS	187	[30:0]	30480020
PI_WDQLVL_TRAIN_SEQ_9	DDR_PI_OFS	188	[30:0]	78880020

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Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PI_WDQLVL_TRAIN_SEQ_10	DDR_PI_OFS	189	[30:0]	488010E0
PI_WDQLVL_TRAIN_SEQ_11	DDR_PI_OFS	18A	[30:0]	494B0000
PI_WDQLVL_TRAIN_SEQ_12	DDR_PI_OFS	18B	[30:0]	49080000
PI_WDQLVL_TRAIN_SEQ_13	DDR_PI_OFS	18C	[30:0]	490011C0
PI_WDQLVL_TRAIN_SEQ_14	DDR_PI_OFS	18D	[30:0]	0A000020
PI_WDQLVL_TRAIN_SEQ_15	DDR_PI_OFS	18E	[30:0]	08000020
PI_WDQLVL_TRAIN_SEQ_16	DDR_PI_OFS	18F	[30:0]	08000020
PI_WDQLVL_TRAIN_SEQ_17	DDR_PI_OFS	190	[30:0]	08000020
PI_WDQLVL_TRAIN_SEQ_18	DDR_PI_OFS	191	[30:0]	08000020
PI_WDQLVL_TRAIN_SEQ_19	DDR_PI_OFS	192	[30:0]	08000020
PI_WDQLVL_TRAIN_SEQ_20	DDR_PI_OFS	193	[30:0]	08000020
PI_WDQLVL_TRAIN_SEQ_21	DDR_PI_OFS	194	[30:0]	08000020
PI_WDQLVL_TRAIN_SEQ_22	DDR_PI_OFS	195	[30:0]	08000020
PI_WDQLVL_TRAIN_SEQ_23	DDR_PI_OFS	196	[30:0]	08000020
PI_WDQLVL_TRAIN_SEQ_24	DDR_PI_OFS	197	[30:0]	08000020
PI_WDQLVL_TRAIN_SEQ_25	DDR_PI_OFS	198	[30:0]	08000020
PI_WDQLVL_TRAIN_SEQ_26	DDR_PI_OFS	199	[30:0]	08000020
PI_WDQLVL_TRAIN_SEQ_27	DDR_PI_OFS	19A	[30:0]	08000020
PI_WDQLVL_TRAIN_SEQ_28	DDR_PI_OFS	19B	[30:0]	08000020
PI_WDQLVL_TRAIN_SEQ_29	DDR_PI_OFS	19C	[30:0]	08000020
PI_WDQLVL_TRAIN_SEQ_30	DDR_PI_OFS	19D	[30:0]	08000020
PI_WDQLVL_TRAIN_SEQ_31	DDR_PI_OFS	19E	[30:0]	08000020
PI_WDQLVL_TRAIN_SEQ_32	DDR_PI_OFS	19F	[30:0]	08000020
PI_WDQLVL_TRAIN_SEQ_33	DDR_PI_OFS	1A0	[30:0]	08000020
PI_WDQLVL_TRAIN_SEQ_34	DDR_PI_OFS	1A1	[30:0]	08000020
PI_WDQLVL_TRAIN_SEQ_35	DDR_PI_OFS	1A2	[30:0]	08000020
PI_WDQLVL_TRAIN_SEQ_36	DDR_PI_OFS	1A3	[30:0]	08000020
PI_WDQLVL_TRAIN_SEQ_37	DDR_PI_OFS	1A4	[30:0]	08000020
PI_WDQLVL_TRAIN_SEQ_38	DDR_PI_OFS	1A5	[30:0]	08000020
PI_WDQLVL_TRAIN_SEQ_39	DDR_PI_OFS	1A6	[30:0]	08000020
PI_WDQLVL_TRAIN_SEQ_40	DDR_PI_OFS	1A7	[30:0]	08000020
PI_WDQLVL_TRAIN_SEQ_41	DDR_PI_OFS	1A8	[30:0]	08000020
PI_WDQLVL_TRAIN_SEQ_42	DDR_PI_OFS	1A9	[30:0]	08000020
PI_WDQLVL_TRAIN_SEQ_43	DDR_PI_OFS	1AA	[30:0]	08000020
PI_WDQLVL_TRAIN_SEQ_44	DDR_PI_OFS	1AB	[30:0]	08000020
PI_SEQ_ARRAY_0	DDR_PI_OFS	1AC	[30:0]	08084340
PI_SEQ_ARRAY_1	DDR_PI_OFS	1AD	[30:0]	001F0000
PI_SEQ_ARRAY_2	DDR_PI_OFS	1AE	[30:0]	001F0000
PI_SEQ_ARRAY_3	DDR_PI_OFS	1AF	[30:0]	001F0000
PI_SEQ_ARRAY_4	DDR_PI_OFS	1B0	[30:0]	001F0000
PI_SEQ_ARRAY_5	DDR_PI_OFS	1B1	[30:0]	001F0000
PI_SEQ_ARRAY_6	DDR_PI_OFS	1B2	[30:0]	001F0000
PI_SEQ_ARRAY_7	DDR_PI_OFS	1B3	[30:0]	081E4340
PI_SEQ_ARRAY_8	DDR_PI_OFS	1B4	[30:0]	003F0000

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Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PI_SEQ_ARRAY_9	DDR_PI_OFS	1B5	[30:0]	003F0000
PI_SEQ_ARRAY_10	DDR_PI_OFS	1B6	[30:0]	003F0000
PI_SEQ_ARRAY_11	DDR_PI_OFS	1B7	[30:0]	081A5047
PI_SEQ_ARRAY_12	DDR_PI_OFS	1B8	[30:0]	001A10FF
PI_SEQ_ARRAY_13	DDR_PI_OFS	1B9	[30:0]	00051A00
PI_SEQ_ARRAY_14	DDR_PI_OFS	1BA	[30:0]	001A11FF
PI_SEQ_ARRAY_15	DDR_PI_OFS	1BB	[30:0]	00051B00
PI_SEQ_ARRAY_16	DDR_PI_OFS	1BC	[30:0]	001F13FF
PI_SEQ_ARRAY_17	DDR_PI_OFS	1BD	[28:0]	081A5047
PI_SEQ_ARRAY_18	DDR_PI_OFS	1BE	[28:0]	001A10FF
PI_SEQ_ARRAY_19	DDR_PI_OFS	1BF	[28:0]	00051A00
PI_SEQ_ARRAY_20	DDR_PI_OFS	1C0	[28:0]	001A11FF
PI_SEQ_ARRAY_21	DDR_PI_OFS	1C1	[28:0]	00051B00
PI_SEQ_ARRAY_22	DDR_PI_OFS	1C2	[28:0]	001F13FF
PI_SEQ_ARRAY_23	DDR_PI_OFS	1C3	[28:0]	081A5047
PI_SEQ_ARRAY_24	DDR_PI_OFS	1C4	[28:0]	001A10FF
PI_SEQ_ARRAY_25	DDR_PI_OFS	1C5	[28:0]	00051A00
PI_SEQ_ARRAY_26	DDR_PI_OFS	1C6	[28:0]	001A11FF
PI_SEQ_ARRAY_27	DDR_PI_OFS	1C7	[28:0]	00051B00
PI_SEQ_ARRAY_28	DDR_PI_OFS	1C8	[28:0]	001F13FF
PI_SEQ_ARRAY_29	DDR_PI_OFS	1C9	[28:0]	11910048
PI_SEQ_ARRAY_30	DDR_PI_OFS	1CA	[28:0]	09911000
PI_SEQ_ARRAY_31	DDR_PI_OFS	1CB	[28:0]	19A20D06
PI_SEQ_ARRAY_32	DDR_PI_OFS	1CC	[28:0]	19A10100
PI_SEQ_ARRAY_33	DDR_PI_OFS	1CD	[28:0]	19A10201
PI_SEQ_ARRAY_34	DDR_PI_OFS	1CE	[28:0]	19A10302
PI_SEQ_ARRAY_35	DDR_PI_OFS	1CF	[28:0]	19A10B04
PI_SEQ_ARRAY_36	DDR_PI_OFS	1D0	[28:0]	19A1160E
PI_SEQ_ARRAY_37	DDR_PI_OFS	1D1	[28:0]	181108F7
PI_SEQ_ARRAY_38	DDR_PI_OFS	1D2	[28:0]	19A10D06
PI_SEQ_ARRAY_39	DDR_PI_OFS	1D3	[28:0]	18051900
PI_SEQ_ARRAY_40	DDR_PI_OFS	1D4	[28:0]	1800803F
PI_SEQ_ARRAY_41	DDR_PI_OFS	1D5	[28:0]	19A01F1A
PI_SEQ_ARRAY_42	DDR_PI_OFS	1D6	[28:0]	19A10C05
PI_SEQ_ARRAY_43	DDR_PI_OFS	1D7	[28:0]	10051F00
PI_SEQ_ARRAY_44	DDR_PI_OFS	1D8	[28:0]	19A10E07
PI_SEQ_ARRAY_45	DDR_PI_OFS	1D9	[28:0]	10051F00
PI_SEQ_ARRAY_46	DDR_PI_OFS	1DA	[28:0]	1800403F
PI_SEQ_ARRAY_47	DDR_PI_OFS	1DB	[28:0]	19A01F1A
PI_SEQ_ARRAY_48	DDR_PI_OFS	1DC	[28:0]	19A00C00
PI_SEQ_ARRAY_49	DDR_PI_OFS	1DD	[28:0]	10001F00
PI_SEQ_ARRAY_50	DDR_PI_OFS	1DE	[28:0]	19A00E00
PI_SEQ_ARRAY_51	DDR_PI_OFS	1DF	[28:0]	10001F00
PI_SEQ_ARRAY_52	DDR_PI_OFS	1E0	[28:0]	19910280

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Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PI_SEQ_ARRAY_53	DDR_PI_OFS	1E1	[28:0]	19A20D06
PI_SEQ_ARRAY_54	DDR_PI_OFS	1E2	[28:0]	18051000
PI_SEQ_ARRAY_55	DDR_PI_OFS	1E3	[28:0]	18861101
PI_SEQ_ARRAY_56	DDR_PI_OFS	1E4	[28:0]	181F0000
PI_SEQ_ARRAY_57	DDR_PI_OFS	1E5	[28:0]	181F0000
PI_SEQ_ARRAY_58	DDR_PI_OFS	1E6	[28:0]	181F0000
PI_SEQ_ARRAY_59	DDR_PI_OFS	1E7	[28:0]	181F0000
PI_SEQ_ARRAY_60	DDR_PI_OFS	1E8	[28:0]	181F0000
PI_SEQ_ARRAY_61	DDR_PI_OFS	1E9	[28:0]	181F0000
PI_SEQ_ARRAY_62	DDR_PI_OFS	1EA	[28:0]	181F0000
PI_SEQ_ARRAY_63	DDR_PI_OFS	1EB	[28:0]	18861100
PI_SEQ_ARRAY_64	DDR_PI_OFS	1EC	[28:0]	19A10D06
PI_SEQ_ARRAY_65	DDR_PI_OFS	1ED	[28:0]	18051800
PI_SEQ_ARRAY_66	DDR_PI_OFS	1EE	[28:0]	101B0001
PI_SEQ_ARRAY_67	DDR_PI_OFS	1EF	[28:0]	181B0100
PI_SEQ_ARRAY_68	DDR_PI_OFS	1F0	[28:0]	181B0200
PI_SEQ_ARRAY_69	DDR_PI_OFS	1F1	[28:0]	181B0300
PI_SEQ_ARRAY_70	DDR_PI_OFS	1F2	[28:0]	181B0400
PI_SEQ_ARRAY_71	DDR_PI_OFS	1F3	[28:0]	1C440316
PI_SEQ_ARRAY_72	DDR_PI_OFS	1F4	[28:0]	100D0000
PI_SEQ_ARRAY_73	DDR_PI_OFS	1F5	[28:0]	101C0000
PI_SEQ_ARRAY_74	DDR_PI_OFS	1F6	[28:0]	181F0000
PI_SEQ_ARRAY_75	DDR_PI_OFS	1F7	[28:0]	181F0000
PI_SEQ_ARRAY_76	DDR_PI_OFS	1F8	[28:0]	181F0000
PI_SEQ_ARRAY_77	DDR_PI_OFS	1F9	[28:0]	181F0000
PI_SEQ_ARRAY_78	DDR_PI_OFS	1FA	[28:0]	181F0000
PI_SEQ_ARRAY_79	DDR_PI_OFS	1FB	[28:0]	181F0000
PI_SEQ_ARRAY_80	DDR_PI_OFS	1FC	[28:0]	181F0000
PI_SEQ_ARRAY_81	DDR_PI_OFS	1FD	[28:0]	181F0000
PI_SEQ_ARRAY_82	DDR_PI_OFS	1FE	[28:0]	181F0000
PI_SEQ_ARRAY_83	DDR_PI_OFS	1FF	[28:0]	181F0000
PI_SEQ_ARRAY_84	DDR_PI_OFS	200	[28:0]	181F0000
PI_SEQ_ARRAY_85	DDR_PI_OFS	201	[28:0]	181F0000
PI_SEQ_ARRAY_86	DDR_PI_OFS	202	[28:0]	181F0000
PI_SEQ_ARRAY_87	DDR_PI_OFS	203	[28:0]	181F0000
PI_SEQ_ARRAY_88	DDR_PI_OFS	204	[28:0]	181F0000
PI_SEQ_ARRAY_89	DDR_PI_OFS	205	[28:0]	09910260
PI_SEQ_ARRAY_90	DDR_PI_OFS	206	[28:0]	11911600
PI_SEQ_ARRAY_91	DDR_PI_OFS	207	[28:0]	19A20D06
PI_SEQ_ARRAY_92	DDR_PI_OFS	208	[28:0]	18051900
PI_SEQ_ARRAY_93	DDR_PI_OFS	209	[28:0]	19A10100
PI_SEQ_ARRAY_94	DDR_PI_OFS	20A	[28:0]	19A10201
PI_SEQ_ARRAY_95	DDR_PI_OFS	20B	[28:0]	19A10302
PI_SEQ_ARRAY_96	DDR_PI_OFS	20C	[28:0]	19A10B04

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Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PI_SEQ_ARRAY_97	DDR_PI_OFS	20D	[28:0]	1800803F
PI_SEQ_ARRAY_98	DDR_PI_OFS	20E	[28:0]	19A01F1A
PI_SEQ_ARRAY_99	DDR_PI_OFS	20F	[28:0]	19A10C05
PI_SEQ_ARRAY_100	DDR_PI_OFS	210	[28:0]	19A10E07
PI_SEQ_ARRAY_101	DDR_PI_OFS	211	[28:0]	1800403F
PI_SEQ_ARRAY_102	DDR_PI_OFS	212	[28:0]	19A01F1A
PI_SEQ_ARRAY_103	DDR_PI_OFS	213	[28:0]	19A00C00
PI_SEQ_ARRAY_104	DDR_PI_OFS	214	[28:0]	19A00E00
PI_SEQ_ARRAY_105	DDR_PI_OFS	215	[28:0]	19A1160E
PI_SEQ_ARRAY_106	DDR_PI_OFS	216	[28:0]	09A30012
PI_SEQ_ARRAY_107	DDR_PI_OFS	217	[28:0]	199F0000
PI_SEQ_ARRAY_108	DDR_PI_OFS	218	[28:0]	0011007F
PI_SEQ_ARRAY_109	DDR_PI_OFS	219	[28:0]	01810201
PI_SEQ_ARRAY_110	DDR_PI_OFS	21A	[28:0]	01800800
PI_SEQ_ARRAY_111	DDR_PI_OFS	21B	[28:0]	01A00D06
PI_SEQ_ARRAY_112	DDR_PI_OFS	21C	[28:0]	080D0000
PI_SEQ_ARRAY_113	DDR_PI_OFS	21D	[28:0]	001F0000
PI_SEQ_ARRAY_114	DDR_PI_OFS	21E	[28:0]	080C0000
PI_SEQ_ARRAY_115	DDR_PI_OFS	21F	[28:0]	01800440
PI_SEQ_ARRAY_116	DDR_PI_OFS	220	[28:0]	01A00D06
PI_SEQ_ARRAY_117	DDR_PI_OFS	221	[28:0]	0011FF7F
PI_SEQ_ARRAY_118	DDR_PI_OFS	222	[28:0]	01810201
PI_SEQ_ARRAY_119	DDR_PI_OFS	223	[28:0]	001F0000
PI_SEQ_ARRAY_120	DDR_PI_OFS	224	[28:0]	001F0200
PI_SEQ_ARRAY_121	DDR_PI_OFS	225	[28:0]	00050000
PI_SEQ_ARRAY_122	DDR_PI_OFS	226	[28:0]	00070100
PI_SEQ_ARRAY_123	DDR_PI_OFS	227	[28:0]	00060200
PI_SEQ_ARRAY_124	DDR_PI_OFS	228	[28:0]	00000000
PI_SEQ_ARRAY_125	DDR_PI_OFS	229	[28:0]	00000000
PI_SEQ_ARRAY_126	DDR_PI_OFS	22A	[28:0]	01A10201
PI_SEQ_ARRAY_127	DDR_PI_OFS	22B	[28:0]	01A10B04
PI_SEQ_ARRAY_128	DDR_PI_OFS	22C	[28:0]	01A1160E
PI_SEQ_ARRAY_129	DDR_PI_OFS	22D	[28:0]	01A10302
PI_SEQ_ARRAY_130	DDR_PI_OFS	22E	[28:0]	00090000
PI_SEQ_ARRAY_131	DDR_PI_OFS	22F	[28:0]	00098000
PI_SEQ_ARRAY_132	DDR_PI_OFS	230	[28:0]	019F0000
PI_SEQ_ARRAY_133	DDR_PI_OFS	231	[28:0]	019F0000
PI_SEQ_ARRAY_134	DDR_PI_OFS	232	[28:0]	01A10201
PI_SEQ_ARRAY_135	DDR_PI_OFS	233	[28:0]	01A10302
PI_SEQ_ARRAY_136	DDR_PI_OFS	234	[28:0]	01A10D06
PI_SEQ_ARRAY_137	DDR_PI_OFS	235	[28:0]	01A10100
PI_SEQ_ARRAY_138	DDR_PI_OFS	236	[28:0]	00000000
PI_SEQ_ARRAY_139	DDR_PI_OFS	237	[28:0]	00000000
PI_SEQ_ARRAY_140	DDR_PI_OFS	238	[28:0]	000A0808

		V4M		
Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PI_SEQ_ARRAY_141	DDR_PI_OFS	239	[28:0]	00058032
PI_SEQ_ARRAY_142	DDR_PI_OFS	23A	[28:0]	001F0000
PI_SEQ_ARRAY_143	DDR_PI_OFS	23B	[28:0]	001F0000
PI_SEQ_ARRAY_144	DDR_PI_OFS	23C	[28:0]	001F0000
PI_SEQ_ARRAY_145	DDR_PI_OFS	23D	[28:0]	001F0000
PI_SEQ_ARRAY_146	DDR_PI_OFS	23E	[28:0]	001F0000
PI_SEQ_ARRAY_147	DDR_PI_OFS	23F	[28:0]	001F0000
PI_SEQ_ARRAY_148	DDR_PI_OFS	240	[28:0]	001F0000
PI_SEQ_ARRAY_149	DDR_PI_OFS	241	[28:0]	001F0000
PI_SEQ_ARRAY_150	DDR_PI_OFS	242	[28:0]	000A0000
PI_SEQ_ARRAY_151	DDR_PI_OFS	243	[28:0]	00060000
PI_SEQ_ARRAY_152	DDR_PI_OFS	244	[28:0]	000D0000
PI_SEQ_ARRAY_153	DDR_PI_OFS	245	[28:0]	001C0000
PI_SEQ_ARRAY_154	DDR_PI_OFS	246	[26:0]	01F0000
PI_SEQ_ARRAY_155	DDR_PI_OFS	247	[26:0]	01F0000
PI_SEQ_ARRAY_156	DDR_PI_OFS	248	[26:0]	01F0000
PI_SEQ_ARRAY_157	DDR_PI_OFS	249	[26:0]	01F0000
PI_SEQ_ARRAY_158	DDR_PI_OFS	24A	[26:0]	01F0000
PI_SEQ_ARRAY_159	DDR_PI_OFS	24B	[26:0]	1910305
PI_SEQ_ARRAY_160	DDR_PI_OFS	24C	[26:0]	1A20D06
PI_SEQ_ARRAY_161	DDR_PI_OFS	24D	[26:0]	19F0000
PI_SEQ_ARRAY_162	DDR_PI_OFS	24E	[26:0]	011FFF7
PI_SEQ_ARRAY_163	DDR_PI_OFS	24F	[26:0]	1810D06
PI_SEQ_ARRAY_164	DDR_PI_OFS	250	[26:0]	0051900
PI_SEQ_ARRAY_165	DDR_PI_OFS	251	[26:0]	000803F
PI_SEQ_ARRAY_166	DDR_PI_OFS	252	[26:0]	1A01F1A
PI_SEQ_ARRAY_167	DDR_PI_OFS	253	[26:0]	1A10C05
PI_SEQ_ARRAY_168	DDR_PI_OFS	254	[26:0]	0051F00
PI_SEQ_ARRAY_169	DDR_PI_OFS	255	[26:0]	000403F
PI_SEQ_ARRAY_170	DDR_PI_OFS	256	[26:0]	1A01F1A
PI_SEQ_ARRAY_171	DDR_PI_OFS	257	[26:0]	1A00C00
PI_SEQ_ARRAY_172	DDR_PI_OFS	258	[26:0]	0001F00
PI_SEQ_ARRAY_173	DDR_PI_OFS	259	[26:0]	01100F7
PI_SEQ_ARRAY_174	DDR_PI_OFS	25A	[26:0]	1810D06
PI_SEQ_ARRAY_175	DDR_PI_OFS	25B	[26:0]	0051800
PI_SEQ_ARRAY_176	DDR_PI_OFS	25C	[26:0]	19F0000
PI_SEQ_ARRAY_177	DDR_PI_OFS	25D	[26:0]	1510001
PI_SEQ_ARRAY_178	DDR_PI_OFS	25E	[26:0]	1D102A0
PI_SEQ_ARRAY_179	DDR_PI_OFS	25F	[26:0]	1E20D06
PI_SEQ_ARRAY_180	DDR_PI_OFS	260	[26:0]	0051900
PI_SEQ_ARRAY_181	DDR_PI_OFS	261	[26:0]	19F0000
PI_SEQ_ARRAY_182	DDR_PI_OFS	262	[26:0]	1510001
PI_SEQ_ARRAY_183	DDR_PI_OFS	263	[26:0]	1D10290
PI_SEQ_ARRAY_184	DDR_PI_OFS	264	[26:0]	1E20D06

		V4M		
Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PI_SEQ_ARRAY_185	DDR_PI_OFS	265	[26:0]	0051900
PI_SEQ_ARRAY_186	DDR_PI_OFS	266	[26:0]	1510001
PI_SEQ_ARRAY_187	DDR_PI_OFS	267	[26:0]	1D10000
PI_SEQ_ARRAY_188	DDR_PI_OFS	268	[26:0]	1E20D06
PI_SEQ_ARRAY_189	DDR_PI_OFS	269	[26:0]	0051800
PI_SEQ_ARRAY_190	DDR_PI_OFS	26A	[26:0]	19F0000
PI_SEQ_ARRAY_191	DDR_PI_OFS	26B	[26:0]	01100F6
PI_SEQ_ARRAY_192	DDR_PI_OFS	26C	[26:0]	1810D06
PI_SEQ_ARRAY_193	DDR_PI_OFS	26D	[26:0]	0051800
PI_SEQ_ARRAY_194	DDR_PI_OFS	26E	[26:0]	1910000
PI_SEQ_ARRAY_195	DDR_PI_OFS	26F	[26:0]	1A20D06
PI_SEQ_ARRAY_196	DDR_PI_OFS	270	[26:0]	19F0000
PI_SEQ_ARRAY_197	DDR_PI_OFS	271	[26:0]	1911000
PI_SEQ_ARRAY_198	DDR_PI_OFS	272	[26:0]	1A20D06
PI_SEQ_ARRAY_199	DDR_PI_OFS	273	[26:0]	1A10100
PI_SEQ_ARRAY_200	DDR_PI_OFS	274	[26:0]	1A10201
PI_SEQ_ARRAY_201	DDR_PI_OFS	275	[26:0]	1A10302
PI_SEQ_ARRAY_202	DDR_PI_OFS	276	[26:0]	1A10B04
PI_SEQ_ARRAY_203	DDR_PI_OFS	277	[26:0]	000803F
PI_SEQ_ARRAY_204	DDR_PI_OFS	278	[26:0]	1A01F1A
PI_SEQ_ARRAY_205	DDR_PI_OFS	279	[26:0]	1A10C05
PI_SEQ_ARRAY_206	DDR_PI_OFS	27A	[26:0]	1A10E07
PI_SEQ_ARRAY_207	DDR_PI_OFS	27B	[26:0]	000403F
PI_SEQ_ARRAY_208	DDR_PI_OFS	27C	[26:0]	1A01F1A
PI_SEQ_ARRAY_209	DDR_PI_OFS	27D	[26:0]	1A00C00
PI_SEQ_ARRAY_210	DDR_PI_OFS	27E	[26:0]	1A00E00
PI_SEQ_ARRAY_211	DDR_PI_OFS	27F	[26:0]	1A1160E
PI_SEQ_ARRAY_212	DDR_PI_OFS	280	[26:0]	1910800
PI_SEQ_ARRAY_213	DDR_PI_OFS	281	[26:0]	1A20D06
PI_SEQ_ARRAY_214	DDR_PI_OFS	282	[26:0]	19F0000
PI_SEQ_ARRAY_215	DDR_PI_OFS	283	[26:0]	19F0000
PI_SEQ_ARRAY_216	DDR_PI_OFS	284	[26:0]	01F0000
PI_SEQ_ARRAY_217	DDR_PI_OFS	285	[26:0]	01F0000
PI_SEQ_ARRAY_218	DDR_PI_OFS	286	[26:0]	01F0000
PI_SEQ_ARRAY_219	DDR_PI_OFS	287	[26:0]	01F0000
PI_SEQ_ARRAY_220	DDR_PI_OFS	288	[26:0]	01F0200
PI_SEQ_ARRAY_221	DDR_PI_OFS	289	[26:0]	01102FD
PI_SEQ_ARRAY_222	DDR_PI_OFS	28A	[26:0]	1A10D06
PI_SEQ_ARRAY_223	DDR_PI_OFS	28B	[26:0]	01F0000
PI_SEQ_ARRAY_224	DDR_PI_OFS	28C	[26:0]	1A10D06
PI_SEQ_ARRAY_225	DDR_PI_OFS	28D	[26:0]	0051300
PI_SEQ_ARRAY_226	DDR_PI_OFS	28E	[26:0]	01F0000
PI_SEQ_ARRAY_227	DDR_PI_OFS	28F	[26:0]	01F0000
PI_SEQ_ARRAY_228	DDR_PI_OFS	290	[26:0]	01F0000

		V4M		
Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PI_SEQ_ARRAY_229	DDR_PI_OFS	291	[26:0]	01F0000
PI_SEQ_ARRAY_230	DDR_PI_OFS	292	[26:0]	0210F08
PI_SEQ_ARRAY_231	DDR_PI_OFS	293	[26:0]	021140D
PI_SEQ_ARRAY_232	DDR_PI_OFS	294	[26:0]	0212015
PI_SEQ_ARRAY_233	DDR_PI_OFS	295	[26:0]	0212818
PI_SEQ_ARRAY_234	DDR_PI_OFS	296	[26:0]	01F0000
PI_SEQ_ARRAY_235	DDR_PI_OFS	297	[26:0]	01F0000
PI_SEQ_ARRAY_236	DDR_PI_OFS	298	[26:0]	0210F08
PI_SEQ_ARRAY_237	DDR_PI_OFS	299	[26:0]	021140D
PI_SEQ_ARRAY_238	DDR_PI_OFS	29A	[26:0]	0212015
PI_SEQ_ARRAY_239	DDR_PI_OFS	29B	[26:0]	0212818
PI_SEQ_ARRAY_240	DDR_PI_OFS	29C	[26:0]	01F0000
PI_SEQ_ARRAY_241	DDR_PI_OFS	29D	[26:0]	01A84FF
PI_SEQ_ARRAY_242	DDR_PI_OFS	29E	[26:0]	01F0000
PI_SEQ_ARRAY_243	DDR_PI_OFS	29F	[26:0]	1800440
PI_SEQ_ARRAY_244	DDR_PI_OFS	2A0	[26:0]	1A00D06
PI_SEQ_ARRAY_245	DDR_PI_OFS	2A1	[26:0]	01F0000
PI_SEQ_ARRAY_246	DDR_PI_OFS	2A2	[26:0]	01F0000
PI_SEQ_ARRAY_247	DDR_PI_OFS	2A3	[26:0]	01F0000
PI_SEQ_ARRAY_248	DDR_PI_OFS	2A4	[26:0]	01F0000
PI_SEQ_ARRAY_249	DDR_PI_OFS	2A5	[26:0]	01F0000
PI_SEQ_ARRAY_250	DDR_PI_OFS	2A6	[26:0]	1800800
PI_SEQ_ARRAY_251	DDR_PI_OFS	2A7	[26:0]	1A00D06
PI_SEQ_ARRAY_252	DDR_PI_OFS	2A8	[26:0]	01F0000
PI_SEQ_ARRAY_253	DDR_PI_OFS	2A9	[26:0]	01F0000
PI_SEQ_ARRAY_254	DDR_PI_OFS	2AA	[26:0]	01F0000
PI_SEQ_ARRAY_255	DDR_PI_OFS	2AB	[26:0]	0031200
PI_SEQ_ARRAY_256	DDR_PI_OFS	2AC	[26:0]	0031300
PI_SEQ_ARRAY_257	DDR_PI_OFS	2AD	[26:0]	01F0000
PI_SEQ_ARRAY_258	DDR_PI_OFS	2AE	[26:0]	031FFF7
PI_SEQ_ARRAY_259	DDR_PI_OFS	2AF	[26:0]	1A10D06
PI_SEQ_ARRAY_260	DDR_PI_OFS	2B0	[26:0]	0051900
PI_SEQ_ARRAY_261	DDR_PI_OFS	2B1	[26:0]	000803F
PI_SEQ_ARRAY_262	DDR_PI_OFS	2B2	[26:0]	1A01F1A
PI_SEQ_ARRAY_263	DDR_PI_OFS	2B3	[26:0]	1A10E07
PI_SEQ_ARRAY_264	DDR_PI_OFS	2B4	[26:0]	0051F00
PI_SEQ_ARRAY_265	DDR_PI_OFS	2B5	[26:0]	000403F
PI_SEQ_ARRAY_266	DDR_PI_OFS	2B6	[26:0]	1A01F1A
PI_SEQ_ARRAY_267	DDR_PI_OFS	2B7	[26:0]	1A00E00
PI_SEQ_ARRAY_268	DDR_PI_OFS	2B8	[26:0]	0001F00
PI_SEQ_ARRAY_269	DDR_PI_OFS	2B9	[26:0]	03100F7
PI_SEQ_ARRAY_270	DDR_PI_OFS	2BA	[26:0]	1A10D06
PI_SEQ_ARRAY_271	DDR_PI_OFS	2BB	[26:0]	0051800
PI_SEQ_ARRAY_272	DDR_PI_OFS	2BC	[26:0]	03F0000

		V4M		
Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PI_SEQ_ARRAY_273	DDR_PI_OFS	2BD	[26:0]	031FFF7
PI_SEQ_ARRAY_274	DDR_PI_OFS	2BE	[26:0]	1A10D06
PI_SEQ_ARRAY_275	DDR_PI_OFS	2BF	[26:0]	0051900
PI_SEQ_ARRAY_276	DDR_PI_OFS	2C0	[26:0]	000803F
PI_SEQ_ARRAY_277	DDR_PI_OFS	2C1	[26:0]	1A01F1A
PI_SEQ_ARRAY_278	DDR_PI_OFS	2C2	[26:0]	1A10E07
PI_SEQ_ARRAY_279	DDR_PI_OFS	2C3	[26:0]	0051F00
PI_SEQ_ARRAY_280	DDR_PI_OFS	2C4	[26:0]	000403F
PI_SEQ_ARRAY_281	DDR_PI_OFS	2C5	[26:0]	1A01F1A
PI_SEQ_ARRAY_282	DDR_PI_OFS	2C6	[26:0]	1A00E00
PI_SEQ_ARRAY_283	DDR_PI_OFS	2C7	[26:0]	0001F00
PI_SEQ_ARRAY_284	DDR_PI_OFS	2C8	[26:0]	03100F7
PI_SEQ_ARRAY_285	DDR_PI_OFS	2C9	[26:0]	1A10D06
PI_SEQ_ARRAY_286	DDR_PI_OFS	2CA	[26:0]	0051800
PI_SEQ_ARRAY_287	DDR_PI_OFS	2CB	[26:0]	03F0000
PI_SEQ_ARRAY_288	DDR_PI_OFS	2CC	[26:0]	01100EF
PI_SEQ_ARRAY_289	DDR_PI_OFS	2CD	[26:0]	001120B
PI_SEQ_ARRAY_290	DDR_PI_OFS	2CE	[26:0]	0051400
PI_SEQ_ARRAY_291	DDR_PI_OFS	2CF	[26:0]	01A0800
PI_SEQ_ARRAY_292	DDR_PI_OFS	2D0	[26:0]	01102FD
PI_SEQ_ARRAY_293	DDR_PI_OFS	2D1	[26:0]	0012E00
PI_SEQ_ARRAY_294	DDR_PI_OFS	2D2	[26:0]	0000000
PI_SEQ_ARRAY_295	DDR_PI_OFS	2D3	[26:0]	01F0000
PI_SEQ_ARRAY_296	DDR_PI_OFS	2D4	[26:0]	01100FD
PI_SEQ_ARRAY_297	DDR_PI_OFS	2D5	[26:0]	0012E00
PI_SEQ_ARRAY_298	DDR_PI_OFS	2D6	[26:0]	0051700
PI_SEQ_ARRAY_299	DDR_PI_OFS	2D7	[26:0]	01A0801
PI_SEQ_ARRAY_300	DDR_PI_OFS	2D8	[26:0]	001120B
PI_SEQ_ARRAY_301	DDR_PI_OFS	2D9	[26:0]	01F0000
PI_SEQ_ARRAY_302	DDR_PI_OFS	2DA	[26:0]	01100EF
PI_SEQ_ARRAY_303	DDR_PI_OFS	2DB	[26:0]	001120B
PI_SEQ_ARRAY_304	DDR_PI_OFS	2DC	[26:0]	0051400
PI_SEQ_ARRAY_305	DDR_PI_OFS	2DD	[26:0]	01A0800
PI_SEQ_ARRAY_306	DDR_PI_OFS	2DE	[26:0]	01101FC
PI_SEQ_ARRAY_307	DDR_PI_OFS	2DF	[26:0]	0011A00
PI_SEQ_ARRAY_308	DDR_PI_OFS	2E0	[26:0]	0000000
PI_SEQ_ARRAY_309	DDR_PI_OFS	2E1	[26:0]	01F0000
PI_SEQ_ARRAY_310	DDR_PI_OFS	2E2	[26:0]	0051500
PI_SEQ_ARRAY_311	DDR_PI_OFS	2E3	[26:0]	01103FC
PI_SEQ_ARRAY_312	DDR_PI_OFS	2E4	[26:0]	0011A00
PI_SEQ_ARRAY_313	DDR_PI_OFS	2E5	[26:0]	0051500
PI_SEQ_ARRAY_314	DDR_PI_OFS	2E6	[26:0]	01102FC
PI_SEQ_ARRAY_315	DDR_PI_OFS	2E7	[26:0]	0011A00
PI_SEQ_ARRAY_316	DDR_PI_OFS	2E8	[26:0]	0001A00

		V4M		
Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PI_SEQ_ARRAY_317	DDR_PI_OFS	2E9	[26:0]	0000000
PI_SEQ_ARRAY_318	DDR_PI_OFS	2EA	[26:0]	01F0000
PI_SEQ_ARRAY_319	DDR_PI_OFS	2EB	[26:0]	01100FC
PI_SEQ_ARRAY_320	DDR_PI_OFS	2EC	[26:0]	0011A00
PI_SEQ_ARRAY_321	DDR_PI_OFS	2ED	[26:0]	01A0801
PI_SEQ_ARRAY_322	DDR_PI_OFS	2EE	[26:0]	001120B
PI_SEQ_ARRAY_323	DDR_PI_OFS	2EF	[26:0]	0000000
PI_SEQ_ARRAY_324	DDR_PI_OFS	2F0	[26:0]	01F0000
PI_SEQ_ARRAY_325	DDR_PI_OFS	2F1	[26:0]	01108E7
PI_SEQ_ARRAY_326	DDR_PI_OFS	2F2	[26:0]	001120B
PI_SEQ_ARRAY_327	DDR_PI_OFS	2F3	[26:0]	0051400
PI_SEQ_ARRAY_328	DDR_PI_OFS	2F4	[26:0]	1910480
PI_SEQ_ARRAY_329	DDR_PI_OFS	2F5	[26:0]	0021009
PI_SEQ_ARRAY_330	DDR_PI_OFS	2F6	[26:0]	01F0000
PI_SEQ_ARRAY_331	DDR_PI_OFS	2F7	[26:0]	01A0800
PI_SEQ_ARRAY_332	DDR_PI_OFS	2F8	[26:0]	0211E00
PI_SEQ_ARRAY_333	DDR_PI_OFS	2F9	[26:0]	01101FC
PI_SEQ_ARRAY_334	DDR_PI_OFS	2FA	[26:0]	0211A00
PI_SEQ_ARRAY_335	DDR_PI_OFS	2FB	[26:0]	0051500
PI_SEQ_ARRAY_336	DDR_PI_OFS	2FC	[26:0]	01103FC
PI_SEQ_ARRAY_337	DDR_PI_OFS	2FD	[26:0]	0011A00
PI_SEQ_ARRAY_338	DDR_PI_OFS	2FE	[26:0]	0051500
PI_SEQ_ARRAY_339	DDR_PI_OFS	2FF	[26:0]	01100FC
PI_SEQ_ARRAY_340	DDR_PI_OFS	300	[26:0]	0011A00
PI_SEQ_ARRAY_341	DDR_PI_OFS	301	[26:0]	0031A00
PI_SEQ_ARRAY_342	DDR_PI_OFS	302	[26:0]	01A0801
PI_SEQ_ARRAY_343	DDR_PI_OFS	303	[26:0]	0000000
PI_SEQ_ARRAY_344	DDR_PI_OFS	304	[26:0]	01F0000
PI_SEQ_ARRAY_345	DDR_PI_OFS	305	[26:0]	0211E00
PI_SEQ_ARRAY_346	DDR_PI_OFS	306	[26:0]	01108F7
PI_SEQ_ARRAY_347	DDR_PI_OFS	307	[26:0]	001120B
PI_SEQ_ARRAY_348	DDR_PI_OFS	308	[26:0]	01F0000
PI_SEQ_ARRAY_349	DDR_PI_OFS	309	[26:0]	0000000
PI_SEQ_ARRAY_350	DDR_PI_OFS	30A	[26:0]	0000000
PI_SEQ_ARRAY_351	DDR_PI_OFS	30B	[26:0]	0000000
PI_SEQ_ARRAY_352	DDR_PI_OFS	30C	[26:0]	0000000
PI_SEQ_ARRAY_353	DDR_PI_OFS	30D	[26:0]	0000000
PI_SEQ_ARRAY_354	DDR_PI_OFS	30E	[26:0]	0000000
PI_SEQ_ARRAY_355	DDR_PI_OFS	30F	[26:0]	0000000
PI_SEQ_ARRAY_356	DDR_PI_OFS	310	[26:0]	0000000
PI_SEQ_ARRAY_357	DDR_PI_OFS	311	[26:0]	0000000
PI_SEQ_ARRAY_358	DDR_PI_OFS	312	[26:0]	01F0000
PI_SEQ_ARRAY_359	DDR_PI_OFS	313	[26:0]	404FF7F
PI_SEQ_ARRAY_360	DDR_PI_OFS	314	[26:0]	404FF7F

		V4M		
Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PI_SEQ_ARRAY_361	DDR_PI_OFS	315	[26:0]	404FF7F
PI_SEQ_ARRAY_362	DDR_PI_OFS	316	[26:0]	404FF7F
PI_SEQ_ARRAY_363	DDR_PI_OFS	317	[26:0]	404FF7F
PI_SEQ_ARRAY_364	DDR_PI_OFS	318	[26:0]	404FF7F
PI_SEQ_ARRAY_365	DDR_PI_OFS	319	[26:0]	404FF7F
PI_SEQ_ARRAY_366	DDR_PI_OFS	31A	[26:0]	404FF7F
PI_SEQ_ARRAY_367	DDR_PI_OFS	31B	[26:0]	0000000
PI_SEQ_ARRAY_368	DDR_PI_OFS	31C	[26:0]	0000000
PI_SEQ_ARRAY_369	DDR_PI_OFS	31D	[26:0]	0000000
PI_SEQ_ARRAY_370	DDR_PI_OFS	31E	[26:0]	0000000
PI_SEQ_ARRAY_371	DDR_PI_OFS	31F	[26:0]	0000000
PI_SEQ_ARRAY_372	DDR_PI_OFS	320	[26:0]	0000000
PI_SEQ_ARRAY_373	DDR_PI_OFS	321	[26:0]	0000000
PI_SEQ_ARRAY_374	DDR_PI_OFS	322	[26:0]	0000000
PI_SEQ_ARRAY_375	DDR_PI_OFS	323	[26:0]	0000000
PI_SEQ_ARRAY_376	DDR_PI_OFS	324	[26:0]	0000000
PI_SEQ_ARRAY_377	DDR_PI_OFS	325	[26:0]	0000000
PI_SEQ_ARRAY_378	DDR_PI_OFS	326	[26:0]	0000000
PI_SEQ_ARRAY_379	DDR_PI_OFS	327	[26:0]	0000000
PI_SEQ_ARRAY_380	DDR_PI_OFS	328	[26:0]	0000000
PI_SEQ_ARRAY_381	DDR_PI_OFS	329	[26:0]	0000000
PI_SEQ_ARRAY_382	DDR_PI_OFS	32A	[26:0]	0000000
PI_SEQ_ARRAY_383	DDR_PI_OFS	32B	[26:0]	0000000
PI_SEQ_ARRAY_384	DDR_PI_OFS	32C	[26:0]	0000000
PI_SEQ_ARRAY_385	DDR_PI_OFS	32D	[26:0]	0000000
PI_SEQ_ARRAY_386	DDR_PI_OFS	32E	[26:0]	0000000
PI_SEQ_ARRAY_387	DDR_PI_OFS	32F	[26:0]	0000000
PI_SEQ_ARRAY_388	DDR_PI_OFS	330	[26:0]	0000000
PI_SEQ_ARRAY_389	DDR_PI_OFS	331	[26:0]	0000000
PI_SEQ_ARRAY_390	DDR_PI_OFS	332	[26:0]	0000000
PI_SEQ_ARRAY_391	DDR_PI_OFS	333	[26:0]	0000000
PI_SEQ_ARRAY_392	DDR_PI_OFS	334	[26:0]	0000000
PI_SEQ_ARRAY_393	DDR_PI_OFS	335	[26:0]	0000000
PI_SEQ_ARRAY_394	DDR_PI_OFS	336	[26:0]	0000000
PI_SEQ_ARRAY_395	DDR_PI_OFS	337	[26:0]	0000000
PI_SEQ_ARRAY_396	DDR_PI_OFS	338	[26:0]	0000000
PI_SEQ_ARRAY_397	DDR_PI_OFS	339	[26:0]	0000000
PI_SEQ_ARRAY_398	DDR_PI_OFS	33A	[26:0]	0000000
PI_SEQ_ARRAY_399	DDR_PI_OFS	33B	[26:0]	0000000
PI_SEQ_ARRAY_400	DDR_PI_OFS	33C	[26:0]	0000000
PI_SEQ_ARRAY_401	DDR_PI_OFS	33D	[26:0]	0000000
PI_SEQ_ARRAY_402	DDR_PI_OFS	33E	[26:0]	0000000
PI_SEQ_ARRAY_403	DDR_PI_OFS	33F	[26:0]	0000000
PI_SEQ_ARRAY_404	DDR_PI_OFS	340	[26:0]	0000000

		V4M		
Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PI_SEQ_ARRAY_405	DDR_PI_OFS	341	[26:0]	0000000
PI_SEQ_ARRAY_406	DDR_PI_OFS	342	[26:0]	0000000
PI_SEQ_ARRAY_407	DDR_PI_OFS	343	[26:0]	0000000
PI_SEQ_ARRAY_408	DDR_PI_OFS	344	[26:0]	0000000
PI_SEQ_ARRAY_409	DDR_PI_OFS	345	[26:0]	0000000
PI_SEQ_ARRAY_410	DDR_PI_OFS	346	[26:0]	0000000
PI_SEQ_ARRAY_411	DDR_PI_OFS	347	[26:0]	0000000
PI_SEQ_ARRAY_412	DDR_PI_OFS	348	[26:0]	0000000
PI_SEQ_ARRAY_413	DDR_PI_OFS	349	[26:0]	0000000
PI_SEQ_ARRAY_414	DDR_PI_OFS	34A	[26:0]	0000000
PI_SEQ_ARRAY_415	DDR_PI_OFS	34B	[26:0]	0000000
PI_SEQ_ARRAY_416	DDR_PI_OFS	34C	[26:0]	0000000
PI_SEQ_ARRAY_417	DDR_PI_OFS	34D	[26:0]	0000000
PI_SEQ_ARRAY_418	DDR_PI_OFS	34E	[26:0]	0000000
PI_SEQ_ARRAY_419	DDR_PI_OFS	34F	[26:0]	0000000
PI_SEQ_ARRAY_420	DDR_PI_OFS	350	[26:0]	0000000
PI_SEQ_ARRAY_421	DDR_PI_OFS	351	[26:0]	0000000
PI_SEQ_ARRAY_422	DDR_PI_OFS	352	[26:0]	0000000
PI_SEQ_ARRAY_423	DDR_PI_OFS	353	[26:0]	0000000
PI_SEQ_ARRAY_424	DDR_PI_OFS	354	[26:0]	0000000
PI_SEQ_ARRAY_425	DDR_PI_OFS	355	[26:0]	0000000
PI_SEQ_ARRAY_426	DDR_PI_OFS	356	[26:0]	0000000
PI_SEQ_ARRAY_427	DDR_PI_OFS	357	[26:0]	0000000
PI_SEQ_ARRAY_428	DDR_PI_OFS	358	[26:0]	0000000
PI_SEQ_ARRAY_429	DDR_PI_OFS	359	[26:0]	0000000
PI_SEQ_ARRAY_430	DDR_PI_OFS	35A	[26:0]	0000000
PI_SEQ_ARRAY_431	DDR_PI_OFS	35B	[26:0]	0000000
PI_SEQ_ARRAY_432	DDR_PI_OFS	35C	[26:0]	0000000
PI_SEQ_ARRAY_433	DDR_PI_OFS	35D	[26:0]	0000000
PI_SEQ_ARRAY_434	DDR_PI_OFS	35E	[26:0]	0000000
PI_SEQ_ARRAY_435	DDR_PI_OFS	35F	[26:0]	0000000
PI_SEQ_ARRAY_436	DDR_PI_OFS	360	[26:0]	0000000
PI_SEQ_ARRAY_437	DDR_PI_OFS	361	[26:0]	0000000
PI_SEQ_ARRAY_438	DDR_PI_OFS	362	[26:0]	0000000
PI_SEQ_ARRAY_439	DDR_PI_OFS	363	[26:0]	0000000
PI_SEQ_ARRAY_440	DDR_PI_OFS	364	[26:0]	0000000
PI_SEQ_ARRAY_441	DDR_PI_OFS	365	[26:0]	0000000
PI_SEQ_ARRAY_442	DDR_PI_OFS	366	[26:0]	0000000
PI_SEQ_ARRAY_443	DDR_PI_OFS	367	[26:0]	0000000
PI_SEQ_ARRAY_444	DDR_PI_OFS	368	[26:0]	0000000
PI_SEQ_ARRAY_445	DDR_PI_OFS	369	[26:0]	0000000
PI_SEQ_ARRAY_446	DDR_PI_OFS	36A	[26:0]	0000000
PI_SEQ_ARRAY_447	DDR_PI_OFS	36B	[26:0]	0000000
PI_SEQ_ARRAY_448	DDR_PI_OFS	36C	[26:0]	0000000

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Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PI_SEQ_ARRAY_449	DDR_PI_OFS	36D	[26:0]	0000000
PI_SEQ_ARRAY_450	DDR_PI_OFS	36E	[26:0]	0000000
PI_SEQ_ARRAY_451	DDR_PI_OFS	36F	[26:0]	0000000
PI_SEQ_ARRAY_452	DDR_PI_OFS	370	[26:0]	0000000
PI_SEQ_ARRAY_453	DDR_PI_OFS	371	[26:0]	0000000
PI_SEQ_ARRAY_454	DDR_PI_OFS	372	[26:0]	0000000
PI_SEQ_ARRAY_455	DDR_PI_OFS	373	[26:0]	0000000
PI_SEQ_ARRAY_456	DDR_PI_OFS	374	[26:0]	0000000
PI_SEQ_ARRAY_457	DDR_PI_OFS	375	[26:0]	0000000
PI_SEQ_ARRAY_458	DDR_PI_OFS	376	[26:0]	0000000
PI_SEQ_ARRAY_459	DDR_PI_OFS	377	[26:0]	0000000
PI_SEQ_ARRAY_460	DDR_PI_OFS	378	[26:0]	0000000
PI_SEQ_ARRAY_461	DDR_PI_OFS	379	[26:0]	0000000
PI_SEQ_ARRAY_462	DDR_PI_OFS	37A	[26:0]	0000000
PI_SEQ_ARRAY_463	DDR_PI_OFS	37B	[26:0]	0000000
PI_SEQ_ARRAY_464	DDR_PI_OFS	37C	[26:0]	0000000
PI_SEQ_ARRAY_465	DDR_PI_OFS	37D	[26:0]	0000000
PI_SEQ_ARRAY_466	DDR_PI_OFS	37E	[26:0]	0000000
PI_SEQ_ARRAY_467	DDR_PI_OFS	37F	[26:0]	0000000
PI_SEQ_ARRAY_468	DDR_PI_OFS	380	[26:0]	0000000
PI_SEQ_ARRAY_469	DDR_PI_OFS	381	[26:0]	0000000
PI_GROUP0_SEQ_INDEX	DDR_PI_OFS	382	[8:0]	000
PI_GROUP1_SEQ_INDEX	DDR_PI_OFS	382	[24:16]	007
PI_GROUP2_SEQ_INDEX	DDR_PI_OFS	383	[8:0]	00B
PI_GROUP3_SEQ_INDEX	DDR_PI_OFS	383	[24:16]	011
PI_GROUP4_SEQ_INDEX	DDR_PI_OFS	384	[8:0]	017
PI_GROUP5_SEQ_INDEX	DDR_PI_OFS	384	[24:16]	01D
PI_GROUP6_SEQ_INDEX	DDR_PI_OFS	385	[8:0]	03F
PI_GROUP7_SEQ_INDEX	DDR_PI_OFS	385	[24:16]	059
PI_GROUP8_SEQ_INDEX	DDR_PI_OFS	386	[8:0]	06C
PI_GROUP9_SEQ_INDEX	DDR_PI_OFS	386	[24:16]	072
PI_GROUP10_SEQ_INDEX	DDR_PI_OFS	387	[8:0]	078
PI_GROUP11_SEQ_INDEX	DDR_PI_OFS	387	[24:16]	079
PI_GROUP12_SEQ_INDEX	DDR_PI_OFS	388	[8:0]	086
PI_GROUP13_SEQ_INDEX	DDR_PI_OFS	388	[24:16]	096
PI_GROUP14_SEQ_INDEX	DDR_PI_OFS	389	[8:0]	09F
PI_GROUP15_SEQ_INDEX	DDR_PI_OFS	389	[24:16]	0A2
PI_GROUP16_SEQ_INDEX	DDR_PI_OFS	38A	[8:0]	0B1
PI_GROUP17_SEQ_INDEX	DDR_PI_OFS	38A	[24:16]	0B6
PI_GROUP18_SEQ_INDEX	DDR_PI_OFS	38B	[8:0]	0BF
PI_GROUP19_SEQ_INDEX	DDR_PI_OFS	38B	[24:16]	0C5
PI_GROUP20_SEQ_INDEX	DDR_PI_OFS	38C	[8:0]	0D8
PI_GROUP21_SEQ_INDEX	DDR_PI_OFS	38C	[24:16]	0DC
PI_GROUP22_SEQ_INDEX	DDR_PI_OFS	38D	[8:0]	0DD

		V4M		
Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PI_GROUP23_SEQ_INDEX	DDR_PI_OFS	38D	[24:16]	0E0
PI_GROUP24_SEQ_INDEX	DDR_PI_OFS	38E	[8:0]	0E3
PI_GROUP25_SEQ_INDEX	DDR_PI_OFS	38E	[24:16]	0E6
PI_GROUP26_SEQ_INDEX	DDR_PI_OFS	38F	[8:0]	0EC
PI_GROUP27_SEQ_INDEX	DDR_PI_OFS	38F	[24:16]	0F1
PI_GROUP28_SEQ_INDEX	DDR_PI_OFS	390	[8:0]	0F3
PI_GROUP29_SEQ_INDEX	DDR_PI_OFS	390	[24:16]	0FA
PI_GROUP30_SEQ_INDEX	DDR_PI_OFS	391	[8:0]	0FF
PI_GROUP31_SEQ_INDEX	DDR_PI_OFS	391	[24:16]	102
PI_GROUP32_SEQ_INDEX	DDR_PI_OFS	392	[8:0]	111
PI_GROUP33_SEQ_INDEX	DDR_PI_OFS	392	[24:16]	120
PI_GROUP34_SEQ_INDEX	DDR_PI_OFS	393	[8:0]	128
PI_GROUP35_SEQ_INDEX	DDR_PI_OFS	393	[24:16]	12E
PI_GROUP36_SEQ_INDEX	DDR_PI_OFS	394	[8:0]	136
PI_GROUP37_SEQ_INDEX	DDR_PI_OFS	394	[24:16]	13F
PI_GROUP38_SEQ_INDEX	DDR_PI_OFS	395	[8:0]	145
PI_GROUP39_SEQ_INDEX	DDR_PI_OFS	395	[24:16]	14B
PI_GROUP40_SEQ_INDEX	DDR_PI_OFS	396	[8:0]	159
PI_GROUP41_SEQ_INDEX	DDR_PI_OFS	396	[24:16]	15D
PI_GROUP42_SEQ_INDEX	DDR_PI_OFS	397	[8:0]	167
PI_GROUP43_SEQ_INDEX	DDR_PI_OFS	397	[24:16]	168
PI_GROUP44_SEQ_INDEX	DDR_PI_OFS	398	[8:0]	169
PI_GROUP45_SEQ_INDEX	DDR_PI_OFS	398	[24:16]	16A
PI_GROUP46_SEQ_INDEX	DDR_PI_OFS	399	[8:0]	16B
PI_GROUP47_SEQ_INDEX	DDR_PI_OFS	399	[24:16]	16C
PI_GROUP48_SEQ_INDEX	DDR_PI_OFS	39A	[8:0]	16D
PI_GROUP49_SEQ_INDEX	DDR_PI_OFS	39A	[24:16]	16E
PI_SEQ_POINTER_PREFETCH	DDR_PI_OFS	39B	[0]	0
PI_CURRENT_SEQ_POINTER	DDR_PI_OFS	39B	[16:8]	000
PI_CURRENT_SEQ_GROUP_POINTER	DDR_PI_OFS	39B	[29:24]	00
PI_CURRENT_SEQ_POINTER_INSIDE_SEQ_GROUP	DDR_PI_OFS	39C	[8:0]	000
PI_RDLVL_TRAIN_SEQ_0	DDR_PI_OFS	39D	[26:0]	04B1040
PI_RDLVL_TRAIN_SEQ_1	DDR_PI_OFS	39E	[26:0]	00811C0
PI_RDLVL_TRAIN_SEQ_2	DDR_PI_OFS	39F	[26:0]	40811C0
PI_RDLVL_TRAIN_SEQ_3	DDR_PI_OFS	3A0	[26:0]	2000000
PI_RDLVL_TRAIN_SEQ_4	DDR_PI_OFS	3A1	[26:0]	0000000
PI_RDLVL_TRAIN_SEQ_5	DDR_PI_OFS	3A2	[26:0]	0000000
PI_RDLVL_TRAIN_SEQ_6	DDR_PI_OFS	3A3	[26:0]	0000000
PI_RDLVL_TRAIN_SEQ_7	DDR_PI_OFS	3A4	[26:0]	0000000
PI_RDLVL_TRAIN_SEQ_8	DDR_PI_OFS	3A5	[26:0]	0000000
PI_RDLVL_TRAIN_SEQ_9	DDR_PI_OFS	3A6	[26:0]	0000000
PI_RDLVL_TRAIN_SEQ_10	DDR_PI_OFS	3A7	[26:0]	0000000
PI_RDLVL_TRAIN_SEQ_11	DDR_PI_OFS	3A8	[26:0]	0000000
PI_RDLVL_TRAIN_SEQ_12	DDR_PI_OFS	3A9	[26:0]	0000000

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Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PI_RDLVL_TRAIN_SEQ_13	DDR_PI_OFS	3AA	[26:0]	0000000
PI_RDLVL_TRAIN_SEQ_14	DDR_PI_OFS	3AB	[26:0]	0000000
PI_RDLVL_TRAIN_SEQ_15	DDR_PI_OFS	3AC	[26:0]	0000000
PI_RDLVL_TRAIN_SEQ_16	DDR_PI_OFS	3AD	[26:0]	0000000
PI_RDLVL_TRAIN_SEQ_17	DDR_PI_OFS	3AE	[26:0]	0000000
PI_RDLVL_TRAIN_SEQ_18	DDR_PI_OFS	3AF	[26:0]	0000000
PI_RDLVL_TRAIN_SEQ_19	DDR_PI_OFS	3B0	[26:0]	0000000
PI_RDLVL_TRAIN_SEQ_20	DDR_PI_OFS	3B1	[26:0]	0000000
PI_RDLVL_TRAIN_SEQ_21	DDR_PI_OFS	3B2	[26:0]	0000000
PI_RDLVL_BURST_DATA1_0	DDR_PI_OFS	3B3	[7:0]	AA
PI_RDLVL_BURST_DATA1_1	DDR_PI_OFS	3B3	[15:8]	7F
PI_RDLVL_BURST_DATA1_2	DDR_PI_OFS	3B3	[23:16]	40
PI_RDLVL_BURST_DATA1_3	DDR_PI_OFS	3B3	[31:24]	5F
PI_RDLVL_BURST_DATA1_4	DDR_PI_OFS	3B4	[7:0]	6F
PI_RDLVL_BURST_DATA1_5	DDR_PI_OFS	3B4	[15:8]	77
PI_RDLVL_BURST_DATA1_6	DDR_PI_OFS	3B4	[23:16]	7B
PI_RDLVL_BURST_DATA1_7	DDR_PI_OFS	3B4	[31:24]	00
PI_RDLVL_BURST_DATA1_8	DDR_PI_OFS	3B5	[7:0]	AA
PI_RDLVL_BURST_DATA1_9	DDR_PI_OFS	3B5	[15:8]	55
PI_RDLVL_BURST_DATA1_10	DDR_PI_OFS	3B5	[23:16]	B5
PI_RDLVL_BURST_DATA1_11	DDR_PI_OFS	3B5	[31:24]	4A
PI_RDLVL_BURST_DATA1_12	DDR_PI_OFS	3B6	[7:0]	56
PI_RDLVL_BURST_DATA1_13	DDR_PI_OFS	3B6	[15:8]	A9
PI_RDLVL_BURST_DATA1_14	DDR_PI_OFS	3B6	[23:16]	A9
PI_RDLVL_BURST_DATA1_15	DDR_PI_OFS	3B6	[31:24]	B5
PI_RDLVL_BURST_DATA2_0	DDR_PI_OFS	3B7	[7:0]	AA
PI_RDLVL_BURST_DATA2_1	DDR_PI_OFS	3B7	[15:8]	BF
PI_RDLVL_BURST_DATA2_2	DDR_PI_OFS	3B7	[23:16]	80
PI_RDLVL_BURST_DATA2_3	DDR_PI_OFS	3B7	[31:24]	9F
PI_RDLVL_BURST_DATA2_4	DDR_PI_OFS	3B8	[7:0]	AF
PI_RDLVL_BURST_DATA2_5	DDR_PI_OFS	3B8	[15:8]	B7
PI_RDLVL_BURST_DATA2_6	DDR_PI_OFS	3B8	[23:16]	BB
PI_RDLVL_BURST_DATA2_7	DDR_PI_OFS	3B8	[31:24]	00
PI_RDLVL_BURST_DATA2_8	DDR_PI_OFS	3B9	[7:0]	00
PI_RDLVL_BURST_DATA2_9	DDR_PI_OFS	3B9	[15:8]	00
PI_RDLVL_BURST_DATA2_10	DDR_PI_OFS	3B9	[23:16]	00
PI_RDLVL_BURST_DATA2_11	DDR_PI_OFS	3B9	[31:24]	00
PI_RDLVL_BURST_DATA2_12	DDR_PI_OFS	3BA	[7:0]	00
PI_RDLVL_BURST_DATA2_13	DDR_PI_OFS	3BA	[15:8]	00
PI_RDLVL_BURST_DATA2_14	DDR_PI_OFS	3BA	[23:16]	00
PI_RDLVL_BURST_DATA2_15	DDR_PI_OFS	3BA	[31:24]	00
PI_RDLVL_INV_DATA1_0	DDR_PI_OFS	3BB	[7:0]	00
PI_RDLVL_INV_DATA1_1	DDR_PI_OFS	3BB	[15:8]	00
PI_RDLVL_INV_DATA1_2	DDR_PI_OFS	3BB	[23:16]	00

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Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PI_RDLVL_INV_DATA1_3	DDR_PI_OFS	3BB	[31:24]	00
PI_RDLVL_INV_DATA2_0	DDR_PI_OFS	3BC	[7:0]	00
PI_RDLVL_INV_DATA2_1	DDR_PI_OFS	3BC	[15:8]	00
PI_RDLVL_INV_DATA2_2	DDR_PI_OFS	3BC	[23:16]	00
PI_RDLVL_INV_DATA2_3	DDR_PI_OFS	3BC	[31:24]	00
PI_RDLVL_BURST_MASK1_0	DDR_PI_OFS	3BD	[7:0]	00
PI_RDLVL_BURST_MASK1_1	DDR_PI_OFS	3BD	[15:8]	00
PI_RDLVL_BURST_MASK1_2	DDR_PI_OFS	3BD	[23:16]	00
PI_RDLVL_BURST_MASK1_3	DDR_PI_OFS	3BD	[31:24]	00
PI_RDLVL_BURST_MASK1_4	DDR_PI_OFS	3BE	[7:0]	00
PI_RDLVL_BURST_MASK1_5	DDR_PI_OFS	3BE	[15:8]	00
PI_RDLVL_BURST_MASK1_6	DDR_PI_OFS	3BE	[23:16]	00
PI_RDLVL_BURST_MASK1_7	DDR_PI_OFS	3BE	[31:24]	00
PI_RDLVL_BURST_MASK2_0	DDR_PI_OFS	3BF	[7:0]	00
PI_RDLVL_BURST_MASK2_1	DDR_PI_OFS	3BF	[15:8]	00
PI_RDLVL_BURST_MASK2_2	DDR_PI_OFS	3BF	[23:16]	00
PI_RDLVL_BURST_MASK2_3	DDR_PI_OFS	3BF	[31:24]	00
PI_RDLVL_BURST_MASK2_4	DDR_PI_OFS	3C0	[7:0]	00
PI_RDLVL_BURST_MASK2_5	DDR_PI_OFS	3C0	[15:8]	00
PI_RDLVL_BURST_MASK2_6	DDR_PI_OFS	3C0	[23:16]	00
PI_RDLVL_BURST_MASK2_7	DDR_PI_OFS	3C0	[31:24]	00
PI_SEQ_WAIT_0	DDR_PI_OFS	3C1	[23:0]	002AF8
PI_SEQ_WAIT_1	DDR_PI_OFS	3C2	[23:0]	006B6B
PI_SEQ_WAIT_2	DDR_PI_OFS	3C3	[23:0]	00006E
PI_SEQ_WAIT_3	DDR_PI_OFS	3C4	[23:0]	000000
PI_SEQ_WAIT_4	DDR_PI_OFS	3C5	[23:0]	000000
PI_SEQ_WAIT_5	DDR_PI_OFS	3C6	[23:0]	000000
PI_SEQ_WAIT_6	DDR_PI_OFS	3C7	[23:0]	000000
PI_SEQ_WAIT_7	DDR_PI_OFS	3C8	[23:0]	000000
PI_SEQ_WAIT_8	DDR_PI_OFS	3C9	[23:0]	000000
PI_SEQ_WAIT_9	DDR_PI_OFS	3CA	[23:0]	000000
PI_SEQ_WAIT_10	DDR_PI_OFS	3CB	[23:0]	000000
PI_SEQ_WAIT_11	DDR_PI_OFS	3CC	[23:0]	000000
PI_SEQ_WAIT_12	DDR_PI_OFS	3CD	[23:0]	000000
PI_SEQ_WAIT_13	DDR_PI_OFS	3CE	[23:0]	000000
PI_SEQ_WAIT_14	DDR_PI_OFS	3CF	[23:0]	000000
PI_SEQ_WAIT_15	DDR_PI_OFS	3D0	[23:0]	000000
PI_SEQ_WAIT_16_F0	DDR_PI_OFS	3D1	[23:0]	00000E
PI_SEQ_WAIT_16_F1	DDR_PI_OFS	3D2	[23:0]	0000C8
PI_SEQ_WAIT_16_F2	DDR_PI_OFS	3D3	[23:0]	000216
PI_SEQ_WAIT_17_F0	DDR_PI_OFS	3D4	[23:0]	000001
PI_SEQ_WAIT_17_F1	DDR_PI_OFS	3D5	[23:0]	000003
PI_SEQ_WAIT_17_F2	DDR_PI_OFS	3D6	[23:0]	000007
PI_SEQ_WAIT_18_F0	DDR_PI_OFS	3D7	[23:0]	000007

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Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PI_SEQ_WAIT_18_F1	DDR_PI_OFS	3D8	[23:0]	000009
PI_SEQ_WAIT_18_F2	DDR_PI_OFS	3D9	[23:0]	000013
PI_SEQ_WAIT_19_F0	DDR_PI_OFS	3DA	[23:0]	000002
PI_SEQ_WAIT_19_F1	DDR_PI_OFS	3DB	[23:0]	000010
PI_SEQ_WAIT_19_F2	DDR_PI_OFS	3DC	[23:0]	00002B
PI_SEQ_WAIT_20_F0	DDR_PI_OFS	3DD	[23:0]	000000
PI_SEQ_WAIT_20_F1	DDR_PI_OFS	3DE	[23:0]	000000
PI_SEQ_WAIT_20_F2	DDR_PI_OFS	3DF	[23:0]	000000
PI_SEQ_WAIT_21_F0	DDR_PI_OFS	3E0	[23:0]	000000
PI_SEQ_WAIT_21_F1	DDR_PI_OFS	3E1	[23:0]	000000
PI_SEQ_WAIT_21_F2	DDR_PI_OFS	3E2	[23:0]	000000
PI_SEQ_WAIT_22_F0	DDR_PI_OFS	3E3	[23:0]	000000
PI_SEQ_WAIT_22_F1	DDR_PI_OFS	3E4	[23:0]	000000
PI_SEQ_WAIT_22_F2	DDR_PI_OFS	3E5	[23:0]	000000
PI_SEQ_WAIT_23_F0	DDR_PI_OFS	3E6	[23:0]	000000
PI_SEQ_WAIT_23_F1	DDR_PI_OFS	3E7	[23:0]	000000
PI_SEQ_WAIT_23_F2	DDR_PI_OFS	3E8	[23:0]	000000
PI_SEQ_WAIT_24_F0	DDR_PI_OFS	3E9	[23:0]	000007
PI_SEQ_WAIT_24_F1	DDR_PI_OFS	3EA	[23:0]	000051
PI_SEQ_WAIT_24_F2	DDR_PI_OFS	3EB	[23:0]	0000D7
PI_SEQ_WAIT_25_F0	DDR_PI_OFS	3EC	[23:0]	00000C
PI_SEQ_WAIT_25_F1	DDR_PI_OFS	3ED	[23:0]	0000A1
PI_SEQ_WAIT_25_F2	DDR_PI_OFS	3EE	[23:0]	0001AC
PI_SEQ_WAIT_26_F0	DDR_PI_OFS	3EF	[23:0]	000000
PI_SEQ_WAIT_26_F1	DDR_PI_OFS	3F0	[23:0]	000000
PI_SEQ_WAIT_26_F2	DDR_PI_OFS	3F1	[23:0]	000009
PI_SEQ_WAIT_27_F0	DDR_PI_OFS	3F2	[23:0]	000000
PI_SEQ_WAIT_27_F1	DDR_PI_OFS	3F3	[23:0]	000000
PI_SEQ_WAIT_27_F2	DDR_PI_OFS	3F4	[23:0]	000000
PI_SEQ_WAIT_28_F0	DDR_PI_OFS	3F5	[23:0]	000000
PI_SEQ_WAIT_28_F1	DDR_PI_OFS	3F6	[23:0]	000000
PI_SEQ_WAIT_28_F2	DDR_PI_OFS	3F7	[23:0]	000000
PI_SEQ_WAIT_29_F0	DDR_PI_OFS	3F8	[23:0]	000000
PI_SEQ_WAIT_29_F1	DDR_PI_OFS	3F9	[23:0]	000000
PI_SEQ_WAIT_29_F2	DDR_PI_OFS	3FA	[23:0]	000000
PI_SEQ_WAIT_30_F0	DDR_PI_OFS	3FB	[23:0]	000000
PI_SEQ_WAIT_30_F1	DDR_PI_OFS	3FC	[23:0]	000000
PI_SEQ_WAIT_30_F2	DDR_PI_OFS	3FD	[23:0]	000000
PI_SEQ_WAIT_31_F0	DDR_PI_OFS	3FE	[23:0]	00000F
PI_SEQ_WAIT_31_F1	DDR_PI_OFS	3FF	[23:0]	0000C9
PI_SEQ_WAIT_31_F2	DDR_PI_OFS	400	[23:0]	000217
PI_SEQ_WAIT_32_F0	DDR_PI_OFS	401	[23:0]	000000
PI_SEQ_WAIT_32_F1	DDR_PI_OFS	402	[23:0]	000000
PI_SEQ_WAIT_32_F2	DDR_PI_OFS	403	[23:0]	000000

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Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PI_SEQ_WAIT_33_F0	DDR_PI_OFS	404	[23:0]	000000
PI_SEQ_WAIT_33_F1	DDR_PI_OFS	405	[23:0]	000000
PI_SEQ_WAIT_33_F2	DDR_PI_OFS	406	[23:0]	000000
PI_SEQ_WAIT_34_F0	DDR_PI_OFS	407	[23:0]	000000
PI_SEQ_WAIT_34_F1	DDR_PI_OFS	408	[23:0]	000000
PI_SEQ_WAIT_34_F2	DDR_PI_OFS	409	[23:0]	000000
PI_SEQ_WAIT_35_F0	DDR_PI_OFS	40A	[23:0]	000000
PI_SEQ_WAIT_35_F1	DDR_PI_OFS	40B	[23:0]	000000
PI_SEQ_WAIT_35_F2	DDR_PI_OFS	40C	[23:0]	000000
PI_WP_GAP_0_F0	DDR_PI_OFS	40D	[14:0]	0011
PI_WP_GAP_0_F1	DDR_PI_OFS	40D	[30:16]	0025
PI_WP_GAP_0_F2	DDR_PI_OFS	40E	[14:0]	0043
PI_RP_GAP_0_F0	DDR_PI_OFS	40E	[30:16]	0008
PI_RP_GAP_0_F1	DDR_PI_OFS	40F	[14:0]	0008
PI_RP_GAP_0_F2	DDR_PI_OFS	40F	[30:16]	0010
PI_WR_GAP_S_0_F0	DDR_PI_OFS	410	[14:0]	0016
PI_WR_GAP_S_0_F1	DDR_PI_OFS	410	[30:16]	001E
PI_WR_GAP_S_0_F2	DDR_PI_OFS	411	[14:0]	0032
PI_WR_GAP_L_0_F0	DDR_PI_OFS	411	[30:16]	0016
PI_WR_GAP_L_0_F1	DDR_PI_OFS	412	[14:0]	001E
PI_WR_GAP_L_0_F2	DDR_PI_OFS	412	[30:16]	0032
PI_RW_GAP_0_F0	DDR_PI_OFS	413	[14:0]	000E
PI_RW_GAP_0_F1	DDR_PI_OFS	413	[30:16]	0012
PI_RW_GAP_0_F2	DDR_PI_OFS	414	[14:0]	0029
PI_WW_GAP_S_0_F0	DDR_PI_OFS	414	[30:16]	0008
PI_WW_GAP_S_0_F1	DDR_PI_OFS	415	[14:0]	0008
PI_WW_GAP_S_0_F2	DDR_PI_OFS	415	[30:16]	0008
PI_WW_GAP_L_0_F0	DDR_PI_OFS	416	[14:0]	0008
PI_WW_GAP_L_0_F1	DDR_PI_OFS	416	[30:16]	0008
PI_WW_GAP_L_0_F2	DDR_PI_OFS	417	[14:0]	0008
PI_RR_GAP_S_0_F0	DDR_PI_OFS	417	[30:16]	0008
PI_RR_GAP_S_0_F1	DDR_PI_OFS	418	[14:0]	0008
PI_RR_GAP_S_0_F2	DDR_PI_OFS	418	[30:16]	0008
PI_RR_GAP_L_0_F0	DDR_PI_OFS	419	[14:0]	0008
PI_RR_GAP_L_0_F1	DDR_PI_OFS	419	[30:16]	0008
PI_RR_GAP_L_0_F2	DDR_PI_OFS	41A	[14:0]	0008
PI_WP_GAP_1_F0	DDR_PI_OFS	41A	[30:16]	0011
PI_WP_GAP_1_F1	DDR_PI_OFS	41B	[14:0]	0025
PI_WP_GAP_1_F2	DDR_PI_OFS	41B	[30:16]	0043
PI_RP_GAP_1_F0	DDR_PI_OFS	41C	[14:0]	0008
PI_RP_GAP_1_F1	DDR_PI_OFS	41C	[30:16]	0008
PI_RP_GAP_1_F2	DDR_PI_OFS	41D	[14:0]	0010
PI_WR_GAP_S_1_F0	DDR_PI_OFS	41D	[30:16]	0016
PI_WR_GAP_S_1_F1	DDR_PI_OFS	41E	[14:0]	001E

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Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PI_WR_GAP_S_1_F2	DDR_PI_OFS	41E	[30:16]	0032
PI_WR_GAP_L_1_F0	DDR_PI_OFS	41F	[14:0]	0016
PI_WR_GAP_L_1_F1	DDR_PI_OFS	41F	[30:16]	001E
PI_WR_GAP_L_1_F2	DDR_PI_OFS	420	[14:0]	0032
PI_RW_GAP_1_F0	DDR_PI_OFS	420	[30:16]	000E
PI_RW_GAP_1_F1	DDR_PI_OFS	421	[14:0]	0012
PI_RW_GAP_1_F2	DDR_PI_OFS	421	[30:16]	0029
PI_WW_GAP_S_1_F0	DDR_PI_OFS	422	[14:0]	0008
PI_WW_GAP_S_1_F1	DDR_PI_OFS	422	[30:16]	0008
PI_WW_GAP_S_1_F2	DDR_PI_OFS	423	[14:0]	0008
PI_WW_GAP_L_1_F0	DDR_PI_OFS	423	[30:16]	0008
PI_WW_GAP_L_1_F1	DDR_PI_OFS	424	[14:0]	0008
PI_WW_GAP_L_1_F2	DDR_PI_OFS	424	[30:16]	0008
PI_RR_GAP_S_1_F0	DDR_PI_OFS	425	[14:0]	0008
PI_RR_GAP_S_1_F1	DDR_PI_OFS	425	[30:16]	0008
PI_RR_GAP_S_1_F2	DDR_PI_OFS	426	[14:0]	0008
PI_RR_GAP_L_1_F0	DDR_PI_OFS	426	[30:16]	0008
PI_RR_GAP_L_1_F1	DDR_PI_OFS	427	[14:0]	0008
PI_RR_GAP_L_1_F2	DDR_PI_OFS	427	[30:16]	0008
PI_WP_GAP_2_F0	DDR_PI_OFS	428	[14:0]	0011
PI_WP_GAP_2_F1	DDR_PI_OFS	428	[30:16]	0025
PI_WP_GAP_2_F2	DDR_PI_OFS	429	[14:0]	0043
PI_RP_GAP_2_F0	DDR_PI_OFS	429	[30:16]	0008
PI_RP_GAP_2_F1	DDR_PI_OFS	42A	[14:0]	0008
PI_RP_GAP_2_F2	DDR_PI_OFS	42A	[30:16]	0010
PI_WR_GAP_S_2_F0	DDR_PI_OFS	42B	[14:0]	0016
PI_WR_GAP_S_2_F1	DDR_PI_OFS	42B	[30:16]	001E
PI_WR_GAP_S_2_F2	DDR_PI_OFS	42C	[14:0]	0032
PI_WR_GAP_L_2_F0	DDR_PI_OFS	42C	[30:16]	0016
PI_WR_GAP_L_2_F1	DDR_PI_OFS	42D	[14:0]	001E
PI_WR_GAP_L_2_F2	DDR_PI_OFS	42D	[30:16]	0032
PI_RW_GAP_2_F0	DDR_PI_OFS	42E	[14:0]	000E
PI_RW_GAP_2_F1	DDR_PI_OFS	42E	[30:16]	0012
PI_RW_GAP_2_F2	DDR_PI_OFS	42F	[14:0]	0029
PI_WW_GAP_S_2_F0	DDR_PI_OFS	42F	[30:16]	0008
PI_WW_GAP_S_2_F1	DDR_PI_OFS	430	[14:0]	0008
PI_WW_GAP_S_2_F2	DDR_PI_OFS	430	[30:16]	0008
PI_WW_GAP_L_2_F0	DDR_PI_OFS	431	[14:0]	0008
PI_WW_GAP_L_2_F1	DDR_PI_OFS	431	[30:16]	0008
PI_WW_GAP_L_2_F2	DDR_PI_OFS	432	[14:0]	0008
PI_RR_GAP_S_2_F0	DDR_PI_OFS	432	[30:16]	0008
PI_RR_GAP_S_2_F1	DDR_PI_OFS	433	[14:0]	0008
PI_RR_GAP_S_2_F2	DDR_PI_OFS	433	[30:16]	0008
PI_RR_GAP_L_2_F0	DDR_PI_OFS	434	[14:0]	0008

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Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PI_RR_GAP_L_2_F1	DDR_PI_OFS	434	[30:16]	0008
PI_RR_GAP_L_2_F2	DDR_PI_OFS	435	[14:0]	0008
PI_WP_GAP_3_F0	DDR_PI_OFS	435	[30:16]	0011
PI_WP_GAP_3_F1	DDR_PI_OFS	436	[14:0]	0025
PI_WP_GAP_3_F2	DDR_PI_OFS	436	[30:16]	0043
PI_RP_GAP_3_F0	DDR_PI_OFS	437	[14:0]	0008
PI_RP_GAP_3_F1	DDR_PI_OFS	437	[30:16]	0008
PI_RP_GAP_3_F2	DDR_PI_OFS	438	[14:0]	0010
PI_WR_GAP_S_3_F0	DDR_PI_OFS	438	[30:16]	0016
PI_WR_GAP_S_3_F1	DDR_PI_OFS	439	[14:0]	001E
PI_WR_GAP_S_3_F2	DDR_PI_OFS	439	[30:16]	0032
PI_WR_GAP_L_3_F0	DDR_PI_OFS	43A	[14:0]	0016
PI_WR_GAP_L_3_F1	DDR_PI_OFS	43A	[30:16]	001E
PI_WR_GAP_L_3_F2	DDR_PI_OFS	43B	[14:0]	0032
PI_RW_GAP_3_F0	DDR_PI_OFS	43B	[30:16]	000E
PI_RW_GAP_3_F1	DDR_PI_OFS	43C	[14:0]	0012
PI_RW_GAP_3_F2	DDR_PI_OFS	43C	[30:16]	0029
PI_WW_GAP_S_3_F0	DDR_PI_OFS	43D	[14:0]	0008
PI_WW_GAP_S_3_F1	DDR_PI_OFS	43D	[30:16]	0008
PI_WW_GAP_S_3_F2	DDR_PI_OFS	43E	[14:0]	0008
PI_WW_GAP_L_3_F0	DDR_PI_OFS	43E	[30:16]	0008
PI_WW_GAP_L_3_F1	DDR_PI_OFS	43F	[14:0]	0008
PI_WW_GAP_L_3_F2	DDR_PI_OFS	43F	[30:16]	0008
PI_RR_GAP_S_3_F0	DDR_PI_OFS	440	[14:0]	0008
PI_RR_GAP_S_3_F1	DDR_PI_OFS	440	[30:16]	0008
PI_RR_GAP_S_3_F2	DDR_PI_OFS	441	[14:0]	0008
PI_RR_GAP_L_3_F0	DDR_PI_OFS	441	[30:16]	0008
PI_RR_GAP_L_3_F1	DDR_PI_OFS	442	[14:0]	0008
PI_RR_GAP_L_3_F2	DDR_PI_OFS	442	[30:16]	0008
PI_ADDR_ARRAY_BANK_0	DDR_PI_OFS	443	[3:0]	0
PI_ADDR_ARRAY_ROW_0	DDR_PI_OFS	443	[25:8]	00000
PI_ADDR_ARRAY_COL_0	DDR_PI_OFS	444	[11:0]	000
PI_ADDR_ARRAY_BANK_1	DDR_PI_OFS	444	[19:16]	0
PI_ADDR_ARRAY_ROW_1	DDR_PI_OFS	445	[17:0]	00000
PI_ADDR_ARRAY_COL_1	DDR_PI_OFS	446	[11:0]	000
PI_ADDR_ARRAY_BANK_2	DDR_PI_OFS	446	[19:16]	0
PI_ADDR_ARRAY_ROW_2	DDR_PI_OFS	447	[17:0]	00000
PI_ADDR_ARRAY_COL_2	DDR_PI_OFS	448	[11:0]	000
PI_ADDR_ARRAY_BANK_3	DDR_PI_OFS	448	[19:16]	0
PI_ADDR_ARRAY_ROW_3	DDR_PI_OFS	449	[17:0]	00000
PI_ADDR_ARRAY_COL_3	DDR_PI_OFS	44A	[11:0]	000
PI_ADDR_ARRAY_BANK_4	DDR_PI_OFS	44A	[19:16]	0
PI_ADDR_ARRAY_ROW_4	DDR_PI_OFS	44B	[17:0]	00000
PI_ADDR_ARRAY_COL_4	DDR_PI_OFS	44C	[11:0]	000

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Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PI_ADDR_ARRAY_BANK_5	DDR_PI_OFS	44C	[19:16]	0
PI_ADDR_ARRAY_ROW_5	DDR_PI_OFS	44D	[17:0]	00000
PI_ADDR_ARRAY_COL_5	DDR_PI_OFS	44E	[11:0]	000
PI_ADDR_ARRAY_BANK_6	DDR_PI_OFS	44E	[19:16]	0
PI_ADDR_ARRAY_ROW_6	DDR_PI_OFS	44F	[17:0]	00000
PI_ADDR_ARRAY_COL_6	DDR_PI_OFS	450	[11:0]	000
PI_ADDR_ARRAY_BANK_7	DDR_PI_OFS	450	[19:16]	0
PI_ADDR_ARRAY_ROW_7	DDR_PI_OFS	451	[17:0]	00000
PI_ADDR_ARRAY_COL_7	DDR_PI_OFS	452	[11:0]	000
PI_ADDR_ARRAY_BANK_8	DDR_PI_OFS	452	[19:16]	0
PI_ADDR_ARRAY_ROW_8	DDR_PI_OFS	453	[17:0]	00000
PI_ADDR_ARRAY_COL_8	DDR_PI_OFS	454	[11:0]	000
PI_ADDR_ARRAY_BANK_9	DDR_PI_OFS	454	[19:16]	0
PI_ADDR_ARRAY_ROW_9	DDR_PI_OFS	455	[17:0]	00000
PI_ADDR_ARRAY_COL_9	DDR_PI_OFS	456	[11:0]	000
PI_ADDR_ARRAY_BANK_10	DDR_PI_OFS	456	[19:16]	0
PI_ADDR_ARRAY_ROW_10	DDR_PI_OFS	457	[17:0]	00000
PI_ADDR_ARRAY_COL_10	DDR_PI_OFS	458	[11:0]	000
PI_ADDR_ARRAY_BANK_11	DDR_PI_OFS	458	[19:16]	0
PI_ADDR_ARRAY_ROW_11	DDR_PI_OFS	459	[17:0]	00000
PI_ADDR_ARRAY_COL_11	DDR_PI_OFS	45A	[11:0]	000
PI_ADDR_ARRAY_BANK_12	DDR_PI_OFS	45A	[19:16]	0
PI_ADDR_ARRAY_ROW_12	DDR_PI_OFS	45B	[17:0]	00000
PI_ADDR_ARRAY_COL_12	DDR_PI_OFS	45C	[11:0]	000
PI_ADDR_ARRAY_BANK_13	DDR_PI_OFS	45C	[19:16]	0
PI_ADDR_ARRAY_ROW_13	DDR_PI_OFS	45D	[17:0]	00000
PI_ADDR_ARRAY_COL_13	DDR_PI_OFS	45E	[11:0]	000
PI_ADDR_ARRAY_BANK_14	DDR_PI_OFS	45E	[19:16]	0
PI_ADDR_ARRAY_ROW_14	DDR_PI_OFS	45F	[17:0]	00000
PI_ADDR_ARRAY_COL_14	DDR_PI_OFS	460	[11:0]	000
PI_ADDR_ARRAY_BANK_15	DDR_PI_OFS	460	[19:16]	0
PI_ADDR_ARRAY_ROW_15	DDR_PI_OFS	461	[17:0]	00000
PI_ADDR_ARRAY_COL_15	DDR_PI_OFS	462	[11:0]	000
PI_ADDR_ARRAY_PARAM_0	DDR_PI_OFS	462	[31:16]	0000
PI_ADDR_ARRAY_PARAM_1	DDR_PI_OFS	463	[15:0]	0000
PI_ADDR_ARRAY_PARAM_2	DDR_PI_OFS	463	[31:16]	0000
PI_ADDR_ARRAY_PARAM_3	DDR_PI_OFS	464	[15:0]	0000
PI_DARRAY0_0	DDR_PI_OFS	464	[23:16]	00
PI_DARRAY0_1	DDR_PI_OFS	464	[31:24]	00
PI_DARRAY0_2	DDR_PI_OFS	465	[7:0]	00
PI_DARRAY0_3	DDR_PI_OFS	465	[15:8]	00
PI_DARRAY0_4	DDR_PI_OFS	465	[23:16]	00
PI_DARRAY0_5	DDR_PI_OFS	465	[31:24]	00
PI_DARRAY0_6	DDR_PI_OFS	466	[7:0]	00

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Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PI_DARRAY0_7	DDR_PI_OFS	466	[15:8]	00
PI_DARRAY0_8	DDR_PI_OFS	466	[23:16]	55
PI_DARRAY0_9	DDR_PI_OFS	466	[31:24]	00
PI_DARRAY0_10	DDR_PI_OFS	467	[7:0]	00
PI_DARRAY0_11	DDR_PI_OFS	467	[15:8]	00
PI_DARRAY0_12	DDR_PI_OFS	467	[23:16]	00
PI_DARRAY0_13	DDR_PI_OFS	467	[31:24]	00
PI_DARRAY0_14	DDR_PI_OFS	468	[7:0]	00
PI_DARRAY0_15	DDR_PI_OFS	468	[15:8]	00
PI_DARRAY0_16	DDR_PI_OFS	468	[23:16]	00
PI_DARRAY0_17	DDR_PI_OFS	468	[31:24]	00
PI_DARRAY0_18	DDR_PI_OFS	469	[7:0]	00
PI_DARRAY0_19	DDR_PI_OFS	469	[15:8]	00
PI_DARRAY0_20	DDR_PI_OFS	469	[23:16]	00
PI_DARRAY0_21	DDR_PI_OFS	469	[31:24]	5A
PI_DARRAY0_22	DDR_PI_OFS	46A	[7:0]	00
PI_DARRAY0_23	DDR_PI_OFS	46A	[15:8]	00
PI_DARRAY0_24	DDR_PI_OFS	46A	[23:16]	3C
PI_DARRAY0_25	DDR_PI_OFS	46A	[31:24]	00
PI_DARRAY0_26	DDR_PI_OFS	46B	[7:0]	00
PI_DARRAY0_27	DDR_PI_OFS	46B	[15:8]	00
PI_DARRAY0_28	DDR_PI_OFS	46B	[23:16]	00
PI_DARRAY0_29	DDR_PI_OFS	46B	[31:24]	00
PI_DARRAY0_30	DDR_PI_OFS	46C	[7:0]	00
PI_DARRAY0_31	DDR_PI_OFS	46C	[15:8]	00
PI_DARRAY0_32	DDR_PI_OFS	46C	[23:16]	00
PI_DARRAY0_33	DDR_PI_OFS	46C	[31:24]	00
PI_DARRAY0_34	DDR_PI_OFS	46D	[7:0]	00
PI_DARRAY0_35	DDR_PI_OFS	46D	[15:8]	00
PI_DARRAY0_36	DDR_PI_OFS	46D	[23:16]	00
PI_DARRAY0_37	DDR_PI_OFS	46D	[31:24]	00
PI_DARRAY0_38	DDR_PI_OFS	46E	[7:0]	00
PI_DARRAY0_39	DDR_PI_OFS	46E	[15:8]	00
PI_DARRAY0_40	DDR_PI_OFS	46E	[23:16]	00
PI_DARRAY0_41	DDR_PI_OFS	46E	[31:24]	00
PI_DARRAY0_42	DDR_PI_OFS	46F	[7:0]	00
PI_DARRAY0_43	DDR_PI_OFS	46F	[15:8]	00
PI_DARRAY0_44	DDR_PI_OFS	46F	[23:16]	00
PI_DARRAY0_45	DDR_PI_OFS	46F	[31:24]	00
PI_DARRAY0_46	DDR_PI_OFS	470	[7:0]	00
PI_DARRAY0_47	DDR_PI_OFS	470	[15:8]	00
PI_DARRAY0_48	DDR_PI_OFS	470	[23:16]	00
PI_DARRAY0_49	DDR_PI_OFS	470	[31:24]	00
PI_DARRAY0_50	DDR_PI_OFS	471	[7:0]	00

		V4M		
Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PI_DARRAY0_51	DDR_PI_OFS	471	[15:8]	00
PI_DARRAY0_52	DDR_PI_OFS	471	[23:16]	00
PI_DARRAY0_53	DDR_PI_OFS	471	[31:24]	00
PI_DARRAY0_54	DDR_PI_OFS	472	[7:0]	00
PI_DARRAY0_55	DDR_PI_OFS	472	[15:8]	00
PI_DARRAY0_56	DDR_PI_OFS	472	[23:16]	00
PI_DARRAY0_57	DDR_PI_OFS	472	[31:24]	00
PI_DARRAY0_58	DDR_PI_OFS	473	[7:0]	00
PI_DARRAY0_59	DDR_PI_OFS	473	[15:8]	00
PI_DARRAY0_60	DDR_PI_OFS	473	[23:16]	00
PI_DARRAY0_61	DDR_PI_OFS	473	[31:24]	00
PI_DARRAY0_62	DDR_PI_OFS	474	[7:0]	00
PI_DARRAY0_63	DDR_PI_OFS	474	[15:8]	00
PI_DARRAY0_64	DDR_PI_OFS	475	[31:0]	00000000
PI_DARRAY0_64_1	DDR_PI_OFS	476	[31:0]	00000000
PI_DARRAY0_64_2	DDR_PI_OFS	477	[31:0]	00000000
PI_DARRAY0_64_3	DDR_PI_OFS	478	[31:0]	00000000
PI_DARRAY0_65	DDR_PI_OFS	479	[31:0]	00000000
PI_DARRAY0_65_1	DDR_PI_OFS	47A	[31:0]	00000000
PI_DARRAY0_65_2	DDR_PI_OFS	47B	[31:0]	00000000
PI_DARRAY0_65_3	DDR_PI_OFS	47C	[31:0]	00000000
PI_DARRAY0_66	DDR_PI_OFS	47D	[31:0]	00000000
PI_DARRAY0_66_1	DDR_PI_OFS	47E	[31:0]	00000000
PI_DARRAY0_66_2	DDR_PI_OFS	47F	[31:0]	00000000
PI_DARRAY0_66_3	DDR_PI_OFS	480	[31:0]	00000000
PI_DARRAY0_67	DDR_PI_OFS	481	[31:0]	00000000
PI_DARRAY0_67_1	DDR_PI_OFS	482	[31:0]	00000000
PI_DARRAY0_67_2	DDR_PI_OFS	483	[31:0]	00000000
PI_DARRAY0_67_3	DDR_PI_OFS	484	[31:0]	00000000
PI_DARRAY0_68	DDR_PI_OFS	485	[31:0]	00000000
PI_DARRAY0_68_1	DDR_PI_OFS	486	[31:0]	00000000
PI_DARRAY0_68_2	DDR_PI_OFS	487	[31:0]	00000000
PI_DARRAY0_68_3	DDR_PI_OFS	488	[31:0]	00000000
PI_DARRAY0_69	DDR_PI_OFS	489	[31:0]	00000000
PI_DARRAY0_69_1	DDR_PI_OFS	48A	[31:0]	00000000
PI_DARRAY0_69_2	DDR_PI_OFS	48B	[31:0]	00000000
PI_DARRAY0_69_3	DDR_PI_OFS	48C	[31:0]	00000000
PI_DARRAY0_70	DDR_PI_OFS	48D	[31:0]	00000000
PI_DARRAY0_70_1	DDR_PI_OFS	48E	[31:0]	00000000
PI_DARRAY0_70_2	DDR_PI_OFS	48F	[31:0]	00000000
PI_DARRAY0_70_3	DDR_PI_OFS	490	[31:0]	00000000
PI_DARRAY0_71	DDR_PI_OFS	491	[31:0]	00000000
PI_DARRAY0_71_1	DDR_PI_OFS	492	[31:0]	00000000
PI_DARRAY0_71_2	DDR_PI_OFS	493	[31:0]	00000000

		V4M		
Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PI_DARRAY0_71_3	DDR_PI_OFS	494	[31:0]	00000000
PI_DARRAY0_72	DDR_PI_OFS	495	[31:0]	00000000
PI_DARRAY0_73	DDR_PI_OFS	496	[31:0]	00000000
PI_DARRAY0_74	DDR_PI_OFS	497	[31:0]	00000000
PI_DARRAY0_75	DDR_PI_OFS	498	[31:0]	00000000
PI_DARRAY0_76	DDR_PI_OFS	499	[31:0]	00000000
PI_DARRAY0_77	DDR_PI_OFS	49A	[31:0]	00000000
PI_DARRAY0_78	DDR_PI_OFS	49B	[31:0]	00000000
PI_DARRAY0_79	DDR_PI_OFS	49C	[31:0]	00000000
PI_DARRAY3_0_CS0_F0	DDR_PI_OFS	49D	[7:0]	04
PI_DARRAY3_1_CS0_F0	DDR_PI_OFS	49D	[15:8]	00
PI_DARRAY3_2_CS0_F0	DDR_PI_OFS	49D	[23:16]	F1
PI_DARRAY3_3_CS0_F0	DDR_PI_OFS	49D	[31:24]	00
PI_DARRAY3_4_CS0_F0	DDR_PI_OFS	49E	[7:0]	00
PI_DARRAY3_5_CS0_F0	DDR_PI_OFS	49E	[15:8]	5D
PI_DARRAY3_6_CS0_F0	DDR_PI_OFS	49E	[23:16]	00
PI_DARRAY3_7_CS0_F0	DDR_PI_OFS	49E	[31:24]	5D
PI_DARRAY3_8_CS0_F0	DDR_PI_OFS	49F	[7:0]	00
PI_DARRAY3_9_CS0_F0	DDR_PI_OFS	49F	[15:8]	00
PI_DARRAY3_10_CS0_F0	DDR_PI_OFS	49F	[23:16]	00
PI_DARRAY3_11_CS0_F0	DDR_PI_OFS	49F	[31:24]	00
PI_DARRAY3_12_CS0_F0	DDR_PI_OFS	4A0	[7:0]	00
PI_DARRAY3_13_CS0_F0	DDR_PI_OFS	4A0	[15:8]	00
PI_DARRAY3_14_CS0_F0	DDR_PI_OFS	4A0	[23:16]	00
PI_DARRAY3_15_CS0_F0	DDR_PI_OFS	4A0	[31:24]	00
PI_DARRAY3_16_CS0_F0	DDR_PI_OFS	4A1	[7:0]	00
PI_DARRAY3_17_CS0_F0	DDR_PI_OFS	4A1	[15:8]	CD
PI_DARRAY3_18_CS0_F0	DDR_PI_OFS	4A1	[23:16]	00
PI_DARRAY3_19_CS0_F0	DDR_PI_OFS	4A1	[31:24]	00
PI_DARRAY3_20_CS0_F0	DDR_PI_OFS	4A2	[7:0]	00
PI_DARRAY3_21_CS0_F0	DDR_PI_OFS	4A2	[15:8]	00
PI_DARRAY3_22_CS0_F0	DDR_PI_OFS	4A2	[23:16]	00
PI_DARRAY3_23_CS0_F0	DDR_PI_OFS	4A2	[31:24]	00
PI_DARRAY3_24_CS0_F0	DDR_PI_OFS	4A3	[7:0]	00
PI_DARRAY3_25_CS0_F0	DDR_PI_OFS	4A3	[15:8]	4D
PI_DARRAY3_26_CS0_F0	DDR_PI_OFS	4A3	[23:16]	00
PI_DARRAY3_27_CS0_F0	DDR_PI_OFS	4A3	[31:24]	00
PI_DARRAY3_28_CS0_F0	DDR_PI_OFS	4A4	[7:0]	00
PI_DARRAY3_29_CS0_F0	DDR_PI_OFS	4A4	[15:8]	00
PI_DARRAY3_30_CS0_F0	DDR_PI_OFS	4A4	[23:16]	00
PI_DARRAY3_31_CS0_F0	DDR_PI_OFS	4A4	[31:24]	00
PI_DARRAY3_32_CS0_F0	DDR_PI_OFS	4A5	[7:0]	00
PI_DARRAY3_33_CS0_F0	DDR_PI_OFS	4A5	[15:8]	00
PI_DARRAY3_34_CS0_F0	DDR_PI_OFS	4A5	[23:16]	00

		V4M		
Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PI_DARRAY3_35_CS0_F0	DDR_PI_OFS	4A5	[31:24]	00
PI_DARRAY3_36_CS0_F0	DDR_PI_OFS	4A6	[7:0]	00
PI_DARRAY3_37_CS0_F0	DDR_PI_OFS	4A6	[15:8]	00
PI_DARRAY3_38_CS0_F0	DDR_PI_OFS	4A6	[23:16]	00
PI_DARRAY3_39_CS0_F0	DDR_PI_OFS	4A6	[31:24]	00
PI_DARRAY3_0_CS0_F1	DDR_PI_OFS	4A7	[7:0]	24
PI_DARRAY3_1_CS0_F1	DDR_PI_OFS	4A7	[15:8]	52
PI_DARRAY3_2_CS0_F1	DDR_PI_OFS	4A7	[23:16]	F1
PI_DARRAY3_3_CS0_F1	DDR_PI_OFS	4A7	[31:24]	00
PI_DARRAY3_4_CS0_F1	DDR_PI_OFS	4A8	[7:0]	44
PI_DARRAY3_5_CS0_F1	DDR_PI_OFS	4A8	[15:8]	19
PI_DARRAY3_6_CS0_F1	DDR_PI_OFS	4A8	[23:16]	00
PI_DARRAY3_7_CS0_F1	DDR_PI_OFS	4A8	[31:24]	1C
PI_DARRAY3_8_CS0_F1	DDR_PI_OFS	4A9	[7:0]	00
PI_DARRAY3_9_CS0_F1	DDR_PI_OFS	4A9	[15:8]	00
PI_DARRAY3_10_CS0_F1	DDR_PI_OFS	4A9	[23:16]	00
PI_DARRAY3_11_CS0_F1	DDR_PI_OFS	4A9	[31:24]	00
PI_DARRAY3_12_CS0_F1	DDR_PI_OFS	4AA	[7:0]	00
PI_DARRAY3_13_CS0_F1	DDR_PI_OFS	4AA	[15:8]	00
PI_DARRAY3_14_CS0_F1	DDR_PI_OFS	4AA	[23:16]	06
PI_DARRAY3_15_CS0_F1	DDR_PI_OFS	4AA	[31:24]	00
PI_DARRAY3_16_CS0_F1	DDR_PI_OFS	4AB	[7:0]	00
PI_DARRAY3_17_CS0_F1	DDR_PI_OFS	4AB	[15:8]	CD
PI_DARRAY3_18_CS0_F1	DDR_PI_OFS	4AB	[23:16]	00
PI_DARRAY3_19_CS0_F1	DDR_PI_OFS	4AB	[31:24]	00
PI_DARRAY3_20_CS0_F1	DDR_PI_OFS	4AC	[7:0]	00
PI_DARRAY3_21_CS0_F1	DDR_PI_OFS	4AC	[15:8]	00
PI_DARRAY3_22_CS0_F1	DDR_PI_OFS	4AC	[23:16]	00
PI_DARRAY3_23_CS0_F1	DDR_PI_OFS	4AC	[31:24]	00
PI_DARRAY3_24_CS0_F1	DDR_PI_OFS	4AD	[7:0]	00
PI_DARRAY3_25_CS0_F1	DDR_PI_OFS	4AD	[15:8]	4D
PI_DARRAY3_26_CS0_F1	DDR_PI_OFS	4AD	[23:16]	00
PI_DARRAY3_27_CS0_F1	DDR_PI_OFS	4AD	[31:24]	00
PI_DARRAY3_28_CS0_F1	DDR_PI_OFS	4AE	[7:0]	00
PI_DARRAY3_29_CS0_F1	DDR_PI_OFS	4AE	[15:8]	00
PI_DARRAY3_30_CS0_F1	DDR_PI_OFS	4AE	[23:16]	00
PI_DARRAY3_31_CS0_F1	DDR_PI_OFS	4AE	[31:24]	00
PI_DARRAY3_32_CS0_F1	DDR_PI_OFS	4AF	[7:0]	00
PI_DARRAY3_33_CS0_F1	DDR_PI_OFS	4AF	[15:8]	00
PI_DARRAY3_34_CS0_F1	DDR_PI_OFS	4AF	[23:16]	00
PI_DARRAY3_35_CS0_F1	DDR_PI_OFS	4AF	[31:24]	00
PI_DARRAY3_36_CS0_F1	DDR_PI_OFS	4B0	[7:0]	00
PI_DARRAY3_37_CS0_F1	DDR_PI_OFS	4B0	[15:8]	00
PI_DARRAY3_38_CS0_F1	DDR_PI_OFS	4B0	[23:16]	00

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Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PI_DARRAY3_39_CS0_F1	DDR_PI_OFS	4B0	[31:24]	00
PI_DARRAY3_0_CS0_F2	DDR_PI_OFS	4B1	[7:0]	74
PI_DARRAY3_1_CS0_F2	DDR_PI_OFS	4B1	[15:8]	3F
PI_DARRAY3_2_CS0_F2	DDR_PI_OFS	4B1	[23:16]	F1
PI_DARRAY3_3_CS0_F2	DDR_PI_OFS	4B1	[31:24]	00
PI_DARRAY3_4_CS0_F2	DDR_PI_OFS	4B2	[7:0]	44
PI_DARRAY3_5_CS0_F2	DDR_PI_OFS	4B2	[15:8]	19
PI_DARRAY3_6_CS0_F2	DDR_PI_OFS	4B2	[23:16]	00
PI_DARRAY3_7_CS0_F2	DDR_PI_OFS	4B2	[31:24]	1C
PI_DARRAY3_8_CS0_F2	DDR_PI_OFS	4B3	[7:0]	00
PI_DARRAY3_9_CS0_F2	DDR_PI_OFS	4B3	[15:8]	00
PI_DARRAY3_10_CS0_F2	DDR_PI_OFS	4B3	[23:16]	00
PI_DARRAY3_11_CS0_F2	DDR_PI_OFS	4B3	[31:24]	00
PI_DARRAY3_12_CS0_F2	DDR_PI_OFS	4B4	[7:0]	00
PI_DARRAY3_13_CS0_F2	DDR_PI_OFS	4B4	[15:8]	00
PI_DARRAY3_14_CS0_F2	DDR_PI_OFS	4B4	[23:16]	06
PI_DARRAY3_15_CS0_F2	DDR_PI_OFS	4B4	[31:24]	00
PI_DARRAY3_16_CS0_F2	DDR_PI_OFS	4B5	[7:0]	00
PI_DARRAY3_17_CS0_F2	DDR_PI_OFS	4B5	[15:8]	CD
PI_DARRAY3_18_CS0_F2	DDR_PI_OFS	4B5	[23:16]	00
PI_DARRAY3_19_CS0_F2	DDR_PI_OFS	4B5	[31:24]	00
PI_DARRAY3_20_CS0_F2	DDR_PI_OFS	4B6	[7:0]	00
PI_DARRAY3_21_CS0_F2	DDR_PI_OFS	4B6	[15:8]	00
PI_DARRAY3_22_CS0_F2	DDR_PI_OFS	4B6	[23:16]	00
PI_DARRAY3_23_CS0_F2	DDR_PI_OFS	4B6	[31:24]	00
PI_DARRAY3_24_CS0_F2	DDR_PI_OFS	4B7	[7:0]	00
PI_DARRAY3_25_CS0_F2	DDR_PI_OFS	4B7	[15:8]	4D
PI_DARRAY3_26_CS0_F2	DDR_PI_OFS	4B7	[23:16]	00
PI_DARRAY3_27_CS0_F2	DDR_PI_OFS	4B7	[31:24]	00
PI_DARRAY3_28_CS0_F2	DDR_PI_OFS	4B8	[7:0]	00
PI_DARRAY3_29_CS0_F2	DDR_PI_OFS	4B8	[15:8]	00
PI_DARRAY3_30_CS0_F2	DDR_PI_OFS	4B8	[23:16]	00
PI_DARRAY3_31_CS0_F2	DDR_PI_OFS	4B8	[31:24]	00
PI_DARRAY3_32_CS0_F2	DDR_PI_OFS	4B9	[7:0]	00
PI_DARRAY3_33_CS0_F2	DDR_PI_OFS	4B9	[15:8]	00
PI_DARRAY3_34_CS0_F2	DDR_PI_OFS	4B9	[23:16]	00
PI_DARRAY3_35_CS0_F2	DDR_PI_OFS	4B9	[31:24]	00
PI_DARRAY3_36_CS0_F2	DDR_PI_OFS	4BA	[7:0]	00
PI_DARRAY3_37_CS0_F2	DDR_PI_OFS	4BA	[15:8]	00
PI_DARRAY3_38_CS0_F2	DDR_PI_OFS	4BA	[23:16]	00
PI_DARRAY3_39_CS0_F2	DDR_PI_OFS	4BA	[31:24]	00
PI_DARRAY3_0_CS1_F0	DDR_PI_OFS	4BB	[7:0]	04
PI_DARRAY3_1_CS1_F0	DDR_PI_OFS	4BB	[15:8]	00
PI_DARRAY3_2_CS1_F0	DDR_PI_OFS	4BB	[23:16]	F1

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Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PI_DARRAY3_3_CS1_F0	DDR_PI_OFS	4BB	[31:24]	00
PI_DARRAY3_4_CS1_F0	DDR_PI_OFS	4BC	[7:0]	00
PI_DARRAY3_5_CS1_F0	DDR_PI_OFS	4BC	[15:8]	5D
PI_DARRAY3_6_CS1_F0	DDR_PI_OFS	4BC	[23:16]	00
PI_DARRAY3_7_CS1_F0	DDR_PI_OFS	4BC	[31:24]	5D
PI_DARRAY3_8_CS1_F0	DDR_PI_OFS	4BD	[7:0]	00
PI_DARRAY3_9_CS1_F0	DDR_PI_OFS	4BD	[15:8]	00
PI_DARRAY3_10_CS1_F0	DDR_PI_OFS	4BD	[23:16]	00
PI_DARRAY3_11_CS1_F0	DDR_PI_OFS	4BD	[31:24]	00
PI_DARRAY3_12_CS1_F0	DDR_PI_OFS	4BE	[7:0]	00
PI_DARRAY3_13_CS1_F0	DDR_PI_OFS	4BE	[15:8]	00
PI_DARRAY3_14_CS1_F0	DDR_PI_OFS	4BE	[23:16]	00
PI_DARRAY3_15_CS1_F0	DDR_PI_OFS	4BE	[31:24]	00
PI_DARRAY3_16_CS1_F0	DDR_PI_OFS	4BF	[7:0]	00
PI_DARRAY3_17_CS1_F0	DDR_PI_OFS	4BF	[15:8]	CD
PI_DARRAY3_18_CS1_F0	DDR_PI_OFS	4BF	[23:16]	00
PI_DARRAY3_19_CS1_F0	DDR_PI_OFS	4BF	[31:24]	00
PI_DARRAY3_20_CS1_F0	DDR_PI_OFS	4C0	[7:0]	00
PI_DARRAY3_21_CS1_F0	DDR_PI_OFS	4C0	[15:8]	00
PI_DARRAY3_22_CS1_F0	DDR_PI_OFS	4C0	[23:16]	00
PI_DARRAY3_23_CS1_F0	DDR_PI_OFS	4C0	[31:24]	00
PI_DARRAY3_24_CS1_F0	DDR_PI_OFS	4C1	[7:0]	00
PI_DARRAY3_25_CS1_F0	DDR_PI_OFS	4C1	[15:8]	4D
PI_DARRAY3_26_CS1_F0	DDR_PI_OFS	4C1	[23:16]	00
PI_DARRAY3_27_CS1_F0	DDR_PI_OFS	4C1	[31:24]	00
PI_DARRAY3_28_CS1_F0	DDR_PI_OFS	4C2	[7:0]	00
PI_DARRAY3_29_CS1_F0	DDR_PI_OFS	4C2	[15:8]	00
PI_DARRAY3_30_CS1_F0	DDR_PI_OFS	4C2	[23:16]	00
PI_DARRAY3_31_CS1_F0	DDR_PI_OFS	4C2	[31:24]	00
PI_DARRAY3_32_CS1_F0	DDR_PI_OFS	4C3	[7:0]	00
PI_DARRAY3_33_CS1_F0	DDR_PI_OFS	4C3	[15:8]	00
PI_DARRAY3_34_CS1_F0	DDR_PI_OFS	4C3	[23:16]	00
PI_DARRAY3_35_CS1_F0	DDR_PI_OFS	4C3	[31:24]	00
PI_DARRAY3_36_CS1_F0	DDR_PI_OFS	4C4	[7:0]	00
PI_DARRAY3_37_CS1_F0	DDR_PI_OFS	4C4	[15:8]	00
PI_DARRAY3_38_CS1_F0	DDR_PI_OFS	4C4	[23:16]	00
PI_DARRAY3_39_CS1_F0	DDR_PI_OFS	4C4	[31:24]	00
PI_DARRAY3_0_CS1_F1	DDR_PI_OFS	4C5	[7:0]	24
PI_DARRAY3_1_CS1_F1	DDR_PI_OFS	4C5	[15:8]	52
PI_DARRAY3_2_CS1_F1	DDR_PI_OFS	4C5	[23:16]	F1
PI_DARRAY3_3_CS1_F1	DDR_PI_OFS	4C5	[31:24]	00
PI_DARRAY3_4_CS1_F1	DDR_PI_OFS	4C6	[7:0]	44
PI_DARRAY3_5_CS1_F1	DDR_PI_OFS	4C6	[15:8]	19
PI_DARRAY3_6_CS1_F1	DDR_PI_OFS	4C6	[23:16]	00

		V4M		
Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PI_DARRAY3_7_CS1_F1	DDR_PI_OFS	4C6	[31:24]	1C
PI_DARRAY3_8_CS1_F1	DDR_PI_OFS	4C7	[7:0]	00
PI_DARRAY3_9_CS1_F1	DDR_PI_OFS	4C7	[15:8]	00
PI_DARRAY3_10_CS1_F1	DDR_PI_OFS	4C7	[23:16]	00
PI_DARRAY3_11_CS1_F1	DDR_PI_OFS	4C7	[31:24]	00
PI_DARRAY3_12_CS1_F1	DDR_PI_OFS	4C8	[7:0]	00
PI_DARRAY3_13_CS1_F1	DDR_PI_OFS	4C8	[15:8]	00
PI_DARRAY3_14_CS1_F1	DDR_PI_OFS	4C8	[23:16]	2E
PI_DARRAY3_15_CS1_F1	DDR_PI_OFS	4C8	[31:24]	00
PI_DARRAY3_16_CS1_F1	DDR_PI_OFS	4C9	[7:0]	00
PI_DARRAY3_17_CS1_F1	DDR_PI_OFS	4C9	[15:8]	CD
PI_DARRAY3_18_CS1_F1	DDR_PI_OFS	4C9	[23:16]	00
PI_DARRAY3_19_CS1_F1	DDR_PI_OFS	4C9	[31:24]	00
PI_DARRAY3_20_CS1_F1	DDR_PI_OFS	4CA	[7:0]	00
PI_DARRAY3_21_CS1_F1	DDR_PI_OFS	4CA	[15:8]	00
PI_DARRAY3_22_CS1_F1	DDR_PI_OFS	4CA	[23:16]	00
PI_DARRAY3_23_CS1_F1	DDR_PI_OFS	4CA	[31:24]	00
PI_DARRAY3_24_CS1_F1	DDR_PI_OFS	4CB	[7:0]	00
PI_DARRAY3_25_CS1_F1	DDR_PI_OFS	4CB	[15:8]	4D
PI_DARRAY3_26_CS1_F1	DDR_PI_OFS	4CB	[23:16]	00
PI_DARRAY3_27_CS1_F1	DDR_PI_OFS	4CB	[31:24]	00
PI_DARRAY3_28_CS1_F1	DDR_PI_OFS	4CC	[7:0]	00
PI_DARRAY3_29_CS1_F1	DDR_PI_OFS	4CC	[15:8]	00
PI_DARRAY3_30_CS1_F1	DDR_PI_OFS	4CC	[23:16]	00
PI_DARRAY3_31_CS1_F1	DDR_PI_OFS	4CC	[31:24]	00
PI_DARRAY3_32_CS1_F1	DDR_PI_OFS	4CD	[7:0]	00
PI_DARRAY3_33_CS1_F1	DDR_PI_OFS	4CD	[15:8]	00
PI_DARRAY3_34_CS1_F1	DDR_PI_OFS	4CD	[23:16]	00
PI_DARRAY3_35_CS1_F1	DDR_PI_OFS	4CD	[31:24]	00
PI_DARRAY3_36_CS1_F1	DDR_PI_OFS	4CE	[7:0]	00
PI_DARRAY3_37_CS1_F1	DDR_PI_OFS	4CE	[15:8]	00
PI_DARRAY3_38_CS1_F1	DDR_PI_OFS	4CE	[23:16]	00
PI_DARRAY3_39_CS1_F1	DDR_PI_OFS	4CE	[31:24]	00
PI_DARRAY3_0_CS1_F2	DDR_PI_OFS	4CF	[7:0]	74
PI_DARRAY3_1_CS1_F2	DDR_PI_OFS	4CF	[15:8]	3F
PI_DARRAY3_2_CS1_F2	DDR_PI_OFS	4CF	[23:16]	F1
PI_DARRAY3_3_CS1_F2	DDR_PI_OFS	4CF	[31:24]	00
PI_DARRAY3_4_CS1_F2	DDR_PI_OFS	4D0	[7:0]	44
PI_DARRAY3_5_CS1_F2	DDR_PI_OFS	4D0	[15:8]	19
PI_DARRAY3_6_CS1_F2	DDR_PI_OFS	4D0	[23:16]	00
PI_DARRAY3_7_CS1_F2	DDR_PI_OFS	4D0	[31:24]	1C
PI_DARRAY3_8_CS1_F2	DDR_PI_OFS	4D1	[7:0]	00
PI_DARRAY3_9_CS1_F2	DDR_PI_OFS	4D1	[15:8]	00
PI_DARRAY3_10_CS1_F2	DDR_PI_OFS	4D1	[23:16]	00

		V4M		
Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PI_DARRAY3_11_CS1_F2	DDR_PI_OFS	4D1	[31:24]	00
PI_DARRAY3_12_CS1_F2	DDR_PI_OFS	4D2	[7:0]	00
PI_DARRAY3_13_CS1_F2	DDR_PI_OFS	4D2	[15:8]	00
PI_DARRAY3_14_CS1_F2	DDR_PI_OFS	4D2	[23:16]	2E
PI_DARRAY3_15_CS1_F2	DDR_PI_OFS	4D2	[31:24]	00
PI_DARRAY3_16_CS1_F2	DDR_PI_OFS	4D3	[7:0]	00
PI_DARRAY3_17_CS1_F2	DDR_PI_OFS	4D3	[15:8]	CD
PI_DARRAY3_18_CS1_F2	DDR_PI_OFS	4D3	[23:16]	00
PI_DARRAY3_19_CS1_F2	DDR_PI_OFS	4D3	[31:24]	00
PI_DARRAY3_20_CS1_F2	DDR_PI_OFS	4D4	[7:0]	00
PI_DARRAY3_21_CS1_F2	DDR_PI_OFS	4D4	[15:8]	00
PI_DARRAY3_22_CS1_F2	DDR_PI_OFS	4D4	[23:16]	00
PI_DARRAY3_23_CS1_F2	DDR_PI_OFS	4D4	[31:24]	00
PI_DARRAY3_24_CS1_F2	DDR_PI_OFS	4D5	[7:0]	00
PI_DARRAY3_25_CS1_F2	DDR_PI_OFS	4D5	[15:8]	4D
PI_DARRAY3_26_CS1_F2	DDR_PI_OFS	4D5	[23:16]	00
PI_DARRAY3_27_CS1_F2	DDR_PI_OFS	4D5	[31:24]	00
PI_DARRAY3_28_CS1_F2	DDR_PI_OFS	4D6	[7:0]	00
PI_DARRAY3_29_CS1_F2	DDR_PI_OFS	4D6	[15:8]	00
PI_DARRAY3_30_CS1_F2	DDR_PI_OFS	4D6	[23:16]	00
PI_DARRAY3_31_CS1_F2	DDR_PI_OFS	4D6	[31:24]	00
PI_DARRAY3_32_CS1_F2	DDR_PI_OFS	4D7	[7:0]	00
PI_DARRAY3_33_CS1_F2	DDR_PI_OFS	4D7	[15:8]	00
PI_DARRAY3_34_CS1_F2	DDR_PI_OFS	4D7	[23:16]	00
PI_DARRAY3_35_CS1_F2	DDR_PI_OFS	4D7	[31:24]	00
PI_DARRAY3_36_CS1_F2	DDR_PI_OFS	4D8	[7:0]	00
PI_DARRAY3_37_CS1_F2	DDR_PI_OFS	4D8	[15:8]	00
PI_DARRAY3_38_CS1_F2	DDR_PI_OFS	4D8	[23:16]	00
PI_DARRAY3_39_CS1_F2	DDR_PI_OFS	4D8	[31:24]	00
PI_DARRAY0_0_MAP	DDR_PI_OFS	4D9	[13:0]	2000
PI_DARRAY0_1_MAP	DDR_PI_OFS	4D9	[29:16]	2000
PI_DARRAY0_2_MAP	DDR_PI_OFS	4DA	[13:0]	2000
PI_DARRAY0_3_MAP	DDR_PI_OFS	4DA	[29:16]	000A
PI_DARRAY0_4_MAP	DDR_PI_OFS	4DB	[13:0]	2000
PI_DARRAY0_5_MAP	DDR_PI_OFS	4DB	[29:16]	2000
PI_DARRAY0_6_MAP	DDR_PI_OFS	4DC	[13:0]	2000
PI_DARRAY0_7_MAP	DDR_PI_OFS	4DC	[29:16]	2000
PI_DARRAY0_8_MAP	DDR_PI_OFS	4DD	[13:0]	000F
PI_DARRAY0_9_MAP	DDR_PI_OFS	4DD	[29:16]	0010
PI_DARRAY0_10_MAP	DDR_PI_OFS	4DE	[13:0]	0011
PI_DARRAY0_11_MAP	DDR_PI_OFS	4DE	[29:16]	0012
PI_DARRAY0_12_MAP	DDR_PI_OFS	4DF	[13:0]	0013
PI_DARRAY0_13_MAP	DDR_PI_OFS	4DF	[29:16]	0014
PI_DARRAY0_14_MAP	DDR_PI_OFS	4E0	[13:0]	2000

		V4M		
Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PI_DARRAY0_15_MAP	DDR_PI_OFS	4E0	[29:16]	0017
PI_DARRAY0_16_MAP	DDR_PI_OFS	4E1	[13:0]	2000
PI_DARRAY0_17_MAP	DDR_PI_OFS	4E1	[29:16]	2000
PI_DARRAY0_18_MAP	DDR_PI_OFS	4E2	[13:0]	2000
PI_DARRAY0_19_MAP	DDR_PI_OFS	4E2	[29:16]	2000
PI_DARRAY0_20_MAP	DDR_PI_OFS	4E3	[13:0]	2000
PI_DARRAY0_21_MAP	DDR_PI_OFS	4E3	[29:16]	0020
PI_DARRAY0_22_MAP	DDR_PI_OFS	4E4	[13:0]	2000
PI_DARRAY0_23_MAP	DDR_PI_OFS	4E4	[29:16]	2000
PI_DARRAY0_24_MAP	DDR_PI_OFS	4E5	[13:0]	0028
PI_DARRAY0_25_MAP	DDR_PI_OFS	4E5	[29:16]	2000
PI_DARRAY0_26_MAP	DDR_PI_OFS	4E6	[13:0]	2000
PI_DARRAY0_27_MAP	DDR_PI_OFS	4E6	[29:16]	2000
PI_DARRAY0_28_MAP	DDR_PI_OFS	4E7	[13:0]	2000
PI_DARRAY0_29_MAP	DDR_PI_OFS	4E7	[29:16]	2000
PI_DARRAY0_30_MAP	DDR_PI_OFS	4E8	[13:0]	2000
PI_DARRAY0_31_MAP	DDR_PI_OFS	4E8	[29:16]	2000
PI_DARRAY0_32_MAP	DDR_PI_OFS	4E9	[13:0]	2000
PI_DARRAY0_33_MAP	DDR_PI_OFS	4E9	[29:16]	2000
PI_DARRAY0_34_MAP	DDR_PI_OFS	4EA	[13:0]	2000
PI_DARRAY0_35_MAP	DDR_PI_OFS	4EA	[29:16]	2000
PI_DARRAY0_36_MAP	DDR_PI_OFS	4EB	[13:0]	2000
PI_DARRAY0_37_MAP	DDR_PI_OFS	4EB	[29:16]	2000
PI_DARRAY0_38_MAP	DDR_PI_OFS	4EC	[13:0]	2000
PI_DARRAY0_39_MAP	DDR_PI_OFS	4EC	[29:16]	2000
PI_DARRAY0_40_MAP	DDR_PI_OFS	4ED	[13:0]	2000
PI_DARRAY0_41_MAP	DDR_PI_OFS	4ED	[29:16]	2000
PI_DARRAY0_42_MAP	DDR_PI_OFS	4EE	[13:0]	2000
PI_DARRAY0_43_MAP	DDR_PI_OFS	4EE	[29:16]	2000
PI_DARRAY0_44_MAP	DDR_PI_OFS	4EF	[13:0]	2000
PI_DARRAY0_45_MAP	DDR_PI_OFS	4EF	[29:16]	2000
PI_DARRAY0_46_MAP	DDR_PI_OFS	4F0	[13:0]	2000
PI_DARRAY0_47_MAP	DDR_PI_OFS	4F0	[29:16]	2000
PI_DARRAY0_48_MAP	DDR_PI_OFS	4F1	[13:0]	2000
PI_DARRAY0_49_MAP	DDR_PI_OFS	4F1	[29:16]	2000
PI_DARRAY0_50_MAP	DDR_PI_OFS	4F2	[13:0]	2000
PI_DARRAY0_51_MAP	DDR_PI_OFS	4F2	[29:16]	2000
PI_DARRAY0_52_MAP	DDR_PI_OFS	4F3	[13:0]	2000
PI_DARRAY0_53_MAP	DDR_PI_OFS	4F3	[29:16]	2000
PI_DARRAY0_54_MAP	DDR_PI_OFS	4F4	[13:0]	2000
PI_DARRAY0_55_MAP	DDR_PI_OFS	4F4	[29:16]	2000
PI_DARRAY0_56_MAP	DDR_PI_OFS	4F5	[13:0]	2000
PI_DARRAY0_57_MAP	DDR_PI_OFS	4F5	[29:16]	2000
PI_DARRAY0_58_MAP	DDR_PI_OFS	4F6	[13:0]	2000

		V4M		
Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PI_DARRAY0_59_MAP	DDR_PI_OFS	4F6	[29:16]	2000
PI_DARRAY0_60_MAP	DDR_PI_OFS	4F7	[13:0]	2000
PI_DARRAY0_61_MAP	DDR_PI_OFS	4F7	[29:16]	2000
PI_DARRAY0_62_MAP	DDR_PI_OFS	4F8	[13:0]	2000
PI_DARRAY0_63_MAP	DDR_PI_OFS	4F8	[29:16]	2000
PI_DARRAY0_64_MAP	DDR_PI_OFS	4F9	[13:0]	2000
PI_DARRAY0_65_MAP	DDR_PI_OFS	4F9	[29:16]	2000
PI_DARRAY0_66_MAP	DDR_PI_OFS	4FA	[13:0]	2000
PI_DARRAY0_67_MAP	DDR_PI_OFS	4FA	[29:16]	2000
PI_DARRAY0_68_MAP	DDR_PI_OFS	4FB	[13:0]	2000
PI_DARRAY0_69_MAP	DDR_PI_OFS	4FB	[29:16]	2000
PI_DARRAY0_70_MAP	DDR_PI_OFS	4FC	[13:0]	2000
PI_DARRAY0_71_MAP	DDR_PI_OFS	4FC	[29:16]	2000
PI_DARRAY0_72_MAP	DDR_PI_OFS	4FD	[13:0]	2000
PI_DARRAY0_73_MAP	DDR_PI_OFS	4FD	[29:16]	2000
PI_DARRAY0_74_MAP	DDR_PI_OFS	4FE	[13:0]	2000
PI_DARRAY0_75_MAP	DDR_PI_OFS	4FE	[29:16]	2000
PI_DARRAY0_76_MAP	DDR_PI_OFS	4FF	[13:0]	2000
PI_DARRAY0_77_MAP	DDR_PI_OFS	4FF	[29:16]	2000
PI_DARRAY0_78_MAP	DDR_PI_OFS	500	[13:0]	2000
PI_DARRAY0_79_MAP	DDR_PI_OFS	500	[29:16]	2000
PI_DARRAY3_0_MAP	DDR_PI_OFS	501	[13:0]	0001
PI_DARRAY3_1_MAP	DDR_PI_OFS	501	[29:16]	0002
PI_DARRAY3_2_MAP	DDR_PI_OFS	502	[13:0]	0003
PI_DARRAY3_3_MAP	DDR_PI_OFS	502	[29:16]	2000
PI_DARRAY3_4_MAP	DDR_PI_OFS	503	[13:0]	000B
PI_DARRAY3_5_MAP	DDR_PI_OFS	503	[29:16]	000C
PI_DARRAY3_6_MAP	DDR_PI_OFS	504	[13:0]	000D
PI_DARRAY3_7_MAP	DDR_PI_OFS	504	[29:16]	000E
PI_DARRAY3_8_MAP	DDR_PI_OFS	505	[13:0]	2000
PI_DARRAY3_9_MAP	DDR_PI_OFS	505	[29:16]	2000
PI_DARRAY3_10_MAP	DDR_PI_OFS	506	[13:0]	2000
PI_DARRAY3_11_MAP	DDR_PI_OFS	506	[29:16]	2000
PI_DARRAY3_12_MAP	DDR_PI_OFS	507	[13:0]	2000
PI_DARRAY3_13_MAP	DDR_PI_OFS	507	[29:16]	2000
PI_DARRAY3_14_MAP	DDR_PI_OFS	508	[13:0]	0016
PI_DARRAY3_15_MAP	DDR_PI_OFS	508	[29:16]	2000
PI_DARRAY3_16_MAP	DDR_PI_OFS	509	[13:0]	2000
PI_DARRAY3_17_MAP	DDR_PI_OFS	509	[29:16]	100C
PI_DARRAY3_18_MAP	DDR_PI_OFS	50A	[13:0]	0000
PI_DARRAY3_19_MAP	DDR_PI_OFS	50A	[29:16]	0008
PI_DARRAY3_20_MAP	DDR_PI_OFS	50B	[13:0]	2000
PI_DARRAY3_21_MAP	DDR_PI_OFS	50B	[29:16]	2000
PI_DARRAY3_22_MAP	DDR_PI_OFS	50C	[13:0]	2000

		V4M		
Bit Name	**Address offset**	**n [hex]**	**Bit**	**Initial value [hex]**
PI_DARRAY3_23_MAP	DDR_PI_OFS	50C	[29:16]	2000
PI_DARRAY3_24_MAP	DDR_PI_OFS	50D	[13:0]	2000
PI_DARRAY3_25_MAP	DDR_PI_OFS	50D	[29:16]	100E
PI_DARRAY3_26_MAP	DDR_PI_OFS	50E	[13:0]	001F
PI_DARRAY3_27_MAP	DDR_PI_OFS	50E	[29:16]	2000
PI_DARRAY3_28_MAP	DDR_PI_OFS	50F	[13:0]	2000
PI_DARRAY3_29_MAP	DDR_PI_OFS	50F	[29:16]	2000
PI_DARRAY3_30_MAP	DDR_PI_OFS	510	[13:0]	2000
PI_DARRAY3_31_MAP	DDR_PI_OFS	510	[29:16]	2000
PI_DARRAY3_32_MAP	DDR_PI_OFS	511	[13:0]	2000
PI_DARRAY3_33_MAP	DDR_PI_OFS	511	[29:16]	2000
PI_DARRAY3_34_MAP	DDR_PI_OFS	512	[13:0]	2000
PI_DARRAY3_35_MAP	DDR_PI_OFS	512	[29:16]	2000
PI_DARRAY3_36_MAP	DDR_PI_OFS	513	[13:0]	2000
PI_DARRAY3_37_MAP	DDR_PI_OFS	513	[29:16]	2000
PI_DARRAY3_38_MAP	DDR_PI_OFS	514	[13:0]	2000
PI_DARRAY3_39_MAP	DDR_PI_OFS	514	[29:16]	2000

Table 5-4 Register Names, Addresses, and Initial Values

Register addresses are calculated in the same way as described in Table 5-3.

Register Name	Address Offset (_OFS)	n [hex] (_OFS + n)	V4M
DDR_PHY_SLICE_000	DDR_PHY_SLICE_OFS	0	0x30030370
DDR_PHY_SLICE_001	DDR_PHY_SLICE_OFS	1	0x00000000
DDR_PHY_SLICE_002	DDR_PHY_SLICE_OFS	2	0x01FF0002
DDR_PHY_SLICE_003	DDR_PHY_SLICE_OFS	3	0x00010003
DDR_PHY_SLICE_004	DDR_PHY_SLICE_OFS	4	0x00000000
DDR_PHY_SLICE_005	DDR_PHY_SLICE_OFS	5	0x00000000
DDR_PHY_SLICE_006	DDR_PHY_SLICE_OFS	6	0x01030000
DDR_PHY_SLICE_007	DDR_PHY_SLICE_OFS	7	0x00010000
DDR_PHY_SLICE_008	DDR_PHY_SLICE_OFS	8	0x01030004
DDR_PHY_SLICE_009	DDR_PHY_SLICE_OFS	9	0x00000000
DDR_PHY_SLICE_010	DDR_PHY_SLICE_OFS	A	0x00000001
DDR_PHY_SLICE_011	DDR_PHY_SLICE_OFS	B	0x00000000
DDR_PHY_SLICE_012	DDR_PHY_SLICE_OFS	C	0x00000000
DDR_PHY_SLICE_013	DDR_PHY_SLICE_OFS	D	0x00010000
DDR_PHY_SLICE_014	DDR_PHY_SLICE_OFS	E	0x08010000
DDR_PHY_SLICE_015	DDR_PHY_SLICE_OFS	F	0x00002002
DDR_PHY_SLICE_016	DDR_PHY_SLICE_OFS	10	0x00000000
DDR_PHY_SLICE_017	DDR_PHY_SLICE_OFS	11	0x040F0100
DDR_PHY_SLICE_018	DDR_PHY_SLICE_OFS	12	0x1404034F
DDR_PHY_SLICE_019	DDR_PHY_SLICE_OFS	13	0x04020102
DDR_PHY_SLICE_020	DDR_PHY_SLICE_OFS	14	0x10040404
DDR_PHY_SLICE_021	DDR_PHY_SLICE_OFS	15	0x00000000
DDR_PHY_SLICE_022	DDR_PHY_SLICE_OFS	16	0x00000000
DDR_PHY_SLICE_023	DDR_PHY_SLICE_OFS	17	0x00FF0000
DDR_PHY_SLICE_024	DDR_PHY_SLICE_OFS	18	0x18CE0008
DDR_PHY_SLICE_025	DDR_PHY_SLICE_OFS	19	0x0000000F
DDR_PHY_SLICE_026	DDR_PHY_SLICE_OFS	1A	0x00000000
DDR_PHY_SLICE_027	DDR_PHY_SLICE_OFS	1B	0x00000001
DDR_PHY_SLICE_028	DDR_PHY_SLICE_OFS	1C	0x00060000
DDR_PHY_SLICE_029	DDR_PHY_SLICE_OFS	1D	0x00000000
DDR_PHY_SLICE_030	DDR_PHY_SLICE_OFS	1E	0x00000000
DDR_PHY_SLICE_031	DDR_PHY_SLICE_OFS	1F	0x00000000
DDR_PHY_SLICE_032	DDR_PHY_SLICE_OFS	20	0x00080840
DDR_PHY_SLICE_033	DDR_PHY_SLICE_OFS	21	0x08040000
DDR_PHY_SLICE_034	DDR_PHY_SLICE_OFS	22	0x00000004
DDR_PHY_SLICE_035	DDR_PHY_SLICE_OFS	23	0x00401030
DDR_PHY_SLICE_036	DDR_PHY_SLICE_OFS	24	0x0200000C
DDR_PHY_SLICE_037	DDR_PHY_SLICE_OFS	25	0x00000020
DDR_PHY_SLICE_038	DDR_PHY_SLICE_OFS	26	0x00000101

Register Name	Address Offset (_OFS)	n [hex] (_OFS + n)	V4M
DDR_PHY_SLICE_039	DDR_PHY_SLICE_OFS	27	0x00000000
DDR_PHY_SLICE_040	DDR_PHY_SLICE_OFS	28	0x00000000
DDR_PHY_SLICE_041	DDR_PHY_SLICE_OFS	29	0x00000000
DDR_PHY_SLICE_042	DDR_PHY_SLICE_OFS	2A	0x00000000
DDR_PHY_SLICE_043	DDR_PHY_SLICE_OFS	2B	0x00000000
DDR_PHY_SLICE_044	DDR_PHY_SLICE_OFS	2C	0x00000000
DDR_PHY_SLICE_045	DDR_PHY_SLICE_OFS	2D	0x00000000
DDR_PHY_SLICE_046	DDR_PHY_SLICE_OFS	2E	0x00000000
DDR_PHY_SLICE_047	DDR_PHY_SLICE_OFS	2F	0x00000000
DDR_PHY_SLICE_048	DDR_PHY_SLICE_OFS	30	0x00000000
DDR_PHY_SLICE_049	DDR_PHY_SLICE_OFS	31	0x00000000
DDR_PHY_SLICE_050	DDR_PHY_SLICE_OFS	32	0x00000000
DDR_PHY_SLICE_051	DDR_PHY_SLICE_OFS	33	0x00000030
DDR_PHY_SLICE_052	DDR_PHY_SLICE_OFS	34	0x00000000
DDR_PHY_SLICE_053	DDR_PHY_SLICE_OFS	35	0x00000000
DDR_PHY_SLICE_054	DDR_PHY_SLICE_OFS	36	0x00000000
DDR_PHY_SLICE_055	DDR_PHY_SLICE_OFS	37	0x00000000
DDR_PHY_SLICE_056	DDR_PHY_SLICE_OFS	38	0x00000000
DDR_PHY_SLICE_057	DDR_PHY_SLICE_OFS	39	0x00000000
DDR_PHY_SLICE_058	DDR_PHY_SLICE_OFS	3A	0x00000000
DDR_PHY_SLICE_059	DDR_PHY_SLICE_OFS	3B	0x00000000
DDR_PHY_SLICE_060	DDR_PHY_SLICE_OFS	3C	0x00000000
DDR_PHY_SLICE_061	DDR_PHY_SLICE_OFS	3D	0x00000104
DDR_PHY_SLICE_062	DDR_PHY_SLICE_OFS	3E	0x001F07FF
DDR_PHY_SLICE_063	DDR_PHY_SLICE_OFS	3F	0x00800800
DDR_PHY_SLICE_064	DDR_PHY_SLICE_OFS	40	0x00061020
DDR_PHY_SLICE_065	DDR_PHY_SLICE_OFS	41	0x04010000
DDR_PHY_SLICE_066	DDR_PHY_SLICE_OFS	42	0x00000000
DDR_PHY_SLICE_067	DDR_PHY_SLICE_OFS	43	0xCE020001
DDR_PHY_SLICE_068	DDR_PHY_SLICE_OFS	44	0x00000007
DDR_PHY_SLICE_069	DDR_PHY_SLICE_OFS	45	0x00017706
DDR_PHY_SLICE_070	DDR_PHY_SLICE_OFS	46	0x00037706
DDR_PHY_SLICE_071	DDR_PHY_SLICE_OFS	47	0x00000000
DDR_PHY_SLICE_072	DDR_PHY_SLICE_OFS	48	0x008C006C
DDR_PHY_SLICE_073	DDR_PHY_SLICE_OFS	49	0x00100001
DDR_PHY_SLICE_074	DDR_PHY_SLICE_OFS	4A	0x03FF0100
DDR_PHY_SLICE_075	DDR_PHY_SLICE_OFS	4B	0x00006E01
DDR_PHY_SLICE_076	DDR_PHY_SLICE_OFS	4C	0x00000301
DDR_PHY_SLICE_077	DDR_PHY_SLICE_OFS	4D	0x00000000
DDR_PHY_SLICE_078	DDR_PHY_SLICE_OFS	4E	0x00000000
DDR_PHY_SLICE_079	DDR_PHY_SLICE_OFS	4F	0x00000000
DDR_PHY_SLICE_080	DDR_PHY_SLICE_OFS	50	0x00380038

Register Name	Address Offset (_OFS)	n [hex] (_OFS + n)	V4M
DDR_PHY_SLICE_081	DDR_PHY_SLICE_OFS	51	0x00380038
DDR_PHY_SLICE_082	DDR_PHY_SLICE_OFS	52	0x00380038
DDR_PHY_SLICE_083	DDR_PHY_SLICE_OFS	53	0x00380038
DDR_PHY_SLICE_084	DDR_PHY_SLICE_OFS	54	0x09000038
DDR_PHY_SLICE_085	DDR_PHY_SLICE_OFS	55	0x90510503
DDR_PHY_SLICE_086	DDR_PHY_SLICE_OFS	56	0x70006161
DDR_PHY_SLICE_087	DDR_PHY_SLICE_OFS	57	0x41C00531
DDR_PHY_SLICE_088	DDR_PHY_SLICE_OFS	58	0x26800064
DDR_PHY_SLICE_089	DDR_PHY_SLICE_OFS	59	0xC0010080
DDR_PHY_SLICE_090	DDR_PHY_SLICE_OFS	5A	0x010100C0
DDR_PHY_SLICE_091	DDR_PHY_SLICE_OFS	5B	0x000E0C01
DDR_PHY_SLICE_092	DDR_PHY_SLICE_OFS	5C	0x00030200
DDR_PHY_SLICE_093	DDR_PHY_SLICE_OFS	5D	0x42100010
DDR_PHY_SLICE_094	DDR_PHY_SLICE_OFS	5E	0x0106083E
DDR_PHY_SLICE_095	DDR_PHY_SLICE_OFS	5F	0x000F0627
DDR_PHY_SLICE_096	DDR_PHY_SLICE_OFS	60	0x00E600C8
DDR_PHY_SLICE_097	DDR_PHY_SLICE_OFS	61	0x01100140
DDR_PHY_SLICE_098	DDR_PHY_SLICE_OFS	62	0x00000000
DDR_PHY_SLICE_099	DDR_PHY_SLICE_OFS	63	0x0000019B
DDR_PHY_SLICE_100	DDR_PHY_SLICE_OFS	64	0x00000000
DDR_PHY_SLICE_101	DDR_PHY_SLICE_OFS	65	0x05000068
DDR_PHY_SLICE_102	DDR_PHY_SLICE_OFS	66	0x00000400
DDR_PHY_SLICE_103	DDR_PHY_SLICE_OFS	67	0x01400000
DDR_PHY_SLICE_104	DDR_PHY_SLICE_OFS	68	0x80800301
DDR_PHY_SLICE_105	DDR_PHY_SLICE_OFS	69	0x000E2210
DDR_PHY_SLICE_106	DDR_PHY_SLICE_OFS	6A	0x76543210
DDR_PHY_SLICE_107	DDR_PHY_SLICE_OFS	6B	0x00000008
DDR_PHY_SLICE_108	DDR_PHY_SLICE_OFS	6C	0x02500250
DDR_PHY_SLICE_109	DDR_PHY_SLICE_OFS	6D	0x02500250
DDR_PHY_SLICE_110	DDR_PHY_SLICE_OFS	6E	0x02500250
DDR_PHY_SLICE_111	DDR_PHY_SLICE_OFS	6F	0x02500250
DDR_PHY_SLICE_112	DDR_PHY_SLICE_OFS	70	0x02500250
DDR_PHY_SLICE_113	DDR_PHY_SLICE_OFS	71	0x00000000
DDR_PHY_SLICE_114	DDR_PHY_SLICE_OFS	72	0x00500050
DDR_PHY_SLICE_115	DDR_PHY_SLICE_OFS	73	0x00500050
DDR_PHY_SLICE_116	DDR_PHY_SLICE_OFS	74	0x00500050
DDR_PHY_SLICE_117	DDR_PHY_SLICE_OFS	75	0x00500050
DDR_PHY_SLICE_118	DDR_PHY_SLICE_OFS	76	0x00500050
DDR_PHY_SLICE_119	DDR_PHY_SLICE_OFS	77	0x00500050
DDR_PHY_SLICE_120	DDR_PHY_SLICE_OFS	78	0x00500050
DDR_PHY_SLICE_121	DDR_PHY_SLICE_OFS	79	0x00500050
DDR_PHY_SLICE_122	DDR_PHY_SLICE_OFS	7A	0x00500050

Register Name	Address Offset (_OFS)	n [hex] (_OFS + n)	V4M
DDR_PHY_SLICE_123	DDR_PHY_SLICE_OFS	7B	0x000500E1
DDR_PHY_SLICE_124	DDR_PHY_SLICE_OFS	7C	0x00000000
DDR_PHY_SLICE_125	DDR_PHY_SLICE_OFS	7D	0x0801000A
DDR_PHY_SLICE_126	DDR_PHY_SLICE_OFS	7E	0x00000000
DDR_PHY_SLICE_127	DDR_PHY_SLICE_OFS	7F	0x20202020
DDR_PHY_SLICE_128	DDR_PHY_SLICE_OFS	80	0x20202020
DDR_PHY_SLICE_129	DDR_PHY_SLICE_OFS	81	0x20202020
DDR_PHY_SLICE_130	DDR_PHY_SLICE_OFS	82	0x00000000
DDR_PHY_SLICE_131	DDR_PHY_SLICE_OFS	83	0x00000000
DDR_PHY_SLICE_132	DDR_PHY_SLICE_OFS	84	0x00000000
DDR_PHY_SLICE_133	DDR_PHY_SLICE_OFS	85	0x00000000
DDR_PHY_SLICE_134	DDR_PHY_SLICE_OFS	86	0x00000000
DDR_PHY_SLICE_135	DDR_PHY_SLICE_OFS	87	0x00000000
DDR_PHY_SLICE_136	DDR_PHY_SLICE_OFS	88	0x00000000
DDR_PHY_SLICE_137	DDR_PHY_SLICE_OFS	89	0x00000000
DDR_PHY_SLICE_138	DDR_PHY_SLICE_OFS	8A	0x00000000
DDR_PHY_SLICE_139	DDR_PHY_SLICE_OFS	8B	0x00000000
DDR_PHY_ADR_V_000	DDR_PHY_ADR_V_OFS	0	0x00400000
DDR_PHY_ADR_V_001	DDR_PHY_ADR_V_OFS	1	0x00202002
DDR_PHY_ADR_V_002	DDR_PHY_ADR_V_OFS	2	0x76543210
DDR_PHY_ADR_V_003	DDR_PHY_ADR_V_OFS	3	0x00010001
DDR_PHY_ADR_V_004	DDR_PHY_ADR_V_OFS	4	0x06543210
DDR_PHY_ADR_V_005	DDR_PHY_ADR_V_OFS	5	0x03060100
DDR_PHY_ADR_V_006	DDR_PHY_ADR_V_OFS	6	0x00001000
DDR_PHY_ADR_V_007	DDR_PHY_ADR_V_OFS	7	0x00000000
DDR_PHY_ADR_V_008	DDR_PHY_ADR_V_OFS	8	0x00000000
DDR_PHY_ADR_V_009	DDR_PHY_ADR_V_OFS	9	0x00000000
DDR_PHY_ADR_V_010	DDR_PHY_ADR_V_OFS	A	0x00000000
DDR_PHY_ADR_V_011	DDR_PHY_ADR_V_OFS	B	0x00000000
DDR_PHY_ADR_V_012	DDR_PHY_ADR_V_OFS	C	0x00000000
DDR_PHY_ADR_V_013	DDR_PHY_ADR_V_OFS	D	0x00000000
DDR_PHY_ADR_V_014	DDR_PHY_ADR_V_OFS	E	0x00000000
DDR_PHY_ADR_V_015	DDR_PHY_ADR_V_OFS	F	0x0000803F
DDR_PHY_ADR_V_016	DDR_PHY_ADR_V_OFS	10	0x00000001
DDR_PHY_ADR_V_017	DDR_PHY_ADR_V_OFS	11	0x00000003
DDR_PHY_ADR_V_018	DDR_PHY_ADR_V_OFS	12	0x00000000
DDR_PHY_ADR_V_019	DDR_PHY_ADR_V_OFS	13	0x000F0000
DDR_PHY_ADR_V_020	DDR_PHY_ADR_V_OFS	14	0x0103000F
DDR_PHY_ADR_V_021	DDR_PHY_ADR_V_OFS	15	0x00030302
DDR_PHY_ADR_V_022	DDR_PHY_ADR_V_OFS	16	0x0000000F
DDR_PHY_ADR_V_023	DDR_PHY_ADR_V_OFS	17	0x00000100
DDR_PHY_ADR_V_024	DDR_PHY_ADR_V_OFS	18	0x00000000

Register Name	Address Offset (_OFS)	n [hex] (_OFS + n)	V4M
DDR_PHY_ADR_V_025	DDR_PHY_ADR_V_OFS	19	0x00000000
DDR_PHY_ADR_V_026	DDR_PHY_ADR_V_OFS	1A	0x00000000
DDR_PHY_ADR_V_027	DDR_PHY_ADR_V_OFS	1B	0x00000000
DDR_PHY_ADR_V_028	DDR_PHY_ADR_V_OFS	1C	0x00000000
DDR_PHY_ADR_V_029	DDR_PHY_ADR_V_OFS	1D	0x00040000
DDR_PHY_ADR_V_030	DDR_PHY_ADR_V_OFS	1E	0x002A0200
DDR_PHY_ADR_V_031	DDR_PHY_ADR_V_OFS	1F	0x00000000
DDR_PHY_ADR_V_032	DDR_PHY_ADR_V_OFS	20	0x00000000
DDR_PHY_ADR_V_033	DDR_PHY_ADR_V_OFS	21	0x00000000
DDR_PHY_ADR_V_034	DDR_PHY_ADR_V_OFS	22	0x00000000
DDR_PHY_ADR_V_035	DDR_PHY_ADR_V_OFS	23	0x00200101
DDR_PHY_ADR_V_036	DDR_PHY_ADR_V_OFS	24	0x10002C03
DDR_PHY_ADR_V_037	DDR_PHY_ADR_V_OFS	25	0x00800003
DDR_PHY_ADR_V_038	DDR_PHY_ADR_V_OFS	26	0x00010080
DDR_PHY_ADR_V_039	DDR_PHY_ADR_V_OFS	27	0x00008008
DDR_PHY_ADR_V_040	DDR_PHY_ADR_V_OFS	28	0x00081020
DDR_PHY_ADR_V_041	DDR_PHY_ADR_V_OFS	29	0x00200000
DDR_PHY_ADR_V_042	DDR_PHY_ADR_V_OFS	2A	0x00010001
DDR_PHY_ADR_V_043	DDR_PHY_ADR_V_OFS	2B	0x00000000
DDR_PHY_ADR_V_044	DDR_PHY_ADR_V_OFS	2C	0x00100302
DDR_PHY_ADR_V_045	DDR_PHY_ADR_V_OFS	2D	0x003E4208
DDR_PHY_ADR_V_046	DDR_PHY_ADR_V_OFS	2E	0x01800180
DDR_PHY_ADR_V_047	DDR_PHY_ADR_V_OFS	2F	0x01800180
DDR_PHY_ADR_V_048	DDR_PHY_ADR_V_OFS	30	0x01800180
DDR_PHY_ADR_V_049	DDR_PHY_ADR_V_OFS	31	0x01800180
DDR_PHY_ADR_V_050	DDR_PHY_ADR_V_OFS	32	0x00000180
DDR_PHY_ADR_V_051	DDR_PHY_ADR_V_OFS	33	0x00000180
DDR_PHY_ADR_V_052	DDR_PHY_ADR_V_OFS	34	0x00000180
DDR_PHY_ADR_V_053	DDR_PHY_ADR_V_OFS	35	0x00000180
DDR_PHY_ADR_V_054	DDR_PHY_ADR_V_OFS	36	0x00000000
DDR_PHY_ADR_V_055	DDR_PHY_ADR_V_OFS	37	0x00000000
DDR_PHY_ADR_V_056	DDR_PHY_ADR_V_OFS	38	0x00000000
DDR_PHY_ADR_V_057	DDR_PHY_ADR_V_OFS	39	0x00000000
DDR_PHY_ADR_V_058	DDR_PHY_ADR_V_OFS	3A	0x00010580
DDR_PHY_ADR_V_059	DDR_PHY_ADR_V_OFS	3B	0x03000040
DDR_PHY_ADR_V_060	DDR_PHY_ADR_V_OFS	3C	0x00000001
DDR_PHY_ADR_G_000	DDR_PHY_ADR_G_OFS	0	0x00000000
DDR_PHY_ADR_G_001	DDR_PHY_ADR_G_OFS	1	0x00000100
DDR_PHY_ADR_G_002	DDR_PHY_ADR_G_OFS	2	0x00000001
DDR_PHY_ADR_G_003	DDR_PHY_ADR_G_OFS	3	0x23800000
DDR_PHY_ADR_G_004	DDR_PHY_ADR_G_OFS	4	0x00000000
DDR_PHY_ADR_G_005	DDR_PHY_ADR_G_OFS	5	0x01000101

Register Name	Address Offset (_OFS)	n [hex] (_OFS + n)	V4M
DDR_PHY_ADR_G_006	DDR_PHY_ADR_G_OFS	6	0x01000000
DDR_PHY_ADR_G_007	DDR_PHY_ADR_G_OFS	7	0x00000000
DDR_PHY_ADR_G_008	DDR_PHY_ADR_G_OFS	8	0x00000000
DDR_PHY_ADR_G_009	DDR_PHY_ADR_G_OFS	9	0x00000000
DDR_PHY_ADR_G_010	DDR_PHY_ADR_G_OFS	A	0x00000000
DDR_PHY_ADR_G_011	DDR_PHY_ADR_G_OFS	B	0x00000000
DDR_PHY_ADR_G_012	DDR_PHY_ADR_G_OFS	C	0x00040101
DDR_PHY_ADR_G_013	DDR_PHY_ADR_G_OFS	D	0x00000000
DDR_PHY_ADR_G_014	DDR_PHY_ADR_G_OFS	E	0x00000000
DDR_PHY_ADR_G_015	DDR_PHY_ADR_G_OFS	F	0x00000064
DDR_PHY_ADR_G_016	DDR_PHY_ADR_G_OFS	10	0x00000000
DDR_PHY_ADR_G_017	DDR_PHY_ADR_G_OFS	11	0x00000000
DDR_PHY_ADR_G_018	DDR_PHY_ADR_G_OFS	12	0x3B421D42
DDR_PHY_ADR_G_019	DDR_PHY_ADR_G_OFS	13	0x00010124
DDR_PHY_ADR_G_020	DDR_PHY_ADR_G_OFS	14	0x00520052
DDR_PHY_ADR_G_021	DDR_PHY_ADR_G_OFS	15	0x00000052
DDR_PHY_ADR_G_022	DDR_PHY_ADR_G_OFS	16	0x00000000
DDR_PHY_ADR_G_023	DDR_PHY_ADR_G_OFS	17	0x00000000
DDR_PHY_ADR_G_024	DDR_PHY_ADR_G_OFS	18	0x00010001
DDR_PHY_ADR_G_025	DDR_PHY_ADR_G_OFS	19	0x00000000
DDR_PHY_ADR_G_026	DDR_PHY_ADR_G_OFS	1A	0x00000000
DDR_PHY_ADR_G_027	DDR_PHY_ADR_G_OFS	1B	0x00010001
DDR_PHY_ADR_G_028	DDR_PHY_ADR_G_OFS	1C	0x00000000
DDR_PHY_ADR_G_029	DDR_PHY_ADR_G_OFS	1D	0x00000000
DDR_PHY_ADR_G_030	DDR_PHY_ADR_G_OFS	1E	0x00010001
DDR_PHY_ADR_G_031	DDR_PHY_ADR_G_OFS	1F	0x07050102
DDR_PHY_ADR_G_032	DDR_PHY_ADR_G_OFS	20	0x01030307
DDR_PHY_ADR_G_033	DDR_PHY_ADR_G_OFS	21	0x00000094
DDR_PHY_ADR_G_034	DDR_PHY_ADR_G_OFS	22	0x00004096
DDR_PHY_ADR_G_035	DDR_PHY_ADR_G_OFS	23	0x08200820
DDR_PHY_ADR_G_036	DDR_PHY_ADR_G_OFS	24	0x08200820
DDR_PHY_ADR_G_037	DDR_PHY_ADR_G_OFS	25	0x08200820
DDR_PHY_ADR_G_038	DDR_PHY_ADR_G_OFS	26	0x08200820
DDR_PHY_ADR_G_039	DDR_PHY_ADR_G_OFS	27	0x08200820
DDR_PHY_ADR_G_040	DDR_PHY_ADR_G_OFS	28	0x004103B8
DDR_PHY_ADR_G_041	DDR_PHY_ADR_G_OFS	29	0x0000003F
DDR_PHY_ADR_G_042	DDR_PHY_ADR_G_OFS	2A	0x00090006
DDR_PHY_ADR_G_043	DDR_PHY_ADR_G_OFS	2B	0x00000000
DDR_PHY_ADR_G_044	DDR_PHY_ADR_G_OFS	2C	0x00000490
DDR_PHY_ADR_G_045	DDR_PHY_ADR_G_OFS	2D	0x00000000
DDR_PHY_ADR_G_046	DDR_PHY_ADR_G_OFS	2E	0x00000108
DDR_PHY_ADR_G_047	DDR_PHY_ADR_G_OFS	2F	0x00000000

Register Name	Address Offset (_OFS)	n [hex] (_OFS + n)	V4M
DDR_PHY_ADR_G_048	DDR_PHY_ADR_G_OFS	30	0x00000000
DDR_PHY_ADR_G_049	DDR_PHY_ADR_G_OFS	31	0x00000000
DDR_PHY_ADR_G_050	DDR_PHY_ADR_G_OFS	32	0x00000000
DDR_PHY_ADR_G_051	DDR_PHY_ADR_G_OFS	33	0x00000000
DDR_PHY_ADR_G_052	DDR_PHY_ADR_G_OFS	34	0x03000000
DDR_PHY_ADR_G_053	DDR_PHY_ADR_G_OFS	35	0x00000000
DDR_PHY_ADR_G_054	DDR_PHY_ADR_G_OFS	36	0x00000000
DDR_PHY_ADR_G_055	DDR_PHY_ADR_G_OFS	37	0x00000002
DDR_PHY_ADR_G_056	DDR_PHY_ADR_G_OFS	38	0x00041020
DDR_PHY_ADR_G_057	DDR_PHY_ADR_G_OFS	39	0x00041020
DDR_PHY_ADR_G_058	DDR_PHY_ADR_G_OFS	3A	0x01C98C98
DDR_PHY_ADR_G_059	DDR_PHY_ADR_G_OFS	3B	0x3F400000
DDR_PHY_ADR_G_060	DDR_PHY_ADR_G_OFS	3C	0x003F3F3F
DDR_PHY_ADR_G_061	DDR_PHY_ADR_G_OFS	3D	0x00000000
DDR_PHY_ADR_G_062	DDR_PHY_ADR_G_OFS	3E	0x00000000
DDR_PHY_ADR_G_063	DDR_PHY_ADR_G_OFS	3F	0x76543210
DDR_PHY_ADR_G_064	DDR_PHY_ADR_G_OFS	40	0x00000098
DDR_PHY_ADR_G_065	DDR_PHY_ADR_G_OFS	41	0x00000007
DDR_PHY_ADR_G_066	DDR_PHY_ADR_G_OFS	42	0x00000000
DDR_PHY_ADR_G_067	DDR_PHY_ADR_G_OFS	43	0x00000000
DDR_PHY_ADR_G_068	DDR_PHY_ADR_G_OFS	44	0x00000000
DDR_PHY_ADR_G_069	DDR_PHY_ADR_G_OFS	45	0x00000002
DDR_PHY_ADR_G_070	DDR_PHY_ADR_G_OFS	46	0x00000000
DDR_PHY_ADR_G_071	DDR_PHY_ADR_G_OFS	47	0x00000000
DDR_PHY_ADR_G_072	DDR_PHY_ADR_G_OFS	48	0x0000017F
DDR_PHY_ADR_G_073	DDR_PHY_ADR_G_OFS	49	0x00000000
DDR_PHY_ADR_G_074	DDR_PHY_ADR_G_OFS	4A	0x00032380
DDR_PHY_ADR_G_075	DDR_PHY_ADR_G_OFS	4B	0x00000100
DDR_PHY_ADR_G_076	DDR_PHY_ADR_G_OFS	4C	0x00000000
DDR_PHY_ADR_G_077	DDR_PHY_ADR_G_OFS	4D	0x31421142
DDR_PHY_ADR_G_078	DDR_PHY_ADR_G_OFS	4E	0x00248000
DDR_PHY_ADR_G_079	DDR_PHY_ADR_G_OFS	4F	0x00000080
DDR_PHY_ADR_G_080	DDR_PHY_ADR_G_OFS	50	0x0004BF77
DDR_PHY_ADR_G_081	DDR_PHY_ADR_G_OFS	51	0x00000006
DDR_PHY_ADR_G_082	DDR_PHY_ADR_G_OFS	52	0x0000027F
DDR_PHY_ADR_G_083	DDR_PHY_ADR_G_OFS	53	0x0000027F
DDR_PHY_ADR_G_084	DDR_PHY_ADR_G_OFS	54	0x0000027F
DDR_PHY_ADR_G_085	DDR_PHY_ADR_G_OFS	55	0x00027F00
DDR_PHY_ADR_G_086	DDR_PHY_ADR_G_OFS	56	0x00CC0000
DDR_PHY_ADR_G_087	DDR_PHY_ADR_G_OFS	57	0x00027F00
DDR_PHY_ADR_G_088	DDR_PHY_ADR_G_OFS	58	0x00CC0000
DDR_PHY_ADR_G_089	DDR_PHY_ADR_G_OFS	59	0x00027F77

Register Name	Address Offset (_OFS)	n [hex] (_OFS + n)	V4M
DDR_PHY_ADR_G_090	DDR_PHY_ADR_G_OFS	5A	0x00000000
DDR_PHY_ADR_G_091	DDR_PHY_ADR_G_OFS	5B	0x00033F00
DDR_PHY_ADR_G_092	DDR_PHY_ADR_G_OFS	5C	0x00EE0000
DDR_PHY_ADR_G_093	DDR_PHY_ADR_G_OFS	5D	0x00027F00
DDR_PHY_ADR_G_094	DDR_PHY_ADR_G_OFS	5E	0x00EE0000
DDR_PHY_ADR_G_095	DDR_PHY_ADR_G_OFS	5F	0x00027F00
DDR_PHY_ADR_G_096	DDR_PHY_ADR_G_OFS	60	0x00CC0000
DDR_PHY_ADR_G_097	DDR_PHY_ADR_G_OFS	61	0x00200106
DDR_PI_000	DDR_PI_OFS	0	0x00000B00
DDR_PI_001	DDR_PI_OFS	1	0x00000000
DDR_PI_002	DDR_PI_OFS	2	0x00000000
DDR_PI_003	DDR_PI_OFS	3	0x00010100
DDR_PI_004	DDR_PI_OFS	4	0x00640004
DDR_PI_005	DDR_PI_OFS	5	0x00000001
DDR_PI_006	DDR_PI_OFS	6	0x00000000
DDR_PI_007	DDR_PI_OFS	7	0x00000000
DDR_PI_008	DDR_PI_OFS	8	0x00000000
DDR_PI_009	DDR_PI_OFS	9	0x00000000
DDR_PI_010	DDR_PI_OFS	A	0xFFFFFFFF
DDR_PI_011	DDR_PI_OFS	B	0x02010000
DDR_PI_012	DDR_PI_OFS	C	0x00000003
DDR_PI_013	DDR_PI_OFS	D	0x00000005
DDR_PI_014	DDR_PI_OFS	E	0x00000002
DDR_PI_015	DDR_PI_OFS	F	0x00000000
DDR_PI_016	DDR_PI_OFS	10	0x00000101
DDR_PI_017	DDR_PI_OFS	11	0xFFFFFFFF
DDR_PI_018	DDR_PI_OFS	12	0xFFFBFFFF
DDR_PI_019	DDR_PI_OFS	13	0x001E2C0E
DDR_PI_020	DDR_PI_OFS	14	0x00000000
DDR_PI_021	DDR_PI_OFS	15	0x00030300
DDR_PI_022	DDR_PI_OFS	16	0x01010700
DDR_PI_023	DDR_PI_OFS	17	0x00000001
DDR_PI_024	DDR_PI_OFS	18	0x00000001
DDR_PI_025	DDR_PI_OFS	19	0x00000000
DDR_PI_026	DDR_PI_OFS	1A	0x00000000
DDR_PI_027	DDR_PI_OFS	1B	0x00000000
DDR_PI_028	DDR_PI_OFS	1C	0x00000000
DDR_PI_029	DDR_PI_OFS	1D	0x00000000
DDR_PI_030	DDR_PI_OFS	1E	0x00000000
DDR_PI_031	DDR_PI_OFS	1F	0x05010000
DDR_PI_032	DDR_PI_OFS	20	0x00000028
DDR_PI_033	DDR_PI_OFS	21	0x00000000

Register Name	Address Offset (_OFS)	n [hex] (_OFS + n)	V4M
DDR_PI_034	DDR_PI_OFS	22	0x00320003
DDR_PI_035	DDR_PI_OFS	23	0x00000000
DDR_PI_036	DDR_PI_OFS	24	0x00000000
DDR_PI_037	DDR_PI_OFS	25	0x04022002
DDR_PI_038	DDR_PI_OFS	26	0x01040100
DDR_PI_039	DDR_PI_OFS	27	0x00000101
DDR_PI_040	DDR_PI_OFS	28	0x00000001
DDR_PI_041	DDR_PI_OFS	29	0x000000AA
DDR_PI_042	DDR_PI_OFS	2A	0x00000055
DDR_PI_043	DDR_PI_OFS	2B	0x000000B5
DDR_PI_044	DDR_PI_OFS	2C	0x0000004A
DDR_PI_045	DDR_PI_OFS	2D	0x00000056
DDR_PI_046	DDR_PI_OFS	2E	0x000000A9
DDR_PI_047	DDR_PI_OFS	2F	0x000000A9
DDR_PI_048	DDR_PI_OFS	30	0x000000B5
DDR_PI_049	DDR_PI_OFS	31	0x00000000
DDR_PI_050	DDR_PI_OFS	32	0x01000000
DDR_PI_051	DDR_PI_OFS	33	0x00030300
DDR_PI_052	DDR_PI_OFS	34	0x0000001A
DDR_PI_053	DDR_PI_OFS	35	0x000007D0
DDR_PI_054	DDR_PI_OFS	36	0x00000300
DDR_PI_055	DDR_PI_OFS	37	0x00000000
DDR_PI_056	DDR_PI_OFS	38	0x00000000
DDR_PI_057	DDR_PI_OFS	39	0x01000000
DDR_PI_058	DDR_PI_OFS	3A	0x00000101
DDR_PI_059	DDR_PI_OFS	3B	0x00000000
DDR_PI_060	DDR_PI_OFS	3C	0x00000000
DDR_PI_061	DDR_PI_OFS	3D	0x00000000
DDR_PI_062	DDR_PI_OFS	3E	0x00000200
DDR_PI_063	DDR_PI_OFS	3F	0x03030300
DDR_PI_064	DDR_PI_OFS	40	0x01000000
DDR_PI_065	DDR_PI_OFS	41	0x00000000
DDR_PI_066	DDR_PI_OFS	42	0x00000000
DDR_PI_067	DDR_PI_OFS	43	0x07010000
DDR_PI_068	DDR_PI_OFS	44	0x00000107
DDR_PI_069	DDR_PI_OFS	45	0x00000000
DDR_PI_070	DDR_PI_OFS	46	0x03000100
DDR_PI_071	DDR_PI_OFS	47	0x00000000
DDR_PI_072	DDR_PI_OFS	48	0x00001703
DDR_PI_073	DDR_PI_OFS	49	0x00000000
DDR_PI_074	DDR_PI_OFS	4A	0x00000000
DDR_PI_075	DDR_PI_OFS	4B	0x00000000

Register Name	Address Offset (_OFS)	n [hex] (_OFS + n)	V4M
DDR_PI_076	DDR_PI_OFS	4C	0x0A0A140A
DDR_PI_077	DDR_PI_OFS	4D	0x10020401
DDR_PI_078	DDR_PI_OFS	4E	0x00000002
DDR_PI_079	DDR_PI_OFS	4F	0x00010000
DDR_PI_080	DDR_PI_OFS	50	0x0B000404
DDR_PI_081	DDR_PI_OFS	51	0x0B050508
DDR_PI_082	DDR_PI_OFS	52	0x00010100
DDR_PI_083	DDR_PI_OFS	53	0x02020301
DDR_PI_084	DDR_PI_OFS	54	0x01001000
DDR_PI_085	DDR_PI_OFS	55	0x00000034
DDR_PI_086	DDR_PI_OFS	56	0x00000000
DDR_PI_087	DDR_PI_OFS	57	0x00000000
DDR_PI_088	DDR_PI_OFS	58	0x00000000
DDR_PI_089	DDR_PI_OFS	59	0x00000000
DDR_PI_090	DDR_PI_OFS	5A	0x00000000
DDR_PI_091	DDR_PI_OFS	5B	0x00080000
DDR_PI_092	DDR_PI_OFS	5C	0x00000000
DDR_PI_093	DDR_PI_OFS	5D	0x55AA55AA
DDR_PI_094	DDR_PI_OFS	5E	0x33CC33CC
DDR_PI_095	DDR_PI_OFS	5F	0x0FF00FF0
DDR_PI_096	DDR_PI_OFS	60	0x0F0FF0F0
DDR_PI_097	DDR_PI_OFS	61	0x00008E38
DDR_PI_098	DDR_PI_OFS	62	0x00000001
DDR_PI_099	DDR_PI_OFS	63	0x00000002
DDR_PI_100	DDR_PI_OFS	64	0x00020001
DDR_PI_101	DDR_PI_OFS	65	0x00020001
DDR_PI_102	DDR_PI_OFS	66	0x02010201
DDR_PI_103	DDR_PI_OFS	67	0x0000000F
DDR_PI_104	DDR_PI_OFS	68	0x00000000
DDR_PI_105	DDR_PI_OFS	69	0x00000000
DDR_PI_106	DDR_PI_OFS	6A	0x00000000
DDR_PI_107	DDR_PI_OFS	6B	0x00000000
DDR_PI_108	DDR_PI_OFS	6C	0x00000000
DDR_PI_109	DDR_PI_OFS	6D	0x00000000
DDR_PI_110	DDR_PI_OFS	6E	0x00000000
DDR_PI_111	DDR_PI_OFS	6F	0x00000000
DDR_PI_112	DDR_PI_OFS	70	0x00000000
DDR_PI_113	DDR_PI_OFS	71	0x00000000
DDR_PI_114	DDR_PI_OFS	72	0xAAAA9999
DDR_PI_115	DDR_PI_OFS	73	0xA5939999
DDR_PI_116	DDR_PI_OFS	74	0x00000000
DDR_PI_117	DDR_PI_OFS	75	0x0000AA55

Register Name	Address Offset (_OFS)	n [hex] (_OFS + n)	V4M
DDR_PI_118	DDR_PI_OFS	76	0x00006633
DDR_PI_119	DDR_PI_OFS	77	0x000198CC
DDR_PI_120	DDR_PI_OFS	78	0x00000000
DDR_PI_121	DDR_PI_OFS	79	0x0003FFFF
DDR_PI_122	DDR_PI_OFS	7A	0x00006633
DDR_PI_123	DDR_PI_OFS	7B	0x000198CC
DDR_PI_124	DDR_PI_OFS	7C	0x00000000
DDR_PI_125	DDR_PI_OFS	7D	0x036DB6DB
DDR_PI_126	DDR_PI_OFS	7E	0x00249249
DDR_PI_127	DDR_PI_OFS	7F	0x05B6DB6D
DDR_PI_128	DDR_PI_OFS	80	0x00000000
DDR_PI_129	DDR_PI_OFS	81	0x00000000
DDR_PI_130	DDR_PI_OFS	82	0x00000000
DDR_PI_131	DDR_PI_OFS	83	0x00000000
DDR_PI_132	DDR_PI_OFS	84	0x00000000
DDR_PI_133	DDR_PI_OFS	85	0x036DB6DB
DDR_PI_134	DDR_PI_OFS	86	0x00249249
DDR_PI_135	DDR_PI_OFS	87	0x05B6DB6D
DDR_PI_136	DDR_PI_OFS	88	0x00000000
DDR_PI_137	DDR_PI_OFS	89	0x00000000
DDR_PI_138	DDR_PI_OFS	8A	0x00000000
DDR_PI_139	DDR_PI_OFS	8B	0x00000000
DDR_PI_140	DDR_PI_OFS	8C	0x00000000
DDR_PI_141	DDR_PI_OFS	8D	0x01000000
DDR_PI_142	DDR_PI_OFS	8E	0x00000101
DDR_PI_143	DDR_PI_OFS	8F	0x00000000
DDR_PI_144	DDR_PI_OFS	90	0x00000000
DDR_PI_145	DDR_PI_OFS	91	0x00000000
DDR_PI_146	DDR_PI_OFS	92	0x00000000
DDR_PI_147	DDR_PI_OFS	93	0x00000000
DDR_PI_148	DDR_PI_OFS	94	0x00000000
DDR_PI_149	DDR_PI_OFS	95	0x00000000
DDR_PI_150	DDR_PI_OFS	96	0x00000000
DDR_PI_151	DDR_PI_OFS	97	0x00010000
DDR_PI_152	DDR_PI_OFS	98	0x00000000
DDR_PI_153	DDR_PI_OFS	99	0x00000000
DDR_PI_154	DDR_PI_OFS	9A	0x00000000
DDR_PI_155	DDR_PI_OFS	9B	0x00000000
DDR_PI_156	DDR_PI_OFS	9C	0x00000000
DDR_PI_157	DDR_PI_OFS	9D	0x00000000
DDR_PI_158	DDR_PI_OFS	9E	0x00000000
DDR_PI_159	DDR_PI_OFS	9F	0x00000000

Register Name	Address Offset (_OFS)	n [hex] (_OFS + n)	V4M
DDR_PI_160	DDR_PI_OFS	A0	0x00000000
DDR_PI_161	DDR_PI_OFS	A1	0x00000000
DDR_PI_162	DDR_PI_OFS	A2	0x00000000
DDR_PI_163	DDR_PI_OFS	A3	0x00000000
DDR_PI_164	DDR_PI_OFS	A4	0x00010000
DDR_PI_165	DDR_PI_OFS	A5	0x00000000
DDR_PI_166	DDR_PI_OFS	A6	0x00000000
DDR_PI_167	DDR_PI_OFS	A7	0x00000000
DDR_PI_168	DDR_PI_OFS	A8	0x00000000
DDR_PI_169	DDR_PI_OFS	A9	0x00000000
DDR_PI_170	DDR_PI_OFS	AA	0x00000000
DDR_PI_171	DDR_PI_OFS	AB	0x00000000
DDR_PI_172	DDR_PI_OFS	AC	0x00000000
DDR_PI_173	DDR_PI_OFS	AD	0x00000000
DDR_PI_174	DDR_PI_OFS	AE	0x00000000
DDR_PI_175	DDR_PI_OFS	AF	0x00000000
DDR_PI_176	DDR_PI_OFS	B0	0x00000000
DDR_PI_177	DDR_PI_OFS	B1	0x00080000
DDR_PI_178	DDR_PI_OFS	B2	0x02000200
DDR_PI_179	DDR_PI_OFS	B3	0x01000100
DDR_PI_180	DDR_PI_OFS	B4	0x01000000
DDR_PI_181	DDR_PI_OFS	B5	0x02000200
DDR_PI_182	DDR_PI_OFS	B6	0x00000200
DDR_PI_183	DDR_PI_OFS	B7	0x00000000
DDR_PI_184	DDR_PI_OFS	B8	0x00000000
DDR_PI_185	DDR_PI_OFS	B9	0x00000000
DDR_PI_186	DDR_PI_OFS	BA	0x00000000
DDR_PI_187	DDR_PI_OFS	BB	0x00000000
DDR_PI_188	DDR_PI_OFS	BC	0x01000400
DDR_PI_189	DDR_PI_OFS	BD	0x03020100
DDR_PI_190	DDR_PI_OFS	BE	0x00060504
DDR_PI_191	DDR_PI_OFS	BF	0x00010100
DDR_PI_192	DDR_PI_OFS	C0	0x02000008
DDR_PI_193	DDR_PI_OFS	C1	0x00000000
DDR_PI_194	DDR_PI_OFS	C2	0x01000001
DDR_PI_195	DDR_PI_OFS	C3	0x00000000
DDR_PI_196	DDR_PI_OFS	C4	0x0000000B
DDR_PI_197	DDR_PI_OFS	C5	0x0000001C
DDR_PI_198	DDR_PI_OFS	C6	0x00000100
DDR_PI_199	DDR_PI_OFS	C7	0x00000000
DDR_PI_200	DDR_PI_OFS	C8	0x00000000
DDR_PI_201	DDR_PI_OFS	C9	0x00000000

Register Name	Address Offset (_OFS)	n [hex] (_OFS + n)	V4M
DDR_PI_202	DDR_PI_OFS	CA	0x00000000
DDR_PI_203	DDR_PI_OFS	CB	0x03010000
DDR_PI_204	DDR_PI_OFS	CC	0x01000100
DDR_PI_205	DDR_PI_OFS	CD	0x01020001
DDR_PI_206	DDR_PI_OFS	CE	0x00010300
DDR_PI_207	DDR_PI_OFS	CF	0x05000104
DDR_PI_208	DDR_PI_OFS	D0	0x01060001
DDR_PI_209	DDR_PI_OFS	D1	0x00010700
DDR_PI_210	DDR_PI_OFS	D2	0x00000000
DDR_PI_211	DDR_PI_OFS	D3	0x00000000
DDR_PI_212	DDR_PI_OFS	D4	0x00010001
DDR_PI_213	DDR_PI_OFS	D5	0x00000000
DDR_PI_214	DDR_PI_OFS	D6	0x00000000
DDR_PI_215	DDR_PI_OFS	D7	0x00000000
DDR_PI_216	DDR_PI_OFS	D8	0x00000000
DDR_PI_217	DDR_PI_OFS	D9	0x01000000
DDR_PI_218	DDR_PI_OFS	DA	0x00000008
DDR_PI_219	DDR_PI_OFS	DB	0x00000000
DDR_PI_220	DDR_PI_OFS	DC	0x01010000
DDR_PI_221	DDR_PI_OFS	DD	0x02000000
DDR_PI_222	DDR_PI_OFS	DE	0x00000201
DDR_PI_223	DDR_PI_OFS	DF	0x00000000
DDR_PI_224	DDR_PI_OFS	E0	0xC8000300
DDR_PI_225	DDR_PI_OFS	E1	0x010000DF
DDR_PI_226	DDR_PI_OFS	E2	0x0000DFD8
DDR_PI_227	DDR_PI_OFS	E3	0x00DFD401
DDR_PI_228	DDR_PI_OFS	E4	0xDFC60100
DDR_PI_229	DDR_PI_OFS	E5	0x1002DF4D
DDR_PI_230	DDR_PI_OFS	E6	0x0000002B
DDR_PI_231	DDR_PI_OFS	E7	0x00000030
DDR_PI_232	DDR_PI_OFS	E8	0x00000040
DDR_PI_233	DDR_PI_OFS	E9	0x00020064
DDR_PI_234	DDR_PI_OFS	EA	0x02000200
DDR_PI_235	DDR_PI_OFS	EB	0x00000004
DDR_PI_236	DDR_PI_OFS	EC	0x0B090000
DDR_PI_237	DDR_PI_OFS	ED	0x000C0600
DDR_PI_238	DDR_PI_OFS	EE	0x00000000
DDR_PI_239	DDR_PI_OFS	EF	0x10001511
DDR_PI_240	DDR_PI_OFS	F0	0x00000012
DDR_PI_241	DDR_PI_OFS	F1	0x2D170000
DDR_PI_242	DDR_PI_OFS	F2	0x00152800
DDR_PI_243	DDR_PI_OFS	F3	0x000000CF
DDR_PI_244	DDR_PI_OFS	F4	0x00000130
DDR_PI_245	DDR_PI_OFS	F5	0x00000C2E

Register Name	Address Offset (_OFS)	n [hex] (_OFS + n)	V4M
DDR_PI_246	DDR_PI_OFS	F6	0x0000032B
DDR_PI_247	DDR_PI_OFS	F7	0x10002082
DDR_PI_248	DDR_PI_OFS	F8	0x00040404
DDR_PI_249	DDR_PI_OFS	F9	0x08002100
DDR_PI_250	DDR_PI_OFS	FA	0x0F001B01
DDR_PI_251	DDR_PI_OFS	FB	0x21002101
DDR_PI_252	DDR_PI_OFS	FC	0x00000000
DDR_PI_253	DDR_PI_OFS	FD	0x00000000
DDR_PI_254	DDR_PI_OFS	FE	0x00000000
DDR_PI_255	DDR_PI_OFS	FF	0x01010000
DDR_PI_256	DDR_PI_OFS	100	0x01000101
DDR_PI_257	DDR_PI_OFS	101	0x03000000
DDR_PI_258	DDR_PI_OFS	102	0x00000100
DDR_PI_259	DDR_PI_OFS	103	0x01000300
DDR_PI_260	DDR_PI_OFS	104	0x03000000
DDR_PI_261	DDR_PI_OFS	105	0x000A0004
DDR_PI_262	DDR_PI_OFS	106	0x08020019
DDR_PI_263	DDR_PI_OFS	107	0x0404020E
DDR_PI_264	DDR_PI_OFS	108	0x000C0034
DDR_PI_265	DDR_PI_OFS	109	0x0013003B
DDR_PI_266	DDR_PI_OFS	10A	0x00210049
DDR_PI_267	DDR_PI_OFS	10B	0x01010101
DDR_PI_268	DDR_PI_OFS	10C	0x0002000E
DDR_PI_269	DDR_PI_OFS	10D	0x000400C8
DDR_PI_270	DDR_PI_OFS	10E	0x01000216
DDR_PI_271	DDR_PI_OFS	10F	0x000F000F
DDR_PI_272	DDR_PI_OFS	110	0x0007000C
DDR_PI_273	DDR_PI_OFS	111	0x00C90100
DDR_PI_274	DDR_PI_OFS	112	0x00A100C9
DDR_PI_275	DDR_PI_OFS	113	0x01000051
DDR_PI_276	DDR_PI_OFS	114	0x02170217
DDR_PI_277	DDR_PI_OFS	115	0x00D701AC
DDR_PI_278	DDR_PI_OFS	116	0x15001515
DDR_PI_279	DDR_PI_OFS	117	0x1F0B0015
DDR_PI_280	DDR_PI_OFS	118	0x0A070600
DDR_PI_281	DDR_PI_OFS	119	0x0D09070D
DDR_PI_282	DDR_PI_OFS	11A	0x1F130A0D
DDR_PI_283	DDR_PI_OFS	11B	0x000C0014
DDR_PI_284	DDR_PI_OFS	11C	0x00001000
DDR_PI_285	DDR_PI_OFS	11D	0x00000C00
DDR_PI_286	DDR_PI_OFS	11E	0x00001000
DDR_PI_287	DDR_PI_OFS	11F	0x00000C00
DDR_PI_288	DDR_PI_OFS	120	0x02001000
DDR_PI_289	DDR_PI_OFS	121	0x0016000E
DDR_PI_290	DDR_PI_OFS	122	0x002400C8

Register Name	Address Offset (_OFS)	n [hex] (_OFS + n)	V4M
DDR_PI_291	DDR_PI_OFS	123	0x1E1A0216
DDR_PI_292	DDR_PI_OFS	124	0x00210004
DDR_PI_293	DDR_PI_OFS	125	0x220E0020
DDR_PI_294	DDR_PI_OFS	126	0x00010000
DDR_PI_295	DDR_PI_OFS	127	0x00020004
DDR_PI_296	DDR_PI_OFS	128	0x00002900
DDR_PI_297	DDR_PI_OFS	129	0x220E002D
DDR_PI_298	DDR_PI_OFS	12A	0x00010300
DDR_PI_299	DDR_PI_OFS	12B	0x00080008
DDR_PI_300	DDR_PI_OFS	12C	0x00003D00
DDR_PI_301	DDR_PI_OFS	12D	0x220E004C
DDR_PI_302	DDR_PI_OFS	12E	0x00010300
DDR_PI_303	DDR_PI_OFS	12F	0x000E0015
DDR_PI_304	DDR_PI_OFS	130	0x00000000
DDR_PI_305	DDR_PI_OFS	131	0x00000003
DDR_PI_306	DDR_PI_OFS	132	0x00040408
DDR_PI_307	DDR_PI_OFS	133	0x09000909
DDR_PI_308	DDR_PI_OFS	134	0x0006C904
DDR_PI_309	DDR_PI_OFS	135	0x20010003
DDR_PI_310	DDR_PI_OFS	136	0x080A0A03
DDR_PI_311	DDR_PI_OFS	137	0x09000F11
DDR_PI_312	DDR_PI_OFS	138	0x10090009
DDR_PI_313	DDR_PI_OFS	139	0x002262B8
DDR_PI_314	DDR_PI_OFS	13A	0x0C0C2003
DDR_PI_315	DDR_PI_OFS	13B	0x272D100A
DDR_PI_316	DDR_PI_OFS	13C	0x00171700
DDR_PI_317	DDR_PI_OFS	13D	0x752F2817
DDR_PI_318	DDR_PI_OFS	13E	0x2008005A
DDR_PI_319	DDR_PI_OFS	13F	0x00161E20
DDR_PI_320	DDR_PI_OFS	140	0x0000019E
DDR_PI_321	DDR_PI_OFS	141	0x0000102C
DDR_PI_322	DDR_PI_OFS	142	0x0000185C
DDR_PI_323	DDR_PI_OFS	143	0x0000F398
DDR_PI_324	DDR_PI_OFS	144	0x00004104
DDR_PI_325	DDR_PI_OFS	145	0x00028A28
DDR_PI_326	DDR_PI_OFS	146	0x01360016
DDR_PI_327	DDR_PI_OFS	147	0x0303033B
DDR_PI_328	DDR_PI_OFS	148	0x002AF804
DDR_PI_329	DDR_PI_OFS	149	0x00000000
DDR_PI_330	DDR_PI_OFS	14A	0x00006B6B
DDR_PI_331	DDR_PI_OFS	14B	0x00000005
DDR_PI_332	DDR_PI_OFS	14C	0x0000006E
DDR_PI_333	DDR_PI_OFS	14D	0x00000016
DDR_PI_334	DDR_PI_OFS	14E	0x00027100
DDR_PI_335	DDR_PI_OFS	14F	0x00000000

Register Name	Address Offset (_OFS)	n [hex] (_OFS + n)	V4M
DDR_PI_336	DDR_PI_OFS	150	0x0001ADAF
DDR_PI_337	DDR_PI_OFS	151	0x00000005
DDR_PI_338	DDR_PI_OFS	152	0x00000640
DDR_PI_339	DDR_PI_OFS	153	0x00000136
DDR_PI_340	DDR_PI_OFS	154	0x000681C8
DDR_PI_341	DDR_PI_OFS	155	0x00000000
DDR_PI_342	DDR_PI_OFS	156	0x0001ADAF
DDR_PI_343	DDR_PI_OFS	157	0x00000005
DDR_PI_344	DDR_PI_OFS	158	0x000010A9
DDR_PI_345	DDR_PI_OFS	159	0x0100033B
DDR_PI_346	DDR_PI_OFS	15A	0x00370040
DDR_PI_347	DDR_PI_OFS	15B	0x00010002
DDR_PI_348	DDR_PI_OFS	15C	0x03200040
DDR_PI_349	DDR_PI_OFS	15D	0x00010018
DDR_PI_350	DDR_PI_OFS	15E	0x08550040
DDR_PI_351	DDR_PI_OFS	15F	0x00000340
DDR_PI_352	DDR_PI_OFS	160	0x006B0028
DDR_PI_353	DDR_PI_OFS	161	0x05040404
DDR_PI_354	DDR_PI_OFS	162	0x000E0603
DDR_PI_355	DDR_PI_OFS	163	0x07040603
DDR_PI_356	DDR_PI_OFS	164	0x0D1000C8
DDR_PI_357	DDR_PI_OFS	165	0x02160E0B
DDR_PI_358	DDR_PI_OFS	166	0x0604062B
DDR_PI_359	DDR_PI_OFS	167	0x00040604
DDR_PI_360	DDR_PI_OFS	168	0x01320017
DDR_PI_361	DDR_PI_OFS	169	0x0105032D
DDR_PI_362	DDR_PI_OFS	16A	0x01050105
DDR_PI_363	DDR_PI_OFS	16B	0x01010100
DDR_PI_364	DDR_PI_OFS	16C	0x08030303
DDR_PI_365	DDR_PI_OFS	16D	0x05010808
DDR_PI_366	DDR_PI_OFS	16E	0x05010501
DDR_PI_367	DDR_PI_OFS	16F	0x02000001
DDR_PI_368	DDR_PI_OFS	170	0x00010003
DDR_PI_369	DDR_PI_OFS	171	0x02010100
DDR_PI_370	DDR_PI_OFS	172	0x00000002
DDR_PI_371	DDR_PI_OFS	173	0x00000000
DDR_PI_372	DDR_PI_OFS	174	0x017F0000
DDR_PI_373	DDR_PI_OFS	175	0x01010101
DDR_PI_374	DDR_PI_OFS	176	0x00000001
DDR_PI_375	DDR_PI_OFS	177	0x00000000
DDR_PI_376	DDR_PI_OFS	178	0x00000000
DDR_PI_377	DDR_PI_OFS	179	0x00000000
DDR_PI_378	DDR_PI_OFS	17A	0x00000000
DDR_PI_379	DDR_PI_OFS	17B	0x01000000
DDR_PI_380	DDR_PI_OFS	17C	0x01000101

Register Name	Address Offset (_OFS)	n [hex] (_OFS + n)	V4M
DDR_PI_381	DDR_PI_OFS	17D	0x00000000
DDR_PI_382	DDR_PI_OFS	17E	0x00000000
DDR_PI_383	DDR_PI_OFS	17F	0x08203020
DDR_PI_384	DDR_PI_OFS	180	0x28100020
DDR_PI_385	DDR_PI_OFS	181	0x08083020
DDR_PI_386	DDR_PI_OFS	182	0x08400020
DDR_PI_387	DDR_PI_OFS	183	0x08402020
DDR_PI_388	DDR_PI_OFS	184	0x08483020
DDR_PI_389	DDR_PI_OFS	185	0x10083020
DDR_PI_390	DDR_PI_OFS	186	0x20180020
DDR_PI_391	DDR_PI_OFS	187	0x30480020
DDR_PI_392	DDR_PI_OFS	188	0x78880020
DDR_PI_393	DDR_PI_OFS	189	0x488010E0
DDR_PI_394	DDR_PI_OFS	18A	0x494B0000
DDR_PI_395	DDR_PI_OFS	18B	0x49080000
DDR_PI_396	DDR_PI_OFS	18C	0x490011C0
DDR_PI_397	DDR_PI_OFS	18D	0x0A000020
DDR_PI_398	DDR_PI_OFS	18E	0x08000020
DDR_PI_399	DDR_PI_OFS	18F	0x08000020
DDR_PI_400	DDR_PI_OFS	190	0x08000020
DDR_PI_401	DDR_PI_OFS	191	0x08000020
DDR_PI_402	DDR_PI_OFS	192	0x08000020
DDR_PI_403	DDR_PI_OFS	193	0x08000020
DDR_PI_404	DDR_PI_OFS	194	0x08000020
DDR_PI_405	DDR_PI_OFS	195	0x08000020
DDR_PI_406	DDR_PI_OFS	196	0x08000020
DDR_PI_407	DDR_PI_OFS	197	0x08000020
DDR_PI_408	DDR_PI_OFS	198	0x08000020
DDR_PI_409	DDR_PI_OFS	199	0x08000020
DDR_PI_410	DDR_PI_OFS	19A	0x08000020
DDR_PI_411	DDR_PI_OFS	19B	0x08000020
DDR_PI_412	DDR_PI_OFS	19C	0x08000020
DDR_PI_413	DDR_PI_OFS	19D	0x08000020
DDR_PI_414	DDR_PI_OFS	19E	0x08000020
DDR_PI_415	DDR_PI_OFS	19F	0x08000020
DDR_PI_416	DDR_PI_OFS	1A0	0x08000020
DDR_PI_417	DDR_PI_OFS	1A1	0x08000020
DDR_PI_418	DDR_PI_OFS	1A2	0x08000020
DDR_PI_419	DDR_PI_OFS	1A3	0x08000020
DDR_PI_420	DDR_PI_OFS	1A4	0x08000020
DDR_PI_421	DDR_PI_OFS	1A5	0x08000020
DDR_PI_422	DDR_PI_OFS	1A6	0x08000020
DDR_PI_423	DDR_PI_OFS	1A7	0x08000020
DDR_PI_424	DDR_PI_OFS	1A8	0x08000020
DDR_PI_425	DDR_PI_OFS	1A9	0x08000020

Register Name	Address Offset (_OFS)	n [hex] (_OFS + n)	V4M
DDR_PI_426	DDR_PI_OFS	1AA	0x08000020
DDR_PI_427	DDR_PI_OFS	1AB	0x08000020
DDR_PI_428	DDR_PI_OFS	1AC	0x08084340
DDR_PI_429	DDR_PI_OFS	1AD	0x001F0000
DDR_PI_430	DDR_PI_OFS	1AE	0x001F0000
DDR_PI_431	DDR_PI_OFS	1AF	0x001F0000
DDR_PI_432	DDR_PI_OFS	1B0	0x001F0000
DDR_PI_433	DDR_PI_OFS	1B1	0x001F0000
DDR_PI_434	DDR_PI_OFS	1B2	0x001F0000
DDR_PI_435	DDR_PI_OFS	1B3	0x081E4340
DDR_PI_436	DDR_PI_OFS	1B4	0x003F0000
DDR_PI_437	DDR_PI_OFS	1B5	0x003F0000
DDR_PI_438	DDR_PI_OFS	1B6	0x003F0000
DDR_PI_439	DDR_PI_OFS	1B7	0x081A5047
DDR_PI_440	DDR_PI_OFS	1B8	0x001A10FF
DDR_PI_441	DDR_PI_OFS	1B9	0x00051A00
DDR_PI_442	DDR_PI_OFS	1BA	0x001A11FF
DDR_PI_443	DDR_PI_OFS	1BB	0x00051B00
DDR_PI_444	DDR_PI_OFS	1BC	0x001F13FF
DDR_PI_445	DDR_PI_OFS	1BD	0x081A5047
DDR_PI_446	DDR_PI_OFS	1BE	0x001A10FF
DDR_PI_447	DDR_PI_OFS	1BF	0x00051A00
DDR_PI_448	DDR_PI_OFS	1C0	0x001A11FF
DDR_PI_449	DDR_PI_OFS	1C1	0x00051B00
DDR_PI_450	DDR_PI_OFS	1C2	0x001F13FF
DDR_PI_451	DDR_PI_OFS	1C3	0x081A5047
DDR_PI_452	DDR_PI_OFS	1C4	0x001A10FF
DDR_PI_453	DDR_PI_OFS	1C5	0x00051A00
DDR_PI_454	DDR_PI_OFS	1C6	0x001A11FF
DDR_PI_455	DDR_PI_OFS	1C7	0x00051B00
DDR_PI_456	DDR_PI_OFS	1C8	0x001F13FF
DDR_PI_457	DDR_PI_OFS	1C9	0x11910048
DDR_PI_458	DDR_PI_OFS	1CA	0x09911000
DDR_PI_459	DDR_PI_OFS	1CB	0x19A20D06
DDR_PI_460	DDR_PI_OFS	1CC	0x19A10100
DDR_PI_461	DDR_PI_OFS	1CD	0x19A10201
DDR_PI_462	DDR_PI_OFS	1CE	0x19A10302
DDR_PI_463	DDR_PI_OFS	1CF	0x19A10B04
DDR_PI_464	DDR_PI_OFS	1D0	0x19A1160E
DDR_PI_465	DDR_PI_OFS	1D1	0x181108F7
DDR_PI_466	DDR_PI_OFS	1D2	0x19A10D06
DDR_PI_467	DDR_PI_OFS	1D3	0x18051900
DDR_PI_468	DDR_PI_OFS	1D4	0x1800803F
DDR_PI_469	DDR_PI_OFS	1D5	0x19A01F1A
DDR_PI_470	DDR_PI_OFS	1D6	0x19A10C05

Register Name	Address Offset (_OFS)	n [hex] (_OFS + n)	V4M
DDR_PI_471	DDR_PI_OFS	1D7	0x10051F00
DDR_PI_472	DDR_PI_OFS	1D8	0x19A10E07
DDR_PI_473	DDR_PI_OFS	1D9	0x10051F00
DDR_PI_474	DDR_PI_OFS	1DA	0x1800403F
DDR_PI_475	DDR_PI_OFS	1DB	0x19A01F1A
DDR_PI_476	DDR_PI_OFS	1DC	0x19A00C00
DDR_PI_477	DDR_PI_OFS	1DD	0x10001F00
DDR_PI_478	DDR_PI_OFS	1DE	0x19A00E00
DDR_PI_479	DDR_PI_OFS	1DF	0x10001F00
DDR_PI_480	DDR_PI_OFS	1E0	0x19910280
DDR_PI_481	DDR_PI_OFS	1E1	0x19A20D06
DDR_PI_482	DDR_PI_OFS	1E2	0x18051000
DDR_PI_483	DDR_PI_OFS	1E3	0x18861101
DDR_PI_484	DDR_PI_OFS	1E4	0x181F0000
DDR_PI_485	DDR_PI_OFS	1E5	0x181F0000
DDR_PI_486	DDR_PI_OFS	1E6	0x181F0000
DDR_PI_487	DDR_PI_OFS	1E7	0x181F0000
DDR_PI_488	DDR_PI_OFS	1E8	0x181F0000
DDR_PI_489	DDR_PI_OFS	1E9	0x181F0000
DDR_PI_490	DDR_PI_OFS	1EA	0x181F0000
DDR_PI_491	DDR_PI_OFS	1EB	0x18861100
DDR_PI_492	DDR_PI_OFS	1EC	0x19A10D06
DDR_PI_493	DDR_PI_OFS	1ED	0x18051800
DDR_PI_494	DDR_PI_OFS	1EE	0x101B0001
DDR_PI_495	DDR_PI_OFS	1EF	0x181B0100
DDR_PI_496	DDR_PI_OFS	1F0	0x181B0200
DDR_PI_497	DDR_PI_OFS	1F1	0x181B0300
DDR_PI_498	DDR_PI_OFS	1F2	0x181B0400
DDR_PI_499	DDR_PI_OFS	1F3	0x1C440316
DDR_PI_500	DDR_PI_OFS	1F4	0x100D0000
DDR_PI_501	DDR_PI_OFS	1F5	0x101C0000
DDR_PI_502	DDR_PI_OFS	1F6	0x181F0000
DDR_PI_503	DDR_PI_OFS	1F7	0x181F0000
DDR_PI_504	DDR_PI_OFS	1F8	0x181F0000
DDR_PI_505	DDR_PI_OFS	1F9	0x181F0000
DDR_PI_506	DDR_PI_OFS	1FA	0x181F0000
DDR_PI_507	DDR_PI_OFS	1FB	0x181F0000
DDR_PI_508	DDR_PI_OFS	1FC	0x181F0000
DDR_PI_509	DDR_PI_OFS	1FD	0x181F0000
DDR_PI_510	DDR_PI_OFS	1FE	0x181F0000
DDR_PI_511	DDR_PI_OFS	1FF	0x181F0000
DDR_PI_512	DDR_PI_OFS	200	0x181F0000
DDR_PI_513	DDR_PI_OFS	201	0x181F0000
DDR_PI_514	DDR_PI_OFS	202	0x181F0000
d	DDR_PI_OFS	203	0x181F0000

Register Name	Address Offset (_OFS)	n [hex] (_OFS + n)	V4M
DDR_PI_516	DDR_PI_OFS	204	0x181F0000
DDR_PI_517	DDR_PI_OFS	205	0x09910260
DDR_PI_518	DDR_PI_OFS	206	0x11911600
DDR_PI_519	DDR_PI_OFS	207	0x19A20D06
DDR_PI_520	DDR_PI_OFS	208	0x18051900
DDR_PI_521	DDR_PI_OFS	209	0x19A10100
DDR_PI_522	DDR_PI_OFS	20A	0x19A10201
DDR_PI_523	DDR_PI_OFS	20B	0x19A10302
DDR_PI_524	DDR_PI_OFS	20C	0x19A10B04
DDR_PI_525	DDR_PI_OFS	20D	0x1800803F
DDR_PI_526	DDR_PI_OFS	20E	0x19A01F1A
DDR_PI_527	DDR_PI_OFS	20F	0x19A10C05
DDR_PI_528	DDR_PI_OFS	210	0x19A10E07
DDR_PI_529	DDR_PI_OFS	211	0x1800403F
DDR_PI_530	DDR_PI_OFS	212	0x19A01F1A
DDR_PI_531	DDR_PI_OFS	213	0x19A00C00
DDR_PI_532	DDR_PI_OFS	214	0x19A00E00
DDR_PI_533	DDR_PI_OFS	215	0x19A1160E
DDR_PI_534	DDR_PI_OFS	216	0x09A30012
DDR_PI_535	DDR_PI_OFS	217	0x199F0000
DDR_PI_536	DDR_PI_OFS	218	0x0011007F
DDR_PI_537	DDR_PI_OFS	219	0x01810201
DDR_PI_538	DDR_PI_OFS	21A	0x01800800
DDR_PI_539	DDR_PI_OFS	21B	0x01A00D06
DDR_PI_540	DDR_PI_OFS	21C	0x080D0000
DDR_PI_541	DDR_PI_OFS	21D	0x001F0000
DDR_PI_542	DDR_PI_OFS	21E	0x080C0000
DDR_PI_543	DDR_PI_OFS	21F	0x01800440
DDR_PI_544	DDR_PI_OFS	220	0x01A00D06
DDR_PI_545	DDR_PI_OFS	221	0x0011FF7F
DDR_PI_546	DDR_PI_OFS	222	0x01810201
DDR_PI_547	DDR_PI_OFS	223	0x001F0000
DDR_PI_548	DDR_PI_OFS	224	0x001F0200
DDR_PI_549	DDR_PI_OFS	225	0x00050000
DDR_PI_550	DDR_PI_OFS	226	0x00070100
DDR_PI_551	DDR_PI_OFS	227	0x00060200
DDR_PI_552	DDR_PI_OFS	228	0x00000000
DDR_PI_553	DDR_PI_OFS	229	0x00000000
DDR_PI_554	DDR_PI_OFS	22A	0x01A10201
DDR_PI_555	DDR_PI_OFS	22B	0x01A10B04
DDR_PI_556	DDR_PI_OFS	22C	0x01A1160E
DDR_PI_557	DDR_PI_OFS	22D	0x01A10302
DDR_PI_558	DDR_PI_OFS	22E	0x00090000
DDR_PI_559	DDR_PI_OFS	22F	0x00098000
DDR_PI_560	DDR_PI_OFS	230	0x019F0000

Register Name	Address Offset (_OFS)	n [hex] (_OFS + n)	V4M
DDR_PI_561	DDR_PI_OFS	231	0x019F0000
DDR_PI_562	DDR_PI_OFS	232	0x01A10201
DDR_PI_563	DDR_PI_OFS	233	0x01A10302
DDR_PI_564	DDR_PI_OFS	234	0x01A10D06
DDR_PI_565	DDR_PI_OFS	235	0x01A10100
DDR_PI_566	DDR_PI_OFS	236	0x00000000
DDR_PI_567	DDR_PI_OFS	237	0x00000000
DDR_PI_568	DDR_PI_OFS	238	0x000A0808
DDR_PI_569	DDR_PI_OFS	239	0x00058032
DDR_PI_570	DDR_PI_OFS	23A	0x001F0000
DDR_PI_571	DDR_PI_OFS	23B	0x001F0000
DDR_PI_572	DDR_PI_OFS	23C	0x001F0000
DDR_PI_573	DDR_PI_OFS	23D	0x001F0000
DDR_PI_574	DDR_PI_OFS	23E	0x001F0000
DDR_PI_575	DDR_PI_OFS	23F	0x001F0000
DDR_PI_576	DDR_PI_OFS	240	0x001F0000
DDR_PI_577	DDR_PI_OFS	241	0x001F0000
DDR_PI_578	DDR_PI_OFS	242	0x000A0000
DDR_PI_579	DDR_PI_OFS	243	0x00060000
DDR_PI_580	DDR_PI_OFS	244	0x000D0000
DDR_PI_581	DDR_PI_OFS	245	0x001C0000
DDR_PI_582	DDR_PI_OFS	246	0x001F0000
DDR_PI_583	DDR_PI_OFS	247	0x001F0000
DDR_PI_584	DDR_PI_OFS	248	0x001F0000
DDR_PI_585	DDR_PI_OFS	249	0x001F0000
DDR_PI_586	DDR_PI_OFS	24A	0x001F0000
DDR_PI_587	DDR_PI_OFS	24B	0x01910305
DDR_PI_588	DDR_PI_OFS	24C	0x01A20D06
DDR_PI_589	DDR_PI_OFS	24D	0x019F0000
DDR_PI_590	DDR_PI_OFS	24E	0x0011FFF7
DDR_PI_591	DDR_PI_OFS	24F	0x01810D06
DDR_PI_592	DDR_PI_OFS	250	0x00051900
DDR_PI_593	DDR_PI_OFS	251	0x0000803F
DDR_PI_594	DDR_PI_OFS	252	0x01A01F1A
DDR_PI_595	DDR_PI_OFS	253	0x01A10C05
DDR_PI_596	DDR_PI_OFS	254	0x00051F00
DDR_PI_597	DDR_PI_OFS	255	0x0000403F
DDR_PI_598	DDR_PI_OFS	256	0x01A01F1A
DDR_PI_599	DDR_PI_OFS	257	0x01A00C00
DDR_PI_600	DDR_PI_OFS	258	0x00001F00
DDR_PI_601	DDR_PI_OFS	259	0x001100F7
DDR_PI_602	DDR_PI_OFS	25A	0x01810D06
DDR_PI_603	DDR_PI_OFS	25B	0x00051800
DDR_PI_604	DDR_PI_OFS	25C	0x019F0000
DDR_PI_605	DDR_PI_OFS	25D	0x01510001

Register Name	Address Offset (_OFS)	n [hex] (_OFS + n)	V4M
DDR_PI_606	DDR_PI_OFS	25E	0x01D102A0
DDR_PI_607	DDR_PI_OFS	25F	0x01E20D06
DDR_PI_608	DDR_PI_OFS	260	0x00051900
DDR_PI_609	DDR_PI_OFS	261	0x019F0000
DDR_PI_610	DDR_PI_OFS	262	0x01510001
DDR_PI_611	DDR_PI_OFS	263	0x01D10290
DDR_PI_612	DDR_PI_OFS	264	0x01E20D06
DDR_PI_613	DDR_PI_OFS	265	0x00051900
DDR_PI_614	DDR_PI_OFS	266	0x01510001
DDR_PI_615	DDR_PI_OFS	267	0x01D10000
DDR_PI_616	DDR_PI_OFS	268	0x01E20D06
DDR_PI_617	DDR_PI_OFS	269	0x00051800
DDR_PI_618	DDR_PI_OFS	26A	0x019F0000
DDR_PI_619	DDR_PI_OFS	26B	0x001100F6
DDR_PI_620	DDR_PI_OFS	26C	0x01810D06
DDR_PI_621	DDR_PI_OFS	26D	0x00051800
DDR_PI_622	DDR_PI_OFS	26E	0x01910000
DDR_PI_623	DDR_PI_OFS	26F	0x01A20D06
DDR_PI_624	DDR_PI_OFS	270	0x019F0000
DDR_PI_625	DDR_PI_OFS	271	0x01911000
DDR_PI_626	DDR_PI_OFS	272	0x01A20D06
DDR_PI_627	DDR_PI_OFS	273	0x01A10100
DDR_PI_628	DDR_PI_OFS	274	0x01A10201
DDR_PI_629	DDR_PI_OFS	275	0x01A10302
DDR_PI_630	DDR_PI_OFS	276	0x01A10B04
DDR_PI_631	DDR_PI_OFS	277	0x0000803F
DDR_PI_632	DDR_PI_OFS	278	0x01A01F1A
DDR_PI_633	DDR_PI_OFS	279	0x01A10C05
DDR_PI_634	DDR_PI_OFS	27A	0x01A10E07
DDR_PI_635	DDR_PI_OFS	27B	0x0000403F
DDR_PI_636	DDR_PI_OFS	27C	0x01A01F1A
DDR_PI_637	DDR_PI_OFS	27D	0x01A00C00
DDR_PI_638	DDR_PI_OFS	27E	0x01A00E00
DDR_PI_639	DDR_PI_OFS	27F	0x01A1160E
DDR_PI_640	DDR_PI_OFS	280	0x01910800
DDR_PI_641	DDR_PI_OFS	281	0x01A20D06
DDR_PI_642	DDR_PI_OFS	282	0x019F0000
DDR_PI_643	DDR_PI_OFS	283	0x019F0000
DDR_PI_644	DDR_PI_OFS	284	0x001F0000
DDR_PI_645	DDR_PI_OFS	285	0x001F0000
DDR_PI_646	DDR_PI_OFS	286	0x001F0000
DDR_PI_647	DDR_PI_OFS	287	0x001F0000
DDR_PI_648	DDR_PI_OFS	288	0x001F0200
DDR_PI_649	DDR_PI_OFS	289	0x001102FD
DDR_PI_650	DDR_PI_OFS	28A	0x01A10D06

Register Name	Address Offset (_OFS)	n [hex] (_OFS + n)	V4M
DDR_PI_651	DDR_PI_OFS	28B	0x001F0000
DDR_PI_652	DDR_PI_OFS	28C	0x01A10D06
DDR_PI_653	DDR_PI_OFS	28D	0x00051300
DDR_PI_654	DDR_PI_OFS	28E	0x001F0000
DDR_PI_655	DDR_PI_OFS	28F	0x001F0000
DDR_PI_656	DDR_PI_OFS	290	0x001F0000
DDR_PI_657	DDR_PI_OFS	291	0x001F0000
DDR_PI_658	DDR_PI_OFS	292	0x00210F08
DDR_PI_659	DDR_PI_OFS	293	0x0021140D
DDR_PI_660	DDR_PI_OFS	294	0x00212015
DDR_PI_661	DDR_PI_OFS	295	0x00212818
DDR_PI_662	DDR_PI_OFS	296	0x001F0000
DDR_PI_663	DDR_PI_OFS	297	0x001F0000
DDR_PI_664	DDR_PI_OFS	298	0x00210F08
DDR_PI_665	DDR_PI_OFS	299	0x0021140D
DDR_PI_666	DDR_PI_OFS	29A	0x00212015
DDR_PI_667	DDR_PI_OFS	29B	0x00212818
DDR_PI_668	DDR_PI_OFS	29C	0x001F0000
DDR_PI_669	DDR_PI_OFS	29D	0x001A84FF
DDR_PI_670	DDR_PI_OFS	29E	0x001F0000
DDR_PI_671	DDR_PI_OFS	29F	0x01800440
DDR_PI_672	DDR_PI_OFS	2A0	0x01A00D06
DDR_PI_673	DDR_PI_OFS	2A1	0x001F0000
DDR_PI_674	DDR_PI_OFS	2A2	0x001F0000
DDR_PI_675	DDR_PI_OFS	2A3	0x001F0000
DDR_PI_676	DDR_PI_OFS	2A4	0x001F0000
DDR_PI_677	DDR_PI_OFS	2A5	0x001F0000
DDR_PI_678	DDR_PI_OFS	2A6	0x01800800
DDR_PI_679	DDR_PI_OFS	2A7	0x01A00D06
DDR_PI_680	DDR_PI_OFS	2A8	0x001F0000
DDR_PI_681	DDR_PI_OFS	2A9	0x001F0000
DDR_PI_682	DDR_PI_OFS	2AA	0x001F0000
DDR_PI_683	DDR_PI_OFS	2AB	0x00031200
DDR_PI_684	DDR_PI_OFS	2AC	0x00031300
DDR_PI_685	DDR_PI_OFS	2AD	0x001F0000
DDR_PI_686	DDR_PI_OFS	2AE	0x0031FFF7
DDR_PI_687	DDR_PI_OFS	2AF	0x01A10D06
DDR_PI_688	DDR_PI_OFS	2B0	0x00051900
DDR_PI_689	DDR_PI_OFS	2B1	0x0000803F
DDR_PI_690	DDR_PI_OFS	2B2	0x01A01F1A
DDR_PI_691	DDR_PI_OFS	2B3	0x01A10E07
DDR_PI_692	DDR_PI_OFS	2B4	0x00051F00
DDR_PI_693	DDR_PI_OFS	2B5	0x0000403F
DDR_PI_694	DDR_PI_OFS	2B6	0x01A01F1A
DDR_PI_695	DDR_PI_OFS	2B7	0x01A00E00

Register Name	Address Offset (_OFS)	n [hex] (_OFS + n)	V4M
DDR_PI_696	DDR_PI_OFS	2B8	0x00001F00
DDR_PI_697	DDR_PI_OFS	2B9	0x003100F7
DDR_PI_698	DDR_PI_OFS	2BA	0x01A10D06
DDR_PI_699	DDR_PI_OFS	2BB	0x00051800
DDR_PI_700	DDR_PI_OFS	2BC	0x003F0000
DDR_PI_701	DDR_PI_OFS	2BD	0x0031FFF7
DDR_PI_702	DDR_PI_OFS	2BE	0x01A10D06
DDR_PI_703	DDR_PI_OFS	2BF	0x00051900
DDR_PI_704	DDR_PI_OFS	2C0	0x0000803F
DDR_PI_705	DDR_PI_OFS	2C1	0x01A01F1A
DDR_PI_706	DDR_PI_OFS	2C2	0x01A10E07
DDR_PI_707	DDR_PI_OFS	2C3	0x00051F00
DDR_PI_708	DDR_PI_OFS	2C4	0x0000403F
DDR_PI_709	DDR_PI_OFS	2C5	0x01A01F1A
DDR_PI_710	DDR_PI_OFS	2C6	0x01A00E00
DDR_PI_711	DDR_PI_OFS	2C7	0x00001F00
DDR_PI_712	DDR_PI_OFS	2C8	0x003100F7
DDR_PI_713	DDR_PI_OFS	2C9	0x01A10D06
DDR_PI_714	DDR_PI_OFS	2CA	0x00051800
DDR_PI_715	DDR_PI_OFS	2CB	0x003F0000
DDR_PI_716	DDR_PI_OFS	2CC	0x001100EF
DDR_PI_717	DDR_PI_OFS	2CD	0x0001120B
DDR_PI_718	DDR_PI_OFS	2CE	0x00051400
DDR_PI_719	DDR_PI_OFS	2CF	0x001A0800
DDR_PI_720	DDR_PI_OFS	2D0	0x001102FD
DDR_PI_721	DDR_PI_OFS	2D1	0x00012E00
DDR_PI_722	DDR_PI_OFS	2D2	0x00000000
DDR_PI_723	DDR_PI_OFS	2D3	0x001F0000
DDR_PI_724	DDR_PI_OFS	2D4	0x001100FD
DDR_PI_725	DDR_PI_OFS	2D5	0x00012E00
DDR_PI_726	DDR_PI_OFS	2D6	0x00051700
DDR_PI_727	DDR_PI_OFS	2D7	0x001A0801
DDR_PI_728	DDR_PI_OFS	2D8	0x0001120B
DDR_PI_729	DDR_PI_OFS	2D9	0x001F0000
DDR_PI_730	DDR_PI_OFS	2DA	0x001100EF
DDR_PI_731	DDR_PI_OFS	2DB	0x0001120B
DDR_PI_732	DDR_PI_OFS	2DC	0x00051400
DDR_PI_733	DDR_PI_OFS	2DD	0x001A0800
DDR_PI_734	DDR_PI_OFS	2DE	0x001101FC
DDR_PI_735	DDR_PI_OFS	2DF	0x00011A00
DDR_PI_736	DDR_PI_OFS	2E0	0x00000000
DDR_PI_737	DDR_PI_OFS	2E1	0x001F0000
DDR_PI_738	DDR_PI_OFS	2E2	0x00051500
DDR_PI_739	DDR_PI_OFS	2E3	0x001103FC
DDR_PI_740	DDR_PI_OFS	2E4	0x00011A00

Register Name	Address Offset (_OFS)	n [hex] (_OFS + n)	V4M
DDR_PI_741	DDR_PI_OFS	2E5	0x00051500
DDR_PI_742	DDR_PI_OFS	2E6	0x001102FC
DDR_PI_743	DDR_PI_OFS	2E7	0x00011A00
DDR_PI_744	DDR_PI_OFS	2E8	0x00001A00
DDR_PI_745	DDR_PI_OFS	2E9	0x00000000
DDR_PI_746	DDR_PI_OFS	2EA	0x001F0000
DDR_PI_747	DDR_PI_OFS	2EB	0x001100FC
DDR_PI_748	DDR_PI_OFS	2EC	0x00011A00
DDR_PI_749	DDR_PI_OFS	2ED	0x001A0801
DDR_PI_750	DDR_PI_OFS	2EE	0x0001120B
DDR_PI_751	DDR_PI_OFS	2EF	0x00000000
DDR_PI_752	DDR_PI_OFS	2F0	0x001F0000
DDR_PI_753	DDR_PI_OFS	2F1	0x001108E7
DDR_PI_754	DDR_PI_OFS	2F2	0x0001120B
DDR_PI_755	DDR_PI_OFS	2F3	0x00051400
DDR_PI_756	DDR_PI_OFS	2F4	0x01910480
DDR_PI_757	DDR_PI_OFS	2F5	0x00021009
DDR_PI_758	DDR_PI_OFS	2F6	0x001F0000
DDR_PI_759	DDR_PI_OFS	2F7	0x001A0800
DDR_PI_760	DDR_PI_OFS	2F8	0x00211E00
DDR_PI_761	DDR_PI_OFS	2F9	0x001101FC
DDR_PI_762	DDR_PI_OFS	2FA	0x00211A00
DDR_PI_763	DDR_PI_OFS	2FB	0x00051500
DDR_PI_764	DDR_PI_OFS	2FC	0x001103FC
DDR_PI_765	DDR_PI_OFS	2FD	0x00011A00
DDR_PI_766	DDR_PI_OFS	2FE	0x00051500
DDR_PI_767	DDR_PI_OFS	2FF	0x001100FC
DDR_PI_768	DDR_PI_OFS	300	0x00011A00
DDR_PI_769	DDR_PI_OFS	301	0x00031A00
DDR_PI_770	DDR_PI_OFS	302	0x001A0801
DDR_PI_771	DDR_PI_OFS	303	0x00000000
DDR_PI_772	DDR_PI_OFS	304	0x001F0000
DDR_PI_773	DDR_PI_OFS	305	0x00211E00
DDR_PI_774	DDR_PI_OFS	306	0x001108F7
DDR_PI_775	DDR_PI_OFS	307	0x0001120B
DDR_PI_776	DDR_PI_OFS	308	0x001F0000
DDR_PI_777	DDR_PI_OFS	309	0x00000000
DDR_PI_778	DDR_PI_OFS	30A	0x00000000
DDR_PI_779	DDR_PI_OFS	30B	0x00000000
DDR_PI_780	DDR_PI_OFS	30C	0x00000000
DDR_PI_781	DDR_PI_OFS	30D	0x00000000
DDR_PI_782	DDR_PI_OFS	30E	0x00000000
DDR_PI_783	DDR_PI_OFS	30F	0x00000000
DDR_PI_784	DDR_PI_OFS	310	0x00000000
DDR_PI_785	DDR_PI_OFS	311	0x00000000

Register Name	Address Offset (_OFS)	n [hex] (_OFS + n)	V4M
DDR_PI_786	DDR_PI_OFS	312	0x001F0000
DDR_PI_787	DDR_PI_OFS	313	0x0404FF7F
DDR_PI_788	DDR_PI_OFS	314	0x0404FF7F
DDR_PI_789	DDR_PI_OFS	315	0x0404FF7F
DDR_PI_790	DDR_PI_OFS	316	0x0404FF7F
DDR_PI_791	DDR_PI_OFS	317	0x0404FF7F
DDR_PI_792	DDR_PI_OFS	318	0x0404FF7F
DDR_PI_793	DDR_PI_OFS	319	0x0404FF7F
DDR_PI_794	DDR_PI_OFS	31A	0x0404FF7F
DDR_PI_795	DDR_PI_OFS	31B	0x00000000
DDR_PI_796	DDR_PI_OFS	31C	0x00000000
DDR_PI_797	DDR_PI_OFS	31D	0x00000000
DDR_PI_798	DDR_PI_OFS	31E	0x00000000
DDR_PI_799	DDR_PI_OFS	31F	0x00000000
DDR_PI_800	DDR_PI_OFS	320	0x00000000
DDR_PI_801	DDR_PI_OFS	321	0x00000000
DDR_PI_802	DDR_PI_OFS	322	0x00000000
DDR_PI_803	DDR_PI_OFS	323	0x00000000
DDR_PI_804	DDR_PI_OFS	324	0x00000000
DDR_PI_805	DDR_PI_OFS	325	0x00000000
DDR_PI_806	DDR_PI_OFS	326	0x00000000
DDR_PI_807	DDR_PI_OFS	327	0x00000000
DDR_PI_808	DDR_PI_OFS	328	0x00000000
DDR_PI_809	DDR_PI_OFS	329	0x00000000
DDR_PI_810	DDR_PI_OFS	32A	0x00000000
DDR_PI_811	DDR_PI_OFS	32B	0x00000000
DDR_PI_812	DDR_PI_OFS	32C	0x00000000
DDR_PI_813	DDR_PI_OFS	32D	0x00000000
DDR_PI_814	DDR_PI_OFS	32E	0x00000000
DDR_PI_815	DDR_PI_OFS	32F	0x00000000
DDR_PI_816	DDR_PI_OFS	330	0x00000000
DDR_PI_817	DDR_PI_OFS	331	0x00000000
DDR_PI_818	DDR_PI_OFS	332	0x00000000
DDR_PI_819	DDR_PI_OFS	333	0x00000000
DDR_PI_820	DDR_PI_OFS	334	0x00000000
DDR_PI_821	DDR_PI_OFS	335	0x00000000
DDR_PI_822	DDR_PI_OFS	336	0x00000000
DDR_PI_823	DDR_PI_OFS	337	0x00000000
DDR_PI_824	DDR_PI_OFS	338	0x00000000
DDR_PI_825	DDR_PI_OFS	339	0x00000000
DDR_PI_826	DDR_PI_OFS	33A	0x00000000
DDR_PI_827	DDR_PI_OFS	33B	0x00000000
DDR_PI_828	DDR_PI_OFS	33C	0x00000000
DDR_PI_829	DDR_PI_OFS	33D	0x00000000
DDR_PI_830	DDR_PI_OFS	33E	0x00000000

Register Name	Address Offset (_OFS)	n [hex] (_OFS + n)	V4M
DDR_PI_831	DDR_PI_OFS	33F	0x00000000
DDR_PI_832	DDR_PI_OFS	340	0x00000000
DDR_PI_833	DDR_PI_OFS	341	0x00000000
DDR_PI_834	DDR_PI_OFS	342	0x00000000
DDR_PI_835	DDR_PI_OFS	343	0x00000000
DDR_PI_836	DDR_PI_OFS	344	0x00000000
DDR_PI_837	DDR_PI_OFS	345	0x00000000
DDR_PI_838	DDR_PI_OFS	346	0x00000000
DDR_PI_839	DDR_PI_OFS	347	0x00000000
DDR_PI_840	DDR_PI_OFS	348	0x00000000
DDR_PI_841	DDR_PI_OFS	349	0x00000000
DDR_PI_842	DDR_PI_OFS	34A	0x00000000
DDR_PI_843	DDR_PI_OFS	34B	0x00000000
DDR_PI_844	DDR_PI_OFS	34C	0x00000000
DDR_PI_845	DDR_PI_OFS	34D	0x00000000
DDR_PI_846	DDR_PI_OFS	34E	0x00000000
DDR_PI_847	DDR_PI_OFS	34F	0x00000000
DDR_PI_848	DDR_PI_OFS	350	0x00000000
DDR_PI_849	DDR_PI_OFS	351	0x00000000
DDR_PI_850	DDR_PI_OFS	352	0x00000000
DDR_PI_851	DDR_PI_OFS	353	0x00000000
DDR_PI_852	DDR_PI_OFS	354	0x00000000
DDR_PI_853	DDR_PI_OFS	355	0x00000000
DDR_PI_854	DDR_PI_OFS	356	0x00000000
DDR_PI_855	DDR_PI_OFS	357	0x00000000
DDR_PI_856	DDR_PI_OFS	358	0x00000000
DDR_PI_857	DDR_PI_OFS	359	0x00000000
DDR_PI_858	DDR_PI_OFS	35A	0x00000000
DDR_PI_859	DDR_PI_OFS	35B	0x00000000
DDR_PI_860	DDR_PI_OFS	35C	0x00000000
DDR_PI_861	DDR_PI_OFS	35D	0x00000000
DDR_PI_862	DDR_PI_OFS	35E	0x00000000
DDR_PI_863	DDR_PI_OFS	35F	0x00000000
DDR_PI_864	DDR_PI_OFS	360	0x00000000
DDR_PI_865	DDR_PI_OFS	361	0x00000000
DDR_PI_866	DDR_PI_OFS	362	0x00000000
DDR_PI_867	DDR_PI_OFS	363	0x00000000
DDR_PI_868	DDR_PI_OFS	364	0x00000000
DDR_PI_869	DDR_PI_OFS	365	0x00000000
DDR_PI_870	DDR_PI_OFS	366	0x00000000
DDR_PI_871	DDR_PI_OFS	367	0x00000000
DDR_PI_872	DDR_PI_OFS	368	0x00000000
DDR_PI_873	DDR_PI_OFS	369	0x00000000
DDR_PI_874	DDR_PI_OFS	36A	0x00000000
DDR_PI_875	DDR_PI_OFS	36B	0x00000000

Register Name	Address Offset (_OFS)	n [hex] (_OFS + n)	V4M
DDR_PI_876	DDR_PI_OFS	36C	0x00000000
DDR_PI_877	DDR_PI_OFS	36D	0x00000000
DDR_PI_878	DDR_PI_OFS	36E	0x00000000
DDR_PI_879	DDR_PI_OFS	36F	0x00000000
DDR_PI_880	DDR_PI_OFS	370	0x00000000
DDR_PI_881	DDR_PI_OFS	371	0x00000000
DDR_PI_882	DDR_PI_OFS	372	0x00000000
DDR_PI_883	DDR_PI_OFS	373	0x00000000
DDR_PI_884	DDR_PI_OFS	374	0x00000000
DDR_PI_885	DDR_PI_OFS	375	0x00000000
DDR_PI_886	DDR_PI_OFS	376	0x00000000
DDR_PI_887	DDR_PI_OFS	377	0x00000000
DDR_PI_888	DDR_PI_OFS	378	0x00000000
DDR_PI_889	DDR_PI_OFS	379	0x00000000
DDR_PI_890	DDR_PI_OFS	37A	0x00000000
DDR_PI_891	DDR_PI_OFS	37B	0x00000000
DDR_PI_892	DDR_PI_OFS	37C	0x00000000
DDR_PI_893	DDR_PI_OFS	37D	0x00000000
DDR_PI_894	DDR_PI_OFS	37E	0x00000000
DDR_PI_895	DDR_PI_OFS	37F	0x00000000
DDR_PI_896	DDR_PI_OFS	380	0x00000000
DDR_PI_897	DDR_PI_OFS	381	0x00000000
DDR_PI_898	DDR_PI_OFS	382	0x00070000
DDR_PI_899	DDR_PI_OFS	383	0x0011000B
DDR_PI_900	DDR_PI_OFS	384	0x001D0017
DDR_PI_901	DDR_PI_OFS	385	0x0059003F
DDR_PI_902	DDR_PI_OFS	386	0x0072006C
DDR_PI_903	DDR_PI_OFS	387	0x00790078
DDR_PI_904	DDR_PI_OFS	388	0x00960086
DDR_PI_905	DDR_PI_OFS	389	0x00A2009F
DDR_PI_906	DDR_PI_OFS	38A	0x00B600B1
DDR_PI_907	DDR_PI_OFS	38B	0x00C500BF
DDR_PI_908	DDR_PI_OFS	38C	0x00DC00D8
DDR_PI_909	DDR_PI_OFS	38D	0x00E000DD
DDR_PI_910	DDR_PI_OFS	38E	0x00E600E3
DDR_PI_911	DDR_PI_OFS	38F	0x00F100EC
DDR_PI_912	DDR_PI_OFS	390	0x00FA00F3
DDR_PI_913	DDR_PI_OFS	391	0x010200FF
DDR_PI_914	DDR_PI_OFS	392	0x01200111
DDR_PI_915	DDR_PI_OFS	393	0x012E0128
DDR_PI_916	DDR_PI_OFS	394	0x013F0136
DDR_PI_917	DDR_PI_OFS	395	0x014B0145
DDR_PI_918	DDR_PI_OFS	396	0x015D0159
DDR_PI_919	DDR_PI_OFS	397	0x01680167
DDR_PI_920	DDR_PI_OFS	398	0x016A0169

Register Name	Address Offset (_OFS)	n [hex] (_OFS + n)	V4M
DDR_PI_921	DDR_PI_OFS	399	0x016C016B
DDR_PI_922	DDR_PI_OFS	39A	0x016E016D
DDR_PI_923	DDR_PI_OFS	39B	0x00000000
DDR_PI_924	DDR_PI_OFS	39C	0x00000000
DDR_PI_925	DDR_PI_OFS	39D	0x004B1040
DDR_PI_926	DDR_PI_OFS	39E	0x000811C0
DDR_PI_927	DDR_PI_OFS	39F	0x040811C0
DDR_PI_928	DDR_PI_OFS	3A0	0x02000000
DDR_PI_929	DDR_PI_OFS	3A1	0x00000000
DDR_PI_930	DDR_PI_OFS	3A2	0x00000000
DDR_PI_931	DDR_PI_OFS	3A3	0x00000000
DDR_PI_932	DDR_PI_OFS	3A4	0x00000000
DDR_PI_933	DDR_PI_OFS	3A5	0x00000000
DDR_PI_934	DDR_PI_OFS	3A6	0x00000000
DDR_PI_935	DDR_PI_OFS	3A7	0x00000000
DDR_PI_936	DDR_PI_OFS	3A8	0x00000000
DDR_PI_937	DDR_PI_OFS	3A9	0x00000000
DDR_PI_938	DDR_PI_OFS	3AA	0x00000000
DDR_PI_939	DDR_PI_OFS	3AB	0x00000000
DDR_PI_940	DDR_PI_OFS	3AC	0x00000000
DDR_PI_941	DDR_PI_OFS	3AD	0x00000000
DDR_PI_942	DDR_PI_OFS	3AE	0x00000000
DDR_PI_943	DDR_PI_OFS	3AF	0x00000000
DDR_PI_944	DDR_PI_OFS	3B0	0x00000000
DDR_PI_945	DDR_PI_OFS	3B1	0x00000000
DDR_PI_946	DDR_PI_OFS	3B2	0x00000000
DDR_PI_947	DDR_PI_OFS	3B3	0x5F407FAA
DDR_PI_948	DDR_PI_OFS	3B4	0x007B776F
DDR_PI_949	DDR_PI_OFS	3B5	0x4AB555AA
DDR_PI_950	DDR_PI_OFS	3B6	0xB5A9A956
DDR_PI_951	DDR_PI_OFS	3B7	0x9F80BFAA
DDR_PI_952	DDR_PI_OFS	3B8	0x00BBB7AF
DDR_PI_953	DDR_PI_OFS	3B9	0x00000000
DDR_PI_954	DDR_PI_OFS	3BA	0x00000000
DDR_PI_955	DDR_PI_OFS	3BB	0x00000000
DDR_PI_956	DDR_PI_OFS	3BC	0x00000000
DDR_PI_957	DDR_PI_OFS	3BD	0x00000000
DDR_PI_958	DDR_PI_OFS	3BE	0x00000000
DDR_PI_959	DDR_PI_OFS	3BF	0x00000000
DDR_PI_960	DDR_PI_OFS	3C0	0x00000000
DDR_PI_961	DDR_PI_OFS	3C1	0x00002AF8
DDR_PI_962	DDR_PI_OFS	3C2	0x00006B6B
DDR_PI_963	DDR_PI_OFS	3C3	0x0000006E
DDR_PI_964	DDR_PI_OFS	3C4	0x00000000
DDR_PI_965	DDR_PI_OFS	3C5	0x00000000

Register Name	Address Offset (_OFS)	n [hex] (_OFS + n)	V4M
DDR_PI_966	DDR_PI_OFS	3C6	0x00000000
DDR_PI_967	DDR_PI_OFS	3C7	0x00000000
DDR_PI_968	DDR_PI_OFS	3C8	0x00000000
DDR_PI_969	DDR_PI_OFS	3C9	0x00000000
DDR_PI_970	DDR_PI_OFS	3CA	0x00000000
DDR_PI_971	DDR_PI_OFS	3CB	0x00000000
DDR_PI_972	DDR_PI_OFS	3CC	0x00000000
DDR_PI_973	DDR_PI_OFS	3CD	0x00000000
DDR_PI_974	DDR_PI_OFS	3CE	0x00000000
DDR_PI_975	DDR_PI_OFS	3CF	0x00000000
DDR_PI_976	DDR_PI_OFS	3D0	0x00000000
DDR_PI_977	DDR_PI_OFS	3D1	0x0000000E
DDR_PI_978	DDR_PI_OFS	3D2	0x000000C8
DDR_PI_979	DDR_PI_OFS	3D3	0x00000216
DDR_PI_980	DDR_PI_OFS	3D4	0x00000001
DDR_PI_981	DDR_PI_OFS	3D5	0x00000003
DDR_PI_982	DDR_PI_OFS	3D6	0x00000007
DDR_PI_983	DDR_PI_OFS	3D7	0x00000007
DDR_PI_984	DDR_PI_OFS	3D8	0x00000009
DDR_PI_985	DDR_PI_OFS	3D9	0x00000013
DDR_PI_986	DDR_PI_OFS	3DA	0x00000002
DDR_PI_987	DDR_PI_OFS	3DB	0x00000010
DDR_PI_988	DDR_PI_OFS	3DC	0x0000002B
DDR_PI_989	DDR_PI_OFS	3DD	0x00000000
DDR_PI_990	DDR_PI_OFS	3DE	0x00000000
DDR_PI_991	DDR_PI_OFS	3DF	0x00000000
DDR_PI_992	DDR_PI_OFS	3E0	0x00000000
DDR_PI_993	DDR_PI_OFS	3E1	0x00000000
DDR_PI_994	DDR_PI_OFS	3E2	0x00000000
DDR_PI_995	DDR_PI_OFS	3E3	0x00000000
DDR_PI_996	DDR_PI_OFS	3E4	0x00000000
DDR_PI_997	DDR_PI_OFS	3E5	0x00000000
DDR_PI_998	DDR_PI_OFS	3E6	0x00000000
DDR_PI_999	DDR_PI_OFS	3E7	0x00000000
DDR_PI_1000	DDR_PI_OFS	3E8	0x00000000
DDR_PI_1001	DDR_PI_OFS	3E9	0x00000007
DDR_PI_1002	DDR_PI_OFS	3EA	0x00000051
DDR_PI_1003	DDR_PI_OFS	3EB	0x000000D7
DDR_PI_1004	DDR_PI_OFS	3EC	0x0000000C
DDR_PI_1005	DDR_PI_OFS	3ED	0x000000A1
DDR_PI_1006	DDR_PI_OFS	3EE	0x000001AC
DDR_PI_1007	DDR_PI_OFS	3EF	0x00000000
DDR_PI_1008	DDR_PI_OFS	3F0	0x00000000
DDR_PI_1009	DDR_PI_OFS	3F1	0x00000009
DDR_PI_1010	DDR_PI_OFS	3F2	0x00000000

Register Name	Address Offset (_OFS)	n [hex] (_OFS + n)	V4M
DDR_PI_1011	DDR_PI_OFS	3F3	0x00000000
DDR_PI_1012	DDR_PI_OFS	3F4	0x00000000
DDR_PI_1013	DDR_PI_OFS	3F5	0x00000000
DDR_PI_1014	DDR_PI_OFS	3F6	0x00000000
DDR_PI_1015	DDR_PI_OFS	3F7	0x00000000
DDR_PI_1016	DDR_PI_OFS	3F8	0x00000000
DDR_PI_1017	DDR_PI_OFS	3F9	0x00000000
DDR_PI_1018	DDR_PI_OFS	3FA	0x00000000
DDR_PI_1019	DDR_PI_OFS	3FB	0x00000000
DDR_PI_1020	DDR_PI_OFS	3FC	0x00000000
DDR_PI_1021	DDR_PI_OFS	3FD	0x00000000
DDR_PI_1022	DDR_PI_OFS	3FE	0x0000000F
DDR_PI_1023	DDR_PI_OFS	3FF	0x000000C9
DDR_PI_1024	DDR_PI_OFS	400	0x00000217
DDR_PI_1025	DDR_PI_OFS	401	0x00000000
DDR_PI_1026	DDR_PI_OFS	402	0x00000000
DDR_PI_1027	DDR_PI_OFS	403	0x00000000
DDR_PI_1028	DDR_PI_OFS	404	0x00000000
DDR_PI_1029	DDR_PI_OFS	405	0x00000000
DDR_PI_1030	DDR_PI_OFS	406	0x00000000
DDR_PI_1031	DDR_PI_OFS	407	0x00000000
DDR_PI_1032	DDR_PI_OFS	408	0x00000000
DDR_PI_1033	DDR_PI_OFS	409	0x00000000
DDR_PI_1034	DDR_PI_OFS	40A	0x00000000
DDR_PI_1035	DDR_PI_OFS	40B	0x00000000
DDR_PI_1036	DDR_PI_OFS	40C	0x00000000
DDR_PI_1037	DDR_PI_OFS	40D	0x00250011
DDR_PI_1038	DDR_PI_OFS	40E	0x00080043
DDR_PI_1039	DDR_PI_OFS	40F	0x00100008
DDR_PI_1040	DDR_PI_OFS	410	0x001E0016
DDR_PI_1041	DDR_PI_OFS	411	0x00160032
DDR_PI_1042	DDR_PI_OFS	412	0x0032001E
DDR_PI_1043	DDR_PI_OFS	413	0x0012000E
DDR_PI_1044	DDR_PI_OFS	414	0x00080029
DDR_PI_1045	DDR_PI_OFS	415	0x00080008
DDR_PI_1046	DDR_PI_OFS	416	0x00080008
DDR_PI_1047	DDR_PI_OFS	417	0x00080008
DDR_PI_1048	DDR_PI_OFS	418	0x00080008
DDR_PI_1049	DDR_PI_OFS	419	0x00080008
DDR_PI_1050	DDR_PI_OFS	41A	0x00110008
DDR_PI_1051	DDR_PI_OFS	41B	0x00430025
DDR_PI_1052	DDR_PI_OFS	41C	0x00080008
DDR_PI_1053	DDR_PI_OFS	41D	0x00160010
DDR_PI_1054	DDR_PI_OFS	41E	0x0032001E
DDR_PI_1055	DDR_PI_OFS	41F	0x001E0016

Register Name	Address Offset (_OFS)	n [hex] (_OFS + n)	V4M
DDR_PI_1056	DDR_PI_OFS	420	0x000E0032
DDR_PI_1057	DDR_PI_OFS	421	0x00290012
DDR_PI_1058	DDR_PI_OFS	422	0x00080008
DDR_PI_1059	DDR_PI_OFS	423	0x00080008
DDR_PI_1060	DDR_PI_OFS	424	0x00080008
DDR_PI_1061	DDR_PI_OFS	425	0x00080008
DDR_PI_1062	DDR_PI_OFS	426	0x00080008
DDR_PI_1063	DDR_PI_OFS	427	0x00080008
DDR_PI_1064	DDR_PI_OFS	428	0x00250011
DDR_PI_1065	DDR_PI_OFS	429	0x00080043
DDR_PI_1066	DDR_PI_OFS	42A	0x00100008
DDR_PI_1067	DDR_PI_OFS	42B	0x001E0016
DDR_PI_1068	DDR_PI_OFS	42C	0x00160032
DDR_PI_1069	DDR_PI_OFS	42D	0x0032001E
DDR_PI_1070	DDR_PI_OFS	42E	0x0012000E
DDR_PI_1071	DDR_PI_OFS	42F	0x00080029
DDR_PI_1072	DDR_PI_OFS	430	0x00080008
DDR_PI_1073	DDR_PI_OFS	431	0x00080008
DDR_PI_1074	DDR_PI_OFS	432	0x00080008
DDR_PI_1075	DDR_PI_OFS	433	0x00080008
DDR_PI_1076	DDR_PI_OFS	434	0x00080008
DDR_PI_1077	DDR_PI_OFS	435	0x00110008
DDR_PI_1078	DDR_PI_OFS	436	0x00430025
DDR_PI_1079	DDR_PI_OFS	437	0x00080008
DDR_PI_1080	DDR_PI_OFS	438	0x00160010
DDR_PI_1081	DDR_PI_OFS	439	0x0032001E
DDR_PI_1082	DDR_PI_OFS	43A	0x001E0016
DDR_PI_1083	DDR_PI_OFS	43B	0x000E0032
DDR_PI_1084	DDR_PI_OFS	43C	0x00290012
DDR_PI_1085	DDR_PI_OFS	43D	0x00080008
DDR_PI_1086	DDR_PI_OFS	43E	0x00080008
DDR_PI_1087	DDR_PI_OFS	43F	0x00080008
DDR_PI_1088	DDR_PI_OFS	440	0x00080008
DDR_PI_1089	DDR_PI_OFS	441	0x00080008
DDR_PI_1090	DDR_PI_OFS	442	0x00080008
DDR_PI_1091	DDR_PI_OFS	443	0x00000000
DDR_PI_1092	DDR_PI_OFS	444	0x00000000
DDR_PI_1093	DDR_PI_OFS	445	0x00000000
DDR_PI_1094	DDR_PI_OFS	446	0x00000000
DDR_PI_1095	DDR_PI_OFS	447	0x00000000
DDR_PI_1096	DDR_PI_OFS	448	0x00000000
DDR_PI_1097	DDR_PI_OFS	449	0x00000000
DDR_PI_1098	DDR_PI_OFS	44A	0x00000000
DDR_PI_1099	DDR_PI_OFS	44B	0x00000000
DDR_PI_1100	DDR_PI_OFS	44C	0x00000000

Register Name	Address Offset (_OFS)	n [hex] (_OFS + n)	V4M
DDR_PI_1101	DDR_PI_OFS	44D	0x00000000
DDR_PI_1102	DDR_PI_OFS	44E	0x00000000
DDR_PI_1103	DDR_PI_OFS	44F	0x00000000
DDR_PI_1104	DDR_PI_OFS	450	0x00000000
DDR_PI_1105	DDR_PI_OFS	451	0x00000000
DDR_PI_1106	DDR_PI_OFS	452	0x00000000
DDR_PI_1107	DDR_PI_OFS	453	0x00000000
DDR_PI_1108	DDR_PI_OFS	454	0x00000000
DDR_PI_1109	DDR_PI_OFS	455	0x00000000
DDR_PI_1110	DDR_PI_OFS	456	0x00000000
DDR_PI_1111	DDR_PI_OFS	457	0x00000000
DDR_PI_1112	DDR_PI_OFS	458	0x00000000
DDR_PI_1113	DDR_PI_OFS	459	0x00000000
DDR_PI_1114	DDR_PI_OFS	45A	0x00000000
DDR_PI_1115	DDR_PI_OFS	45B	0x00000000
DDR_PI_1116	DDR_PI_OFS	45C	0x00000000
DDR_PI_1117	DDR_PI_OFS	45D	0x00000000
DDR_PI_1118	DDR_PI_OFS	45E	0x00000000
DDR_PI_1119	DDR_PI_OFS	45F	0x00000000
DDR_PI_1120	DDR_PI_OFS	460	0x00000000
DDR_PI_1121	DDR_PI_OFS	461	0x00000000
DDR_PI_1122	DDR_PI_OFS	462	0x00000000
DDR_PI_1123	DDR_PI_OFS	463	0x00000000
DDR_PI_1124	DDR_PI_OFS	464	0x00000000
DDR_PI_1125	DDR_PI_OFS	465	0x00000000
DDR_PI_1126	DDR_PI_OFS	466	0x00550000
DDR_PI_1127	DDR_PI_OFS	467	0x00000000
DDR_PI_1128	DDR_PI_OFS	468	0x00000000
DDR_PI_1129	DDR_PI_OFS	469	0x5A000000
DDR_PI_1130	DDR_PI_OFS	46A	0x003C0000
DDR_PI_1131	DDR_PI_OFS	46B	0x00000000
DDR_PI_1132	DDR_PI_OFS	46C	0x00000000
DDR_PI_1133	DDR_PI_OFS	46D	0x00000000
DDR_PI_1134	DDR_PI_OFS	46E	0x00000000
DDR_PI_1135	DDR_PI_OFS	46F	0x00000000
DDR_PI_1136	DDR_PI_OFS	470	0x00000000
DDR_PI_1137	DDR_PI_OFS	471	0x00000000
DDR_PI_1138	DDR_PI_OFS	472	0x00000000
DDR_PI_1139	DDR_PI_OFS	473	0x00000000
DDR_PI_1140	DDR_PI_OFS	474	0x00000000
DDR_PI_1141	DDR_PI_OFS	475	0x00000000
DDR_PI_1142	DDR_PI_OFS	476	0x00000000
DDR_PI_1143	DDR_PI_OFS	477	0x00000000
DDR_PI_1144	DDR_PI_OFS	478	0x00000000
DDR_PI_1145	DDR_PI_OFS	479	0x00000000

Register Name	Address Offset (_OFS)	n [hex] (_OFS + n)	V4M
DDR_PI_1146	DDR_PI_OFS	47A	0x00000000
DDR_PI_1147	DDR_PI_OFS	47B	0x00000000
DDR_PI_1148	DDR_PI_OFS	47C	0x00000000
DDR_PI_1149	DDR_PI_OFS	47D	0x00000000
DDR_PI_1150	DDR_PI_OFS	47E	0x00000000
DDR_PI_1151	DDR_PI_OFS	47F	0x00000000
DDR_PI_1152	DDR_PI_OFS	480	0x00000000
DDR_PI_1153	DDR_PI_OFS	481	0x00000000
DDR_PI_1154	DDR_PI_OFS	482	0x00000000
DDR_PI_1155	DDR_PI_OFS	483	0x00000000
DDR_PI_1156	DDR_PI_OFS	484	0x00000000
DDR_PI_1157	DDR_PI_OFS	485	0x00000000
DDR_PI_1158	DDR_PI_OFS	486	0x00000000
DDR_PI_1159	DDR_PI_OFS	487	0x00000000
DDR_PI_1160	DDR_PI_OFS	488	0x00000000
DDR_PI_1161	DDR_PI_OFS	489	0x00000000
DDR_PI_1162	DDR_PI_OFS	48A	0x00000000
DDR_PI_1163	DDR_PI_OFS	48B	0x00000000
DDR_PI_1164	DDR_PI_OFS	48C	0x00000000
DDR_PI_1165	DDR_PI_OFS	48D	0x00000000
DDR_PI_1166	DDR_PI_OFS	48E	0x00000000
DDR_PI_1167	DDR_PI_OFS	48F	0x00000000
DDR_PI_1168	DDR_PI_OFS	490	0x00000000
DDR_PI_1169	DDR_PI_OFS	491	0x00000000
DDR_PI_1170	DDR_PI_OFS	492	0x00000000
DDR_PI_1171	DDR_PI_OFS	493	0x00000000
DDR_PI_1172	DDR_PI_OFS	494	0x00000000
DDR_PI_1173	DDR_PI_OFS	495	0x00000000
DDR_PI_1174	DDR_PI_OFS	496	0x00000000
DDR_PI_1175	DDR_PI_OFS	497	0x00000000
DDR_PI_1176	DDR_PI_OFS	498	0x00000000
DDR_PI_1177	DDR_PI_OFS	499	0x00000000
DDR_PI_1178	DDR_PI_OFS	49A	0x00000000
DDR_PI_1179	DDR_PI_OFS	49B	0x00000000
DDR_PI_1180	DDR_PI_OFS	49C	0x00000000
DDR_PI_1181	DDR_PI_OFS	49D	0x00F10004
DDR_PI_1182	DDR_PI_OFS	49E	0x5D005D00
DDR_PI_1183	DDR_PI_OFS	49F	0x00000000
DDR_PI_1184	DDR_PI_OFS	4A0	0x00000000
DDR_PI_1185	DDR_PI_OFS	4A1	0x0000CD00
DDR_PI_1186	DDR_PI_OFS	4A2	0x00000000
DDR_PI_1187	DDR_PI_OFS	4A3	0x00004D00
DDR_PI_1188	DDR_PI_OFS	4A4	0x00000000
DDR_PI_1189	DDR_PI_OFS	4A5	0x00000000
DDR_PI_1190	DDR_PI_OFS	4A6	0x00000000

Register Name	Address Offset (_OFS)	n [hex] (_OFS + n)	V4M
DDR_PI_1191	DDR_PI_OFS	4A7	0x00F15224
DDR_PI_1192	DDR_PI_OFS	4A8	0x1C001944
DDR_PI_1193	DDR_PI_OFS	4A9	0x00000000
DDR_PI_1194	DDR_PI_OFS	4AA	0x00060000
DDR_PI_1195	DDR_PI_OFS	4AB	0x0000CD00
DDR_PI_1196	DDR_PI_OFS	4AC	0x00000000
DDR_PI_1197	DDR_PI_OFS	4AD	0x00004D00
DDR_PI_1198	DDR_PI_OFS	4AE	0x00000000
DDR_PI_1199	DDR_PI_OFS	4AF	0x00000000
DDR_PI_1200	DDR_PI_OFS	4B0	0x00000000
DDR_PI_1201	DDR_PI_OFS	4B1	0x00F13F74
DDR_PI_1202	DDR_PI_OFS	4B2	0x1C001944
DDR_PI_1203	DDR_PI_OFS	4B3	0x00000000
DDR_PI_1204	DDR_PI_OFS	4B4	0x00060000
DDR_PI_1205	DDR_PI_OFS	4B5	0x0000CD00
DDR_PI_1206	DDR_PI_OFS	4B6	0x00000000
DDR_PI_1207	DDR_PI_OFS	4B7	0x00004D00
DDR_PI_1208	DDR_PI_OFS	4B8	0x00000000
DDR_PI_1209	DDR_PI_OFS	4B9	0x00000000
DDR_PI_1210	DDR_PI_OFS	4BA	0x00000000
DDR_PI_1211	DDR_PI_OFS	4BB	0x00F10004
DDR_PI_1212	DDR_PI_OFS	4BC	0x5D005D00
DDR_PI_1213	DDR_PI_OFS	4BD	0x00000000
DDR_PI_1214	DDR_PI_OFS	4BE	0x00000000
DDR_PI_1215	DDR_PI_OFS	4BF	0x0000CD00
DDR_PI_1216	DDR_PI_OFS	4C0	0x00000000
DDR_PI_1217	DDR_PI_OFS	4C1	0x00004D00
DDR_PI_1218	DDR_PI_OFS	4C2	0x00000000
DDR_PI_1219	DDR_PI_OFS	4C3	0x00000000
DDR_PI_1220	DDR_PI_OFS	4C4	0x00000000
DDR_PI_1221	DDR_PI_OFS	4C5	0x00F15224
DDR_PI_1222	DDR_PI_OFS	4C6	0x1C001944
DDR_PI_1223	DDR_PI_OFS	4C7	0x00000000
DDR_PI_1224	DDR_PI_OFS	4C8	0x002E0000
DDR_PI_1225	DDR_PI_OFS	4C9	0x0000CD00
DDR_PI_1226	DDR_PI_OFS	4CA	0x00000000
DDR_PI_1227	DDR_PI_OFS	4CB	0x00004D00
DDR_PI_1228	DDR_PI_OFS	4CC	0x00000000
DDR_PI_1229	DDR_PI_OFS	4CD	0x00000000
DDR_PI_1230	DDR_PI_OFS	4CE	0x00000000
DDR_PI_1231	DDR_PI_OFS	4CF	0x00F13F74
DDR_PI_1232	DDR_PI_OFS	4D0	0x1C001944
DDR_PI_1233	DDR_PI_OFS	4D1	0x00000000
DDR_PI_1234	DDR_PI_OFS	4D2	0x002E0000
DDR_PI_1235	DDR_PI_OFS	4D3	0x0000CD00

Register Name	Address Offset (_OFS)	n [hex] (_OFS + n)	V4M
DDR_PI_1236	DDR_PI_OFS	4D4	0x00000000
DDR_PI_1237	DDR_PI_OFS	4D5	0x00004D00
DDR_PI_1238	DDR_PI_OFS	4D6	0x00000000
DDR_PI_1239	DDR_PI_OFS	4D7	0x00000000
DDR_PI_1240	DDR_PI_OFS	4D8	0x00000000
DDR_PI_1241	DDR_PI_OFS	4D9	0x20002000
DDR_PI_1242	DDR_PI_OFS	4DA	0x000A2000
DDR_PI_1243	DDR_PI_OFS	4DB	0x20002000
DDR_PI_1244	DDR_PI_OFS	4DC	0x20002000
DDR_PI_1245	DDR_PI_OFS	4DD	0x0010000F
DDR_PI_1246	DDR_PI_OFS	4DE	0x00120011
DDR_PI_1247	DDR_PI_OFS	4DF	0x00140013
DDR_PI_1248	DDR_PI_OFS	4E0	0x00172000
DDR_PI_1249	DDR_PI_OFS	4E1	0x20002000
DDR_PI_1250	DDR_PI_OFS	4E2	0x20002000
DDR_PI_1251	DDR_PI_OFS	4E3	0x00202000
DDR_PI_1252	DDR_PI_OFS	4E4	0x20002000
DDR_PI_1253	DDR_PI_OFS	4E5	0x20000028
DDR_PI_1254	DDR_PI_OFS	4E6	0x20002000
DDR_PI_1255	DDR_PI_OFS	4E7	0x20002000
DDR_PI_1256	DDR_PI_OFS	4E8	0x20002000
DDR_PI_1257	DDR_PI_OFS	4E9	0x20002000
DDR_PI_1258	DDR_PI_OFS	4EA	0x20002000
DDR_PI_1259	DDR_PI_OFS	4EB	0x20002000
DDR_PI_1260	DDR_PI_OFS	4EC	0x20002000
DDR_PI_1261	DDR_PI_OFS	4ED	0x20002000
DDR_PI_1262	DDR_PI_OFS	4EE	0x20002000
DDR_PI_1263	DDR_PI_OFS	4EF	0x20002000
DDR_PI_1264	DDR_PI_OFS	4F0	0x20002000
DDR_PI_1265	DDR_PI_OFS	4F1	0x20002000
DDR_PI_1266	DDR_PI_OFS	4F2	0x20002000
DDR_PI_1267	DDR_PI_OFS	4F3	0x20002000
DDR_PI_1268	DDR_PI_OFS	4F4	0x20002000
DDR_PI_1269	DDR_PI_OFS	4F5	0x20002000
DDR_PI_1270	DDR_PI_OFS	4F6	0x20002000
DDR_PI_1271	DDR_PI_OFS	4F7	0x20002000
DDR_PI_1272	DDR_PI_OFS	4F8	0x20002000
DDR_PI_1273	DDR_PI_OFS	4F9	0x20002000
DDR_PI_1274	DDR_PI_OFS	4FA	0x20002000
DDR_PI_1275	DDR_PI_OFS	4FB	0x20002000
DDR_PI_1276	DDR_PI_OFS	4FC	0x20002000
DDR_PI_1277	DDR_PI_OFS	4FD	0x20002000
DDR_PI_1278	DDR_PI_OFS	4FE	0x20002000
DDR_PI_1279	DDR_PI_OFS	4FF	0x20002000
DDR_PI_1280	DDR_PI_OFS	500	0x20002000

Register Name	Address Offset (_OFS)	n [hex] (_OFS + n)	V4M
DDR_PI_1281	DDR_PI_OFS	501	0x00020001
DDR_PI_1282	DDR_PI_OFS	502	0x20000003
DDR_PI_1283	DDR_PI_OFS	503	0x000C000B
DDR_PI_1284	DDR_PI_OFS	504	0x000E000D
DDR_PI_1285	DDR_PI_OFS	505	0x20002000
DDR_PI_1286	DDR_PI_OFS	506	0x20002000
DDR_PI_1287	DDR_PI_OFS	507	0x20002000
DDR_PI_1288	DDR_PI_OFS	508	0x20000016
DDR_PI_1289	DDR_PI_OFS	509	0x100C2000
DDR_PI_1290	DDR_PI_OFS	50A	0x00080000
DDR_PI_1291	DDR_PI_OFS	50B	0x20002000
DDR_PI_1292	DDR_PI_OFS	50C	0x20002000
DDR_PI_1293	DDR_PI_OFS	50D	0x100E2000
DDR_PI_1294	DDR_PI_OFS	50E	0x2000001F
DDR_PI_1295	DDR_PI_OFS	50F	0x20002000
DDR_PI_1296	DDR_PI_OFS	510	0x20002000
DDR_PI_1297	DDR_PI_OFS	511	0x20002000
DDR_PI_1298	DDR_PI_OFS	512	0x20002000
DDR_PI_1299	DDR_PI_OFS	513	0x20002000
DDR_PI_1300	DDR_PI_OFS	514	0x20002000

5.3 List of other Registers

Table 5-5 lists Product register. Table 5-6 lists CPG registers. Table 5-7 lists Mode Monitor registers. Table 5-8 lists OTP Monitor register.

Table 5-5 Product Register

Register Name	Abbreviation	R/W	Value after Reset	Address	Bit Name	Bit
Product Register	PRR	R	—	0xFFF0 0044	—	[31:0]

Table 5-6 CPG Register

Register Name	Abbreviation	R/W	Value after Reset	Address	Bit Name	Bit
CPG Write Protect Register	CPG_CPGWPR	R/W	0x0000 0000	0xE615 0000	WPRTCT	[31:0]
Frequency Control Register D	CPG_FRQCRD	R/W	0x0000 0000	0xE615 080C	KICK	[31]
					ZB3FC	[3:0]
PLL Enable Control Register	CPG_PLLECR	R/W	0x0000 EBEB	0xE615 0820	PLL7ST	[24]
					PLL7E	[16]
					PLL6ST	[15]
					PLL5ST	[14]
					PLL4ST	[13]
					PLL3ST	[11]
					PLL2ST	[9]
					PLL1ST	[8]
					PLL6E	[7]
					PLL5E	[6]
					PLL4E	[5]
					PLL3E	[3]
					PLL2E	[1]
					PLL1E	[0]
PLL3 Control Register 0	CPG_PLL3CR0	R/W	0x0--- 0000	0xE615 083C	KICK	[31]
					NI	[27:20]
					SSMODE	[18:16]
PLL3 Control Register 1	CPG_PLL3CR1	R/W	0x0000 0000	0xE615 08C0	NF	[24:0]
Software Reset Register 4	CPG_SRCR4	R/W	0x0000 0000	0xE615 2C10	DSITXLINK0	[15]
					DOC2CH	[14]
					DIS0	[11]
					DDR1:DDR0	[9]
					CSITOP1	[0]

Register Name	Abbreviation	R/W	Value after Reset	Address	Bit Name	Bit
Software Reset Clearing Register 4	CPG_SRSTCLR4	W	0x0000 0000	0xE615 2C90	DSITXLINK0	[15]
					DOC2CH	[14]
					DIS0	[11]
					DDR1:DDR0	[9]
					CSITOP1	[0]
Functional Safety Reset Check Register 4	CPG_FSRCHKRA4	R	—	0xE615 0410	RCHKm	[31:0]
Functional Safety Reset Check Clear Register 4	CPG_FSRCHKCLRR4	W	0x0000 0000	0xE615 0590	RCLRm	[31:0]
Functional Safety Reset Check Set Register 4	CPG_FSRCHKSETR4	W	0x0000 0000	0xE615 0510	RSETm	[31:0]

Table 5-7 Mode Monitor Register

Register Name	Abbreviation	R/W	Value after Reset	Address	Bit Name	Bit
Mode Monitor Register 0	RST_MODEMR0	R	—	0xE616 0000	—	
Mode Monitor Register 1	RST_MODEMR1	R	—	0xE616 0004	—	

Table 5-8 OTP Monitor Register

Register Name	Abbreviation	R/W	Value after Reset	Address	Bit Name	Bit
OTP_MEM Monitor Register 17	OTPMONITOR17	R	—	0xE61B F144	ID_Reg	[7:0]

Appendix

A1. Concrete Examples of Configuration Values

A1.1 Configuration Values

In this appendix, hardware configuration values set to DBSC and PHY are explained. For DBSC settings, see section 1.2.1, section 4.4.1. For PHY settings, see section 4.2.2. The Reference [4] is helpful to set these parameters.

Table A1-1 Configuration Values

These values are concrete examples of R-Car V4M RENESAS LPDDR4X board.

configuration parameter	description	Table/Figure	Value (ex: RENESAS Gray Hawk board (DRAM: 64Gbit 2rank))
bdcfg_phyvalid	Active memory channels ch0: 'b00000001 ch1: 'b00000010 ch2: 'b00000100 ch3: 'b00001000 ch4: 'b00010000 ch5: 'b00100000 ch6: 'b01000000 ch7: 'b10000000	—	0x03: ch0, ch1 are valid.
bdcfg_vref_r	Read DQ Vref Training Range	Table 4-17	0x00000000
bdcfg_vref_w	Write DQ Vref Training Range	Table 4-18	0x0000
bdcfg_vref_ca	CA Vref Training Range	Table 4-19	0x0000

configuration parameter	description	Table/Figure	Value (ex: RENESAS Gray Hawk board (DRAM: 64Gbit 2rank))
bdcfg_ddr_density	Memory density (number of CS signals, i.e. ranks) is identified by bdcfg_ddr_density, which is defined per channel and per CS signal. bdcfg_ddr_density Memory density ---------- 0x00 4Gbit/die (2Gbit/channel) or 2Gbit/die (2Gbit/channel) 0x01 6Gbit/die (3Gbit/channel) or 3Gbit/die (3Gbit/channel) 0x02 8Gbit/die (4Gbit/channel) or 4Gbit/die (4Gbit/channel) 0x03 12Gbit/die (6Gbit/channel) or 6Gbit/die (6Gbit/channel) 0x04 16Gbit/die (8Gbit/channel) or 8Gbit/die (8Gbit/channel) 0x05 24Gbit/die (12Gbit/channel) or 12Gbit/die (12Gbit/channel) 0x06 32Gbit/die (16Gbit/channel) or 16Gbit/die (16Gbit/channel) 0xFF No Memory	Table 4-5, Figure 4-2	Memory setting example: cs0: 0x06 cs1: 0x06

configuration parameter	description	Table/Figure	Value (ex: RENESAS Gray Hawk board (DRAM: 64Gbit 2rank))
bdcfg_ca_swap	bdcfg_ca_swap is the swap setting for CA, which is defined per channel. This value indicates the destination for connection from the SoC pins to those of the LPDDR4X memory. The relation between the SoC pins and the bit fields of bdcfg_ca_swap is as follows. bdcfg_ca_swap is 28-bit. CA signal connection SoC pin bdcfg_ca_swap[] Point to Point --- CA0 bdcfg_ca_swap[3:0] used CA1 bdcfg_ca_swap[7:4] used CA2 bdcfg_ca_swap[11:8] used CA3 bdcfg_ca_swap[15:12] used CA4 bdcfg_ca_swap[19:16] used CA5 bdcfg_ca_swap[23:20] used CA6 bdcfg_ca_swap[27:24] used T-branch connection is not supported.	Table 4-38, Table 4-40	If bdcfg_ca_swap=0x6302451, the connections between SoC and LPDDR4X memory are as follows. SoC LPDDR4X DRAM --- CA0 ---- CA1A, CA1B CA1 ---- CA5A, CA5B CA2 ---- CA4A, CA4B CA3 ---- CA2A, CA2B CA4 ---- CA0A, CA0B CA5 ---- CA3A, CA3B CA6 ---- CA6A, CA6B
bdcfg_dqs_swap	bdcfg_dqs_swap is the swap setting for DQS, which is defined per channel. bdcfg_dqs_swap values indicate the destinations for connection from SoC pins to those of the LPDDR4X memory. The following is the relation between SoC byte-lanes and bit fields of bdcfg_dqs_swap. SoC bdcfg_dqs_swap[] --- byte-lane0:DQS0,DM0,DQ[7:0] bdcfg_dqs_swap[3:0] byte-lane1:DQS1,DM1,DQ[15:8] bdcfg_dqs_swap[7:4]	Table 4-45	If bdcfg_dqs_swap = 0x10, the connections between SoC and LPDDR4X memory are as follows. SoC LPDDR4X DRAM --- byte-lane0: DQS0,DM0,DQ[15:8] ------ DQS0_A,DM0_A,DQ_A[15:8] byte-lane1: DQS1,DM1,DQ[7:0] -------- DQS1_A,DM1_A,DQ_A[7:0]

configuration parameter	description	Table/Figure	Value (ex: RENESAS Gray Hawk board (DRAM: 64Gbit 2rank))	
bdcfg_dq_swap	bdcfg_dq_swap is the swap setting for DQ, which is defined per channel and per slice. bdcfg_dq_swap values indicate the destinations for connection from SoC pins to those of the LPDDR4X memory. The following is the relation between DQ of the SoC and bit fields of bdcfg_dq_swap. This field are defined by the byte-lane signal sequence (bdcfg_dqs_swap). SoC bdcfg_dq_swap[] ---------- DQ0 bdcfg_dq_swap[3:0] DQ1 bdcfg_dq_swap[7:4] DQ2 bdcfg_dq_swap[11:8] DQ3 bdcfg_dq_swap[15:12] DQ4 bdcfg_dq_swap[19:16] DQ5 bdcfg_dq_swap[23:20] DQ6 bdcfg_dq_swap[27:24] DQ7 bdcfg_dq_swap[31:28]	Table 4-34	If bdcfg_dq_swap = 0x21380465 for slice 0, the connections between SoC and LPDDR4X memory are as follows. Byte-lane0 SoC LPDDR4X DRAM ---------- DQ0---DQ_A[5] DQ1---DQ_A[6] DQ2---DQ_A[4] DQ3---DQ_A[0] DQ4---DQ_A[8] DQ5---DQ_A[3] DQ6---DQ_A[1] DQ7---DQ_A[2]	If bdcfg_dq_swap = 0x12638045 for slice 1, the connections between SoC and LPDDR4X memory are as follows. Byte-lane1 SoC LPDDR4X DRAM ---------- DQ8----DQ_A[13] DQ9----DQ_A[12] DQ10--DQ_A[8] DQ11--DQ_A[16] DQ12--DQ_A[11] DQ13--DQ_A[14] DQ14--DQ_A[10] DQ15--DQ_A[9]
bdcfg_dm_swap	bdcfg_dm_swap is the swap setting for DM, which is defined per channel and per slice.	Table 4-34	0x07	0x07
bdcfg_cs_swap	bdcfg_cs_swap is the swap setting for CS, which is defined per channel.	Table 4-41	0x10	
bdcfg_cke_swap	bdcfg_cke_swap is the swap setting for CKE, which is defined per channel.	Table 4-42	0x10	

A2. Initial PLL3 Setting

In this appendix, Initial PLL3 Setting is explained. Figure A2-1 shows the flow of Initial PLL3 Setting. For details of PLL3 Setting, see Appendix A3.

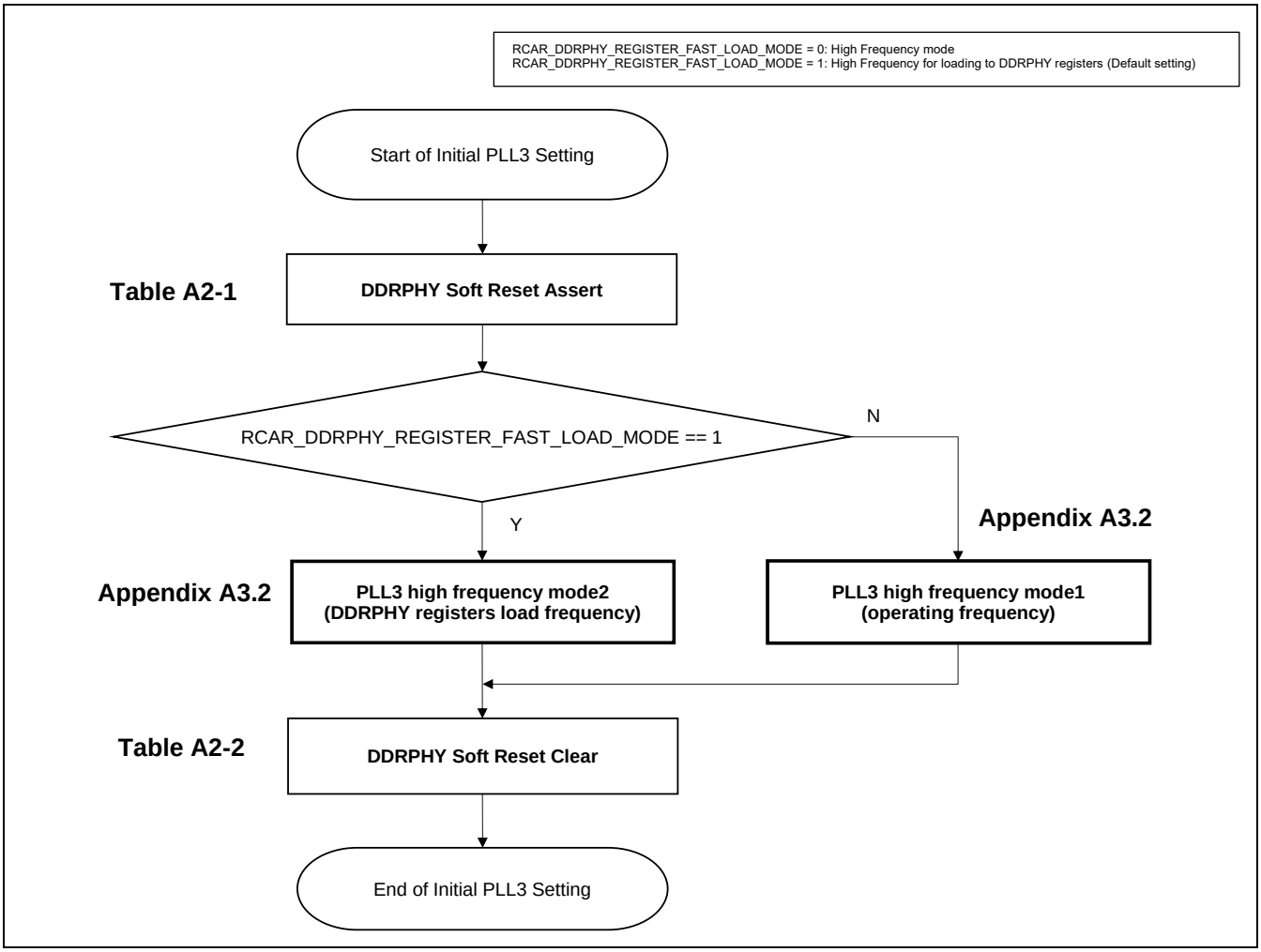

Figure A2-1 Flow of Initial PLL3 Setting

Table A2-1 DDRPHY Soft Reset Assert

Op.	Register Name	Bit	Bit Name	Data	Description
W	CPG_CPGWPR	—	—	~(0x00000200)	
W	CPG_FSRCHKCLRR4	—	—	0x00000200	
W	CPG_CPGWPR	—	—	~(0x00000200)	
W	CPG_FSRCHKSETR	—	—	0x00000200	
R	CPG_SRCR4	—	—	dataL	
W	CPG_CPGWPR	—	—	~(dataL | 0x00000200)	
W	CPG_SRCR4	—	—	dataL | 0x00000200	
R	CPG_FSRCHKRA4	—	—	dataL	
W	CPG_CPGWPR	—	—	~(0x00000200)	
W	CPG_FSRCHKCLRR4	—	—	0x00000200	

Table A2-2 DDRPHY Soft Reset Clear

Op.	Register Name	Bit	Bit Name	Data	Description
W	CPG_CPGWPR	—	—	~(0x00000200)	
W	CPG_SRSTCLR4	—	—	0x00000200	
R	CPG_SRCR4	—	—	dataL	

A3. Setting PLL3

In this appendix, the setting of PLL3 is explained. There are four sets of PLL3 settings for four frequencies.

- PLL3 low frequency mode (boot frequency)
- PLL3 medium frequency mode (operating frequency)
- PLL3 high frequency mode1 (operating frequency)
- PLL3 high frequency mode2 (DDRPHY registers load frequency)

This block also contains the settings for PLL3 multiplication mode. At high frequency and medium frequency, the fractional multiplication mode should be used, and the integer multiplication mode can only be used for debugging purpose. At low frequency, the integer multiplication mode should be used.

The calculated value in Appendix A3.1 is used in the Table A3-1, Table A3-2, Table A3-3, Table A3-4, Table A3-5, Table A3-6, and Table A3-7.

For each set of frequency settings, parameters (divisors and multipliers) in the Table A3-1, Table A3-2, Table A3-3, Table A3-4, Table A3-5, Table A3-6, and Table A3-7 are used to set the registers Appendix A3.2.

Table A3-1 Setting the Divisors and Multipliers for PLL3 low frequency mode (Integer mode)

ddr_mul_low: Multiplier for PLL3 low frequency mode
dataDIV: Divisor for PLL3
dataMUL: Multiplier for PLL3 (Integer)
dataNF: Multiplier for PLL3 (Fractional)
ssmode: PLL3 mode and output frequency dither mode

Variable	Formula
ddr_mul_low	(3200 * brd_clkdiv * (brd_clkdiva + 1)) / (brd_clk)
dataDIV	0x0C
ssmode	0x0
dataNF	0x00
dataMUL	(((ddr_mul_low / 2) – 1) << 20) | (ssmode << 16)

Table A3-2 Setting the Divisors and Multipliers for PLL3 medium frequency mode (Fractional mode)

ddr_mul: Multiplier for PLL3 medium frequency mode
dataDIV: Divisor for PLL3
dataMUL: Multiplier for PLL3 (Integer)
dataNF: Multiplier for PLL3 (Fractional)
ssmode: PLL3 mode and output frequency dither mode

Variable	Formula
ddr_mul	(ddr_mbps * brd_clkdiv * (brd_clkdiva + 1)) / (brd_clk * ddr_mbpsdiv)
dataDIV	ddr_medium_div
ssmode	0x4
dataNF	((8 * ddr_mbps * brd_clkdiv * (brd_clkdiva + 1)) / (ddr_mbpsdiv * brd_clk)) – (8 * (ddr_mul / 2) * 2)
dataMUL	(((ddr_mul / 2) – 1) << 20) | (ssmode << 16)

Table A3-3 Setting the Divisors and Multipliers for PLL3 medium frequency mode (Integer mode)

ddr_mul: Multiplier for PLL3 medium frequency mode
dataDIV: Divisor for PLL3
dataMUL: Multiplier for PLL3 (Integer)
dataNF: Multiplier for PLL3 (Fractional)
ssmode: PLL3 mode and output frequency dither mode

Variable	Formula
ddr_mul	(ddr_mbps * brd_clkdiv * (brd_clkdiva + 1)) / (brd_clk * ddr_mbpsdiv)
dataDIV	ddr_medium_div
ssmode	0x0
dataNF	0x00
dataMUL	(((ddr_mul / 2) – 1) << 20) | (ssmode << 16)

Table A3-4 Setting the Divisors and Multipliers for PLL3 high frequency mode1 (Fractional mode)

ddr_mul: Multiplier for PLL3 high frequency mode1
dataDIV: Divisor for PLL3
dataMUL: Multiplier for PLL3 (Integer)
dataNF: Multiplier for PLL3 (Fractional)
ssmode: PLL3 mode and output frequency dither mode

Variable	Formula
ddr_mul	(ddr_mbps * brd_clkdiv * (brd_clkdiva + 1)) / (brd_clk * ddr_mbpsdiv)
dataDIV	0x0
ssmode	0x4
dataNF	((8 * ddr_mbps * brd_clkdiv * (brd_clkdiva + 1U)) / (ddr_mbpsdiv * brd_clk)) – (8 * (ddr_mul / 2) * 2)
dataMUL	(((ddr_mul / 2) – 1) << 20) | (ssmode << 16)

Table A3-5 Setting the Divisors and Multipliers for PLL3 high frequency mode1 (Integer mode)

ddr_mul: Multiplier for PLL3 high frequency mode1
dataDIV: Divisor for PLL3
dataMUL: Multiplier for PLL3 (Integer)
dataNF: Multiplier for PLL3 (Fractional)
ssmode: PLL3 mode and output frequency dither mode

Variable	Formula
ddr_mul	(ddr_mbps * brd_clkdiv * (brd_clkdiva + 1)) / (brd_clk * ddr_mbpsdiv)
dataDIV	0x0
ssmode	0x0
dataNF	0x00
dataMUL	(((ddr_mul / 2) – 1) << 20) | (ssmode << 16)

Table A3-6 Setting the Divisors and Multipliers for PLL3 high frequency mode2 (Fractional mode)

ddr_mul_reg: Multiplier for PLL3 high frequency mode2
dataDIV: Divisor for PLL3
dataMUL: Multiplier for PLL3 (Integer)
dataNF: Multiplier for PLL3 (Fractional)
ssmode: PLL3 mode and output frequency dither mode

Variable	Formula
ddr_mul_reg	(12800 * brd_clkdiv * (brd_clkdiva + 1)) / (brd_clk * 3)
dataDIV	0x0
ssmode	0x4
dataNF	0x00
dataMUL	(((ddr_mul_reg / 2) – 1) << 20) | (ssmode << 16)

Table A3-7 Setting the Divisors and Multipliers for PLL3 high frequency mode2 (Integer mode)

ddr_mul_reg: Multiplier for PLL3 high frequency mode2
dataDIV: Divisor for PLL3
dataMUL: Multiplier for PLL3 (Integer)
dataNF: Multiplier for PLL3 (Fractional)
ssmode: PLL3 mode and output frequency dither mode

Variable	Formula
ddr_mul_reg	(12800 * brd_clkdiv * (brd_clkdiva + 1)) / (brd_clk * 3)
dataDIV	0x0
ssmode	0x0
dataNF	0x00
dataMUL	(((ddr_mul_reg / 2) – 1) << 20) | (ssmode << 16)

A3.1 Calculate the value to be set for PLL3

In this appendix, Calculate the value to be set for PLL3.

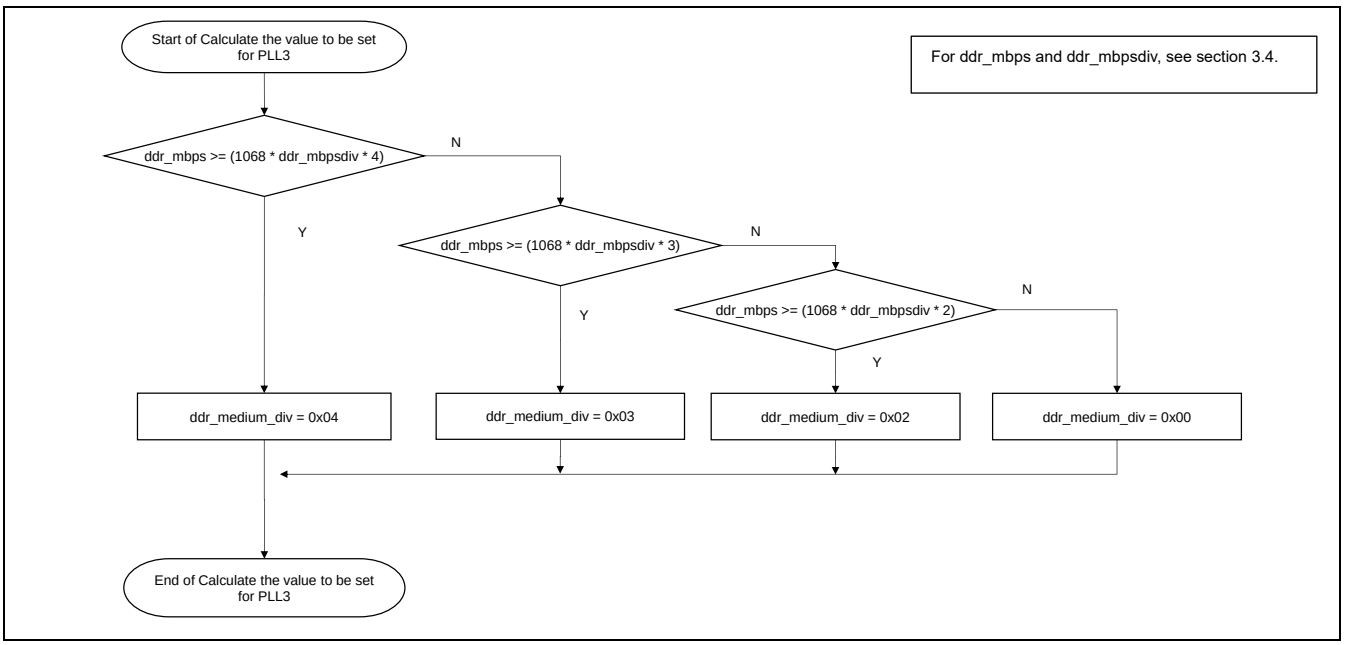

Figure A3-1 Flow of Calculate the value to be set for PLL3

A3.2 PLL3 Setting

In this appendix, the setting of PLL3 is explained. For each set of frequency settings, parameters (divisors and multipliers) in the Table A3-1, Table A3-2, Table A3-3, Table A3-4, Table A3-5, Table A3-6, and Table A3-7 are set in registers as listed in Table A3-9 and Table A3-13. Figure A3-2 is a flowchart of PLL3 setting.

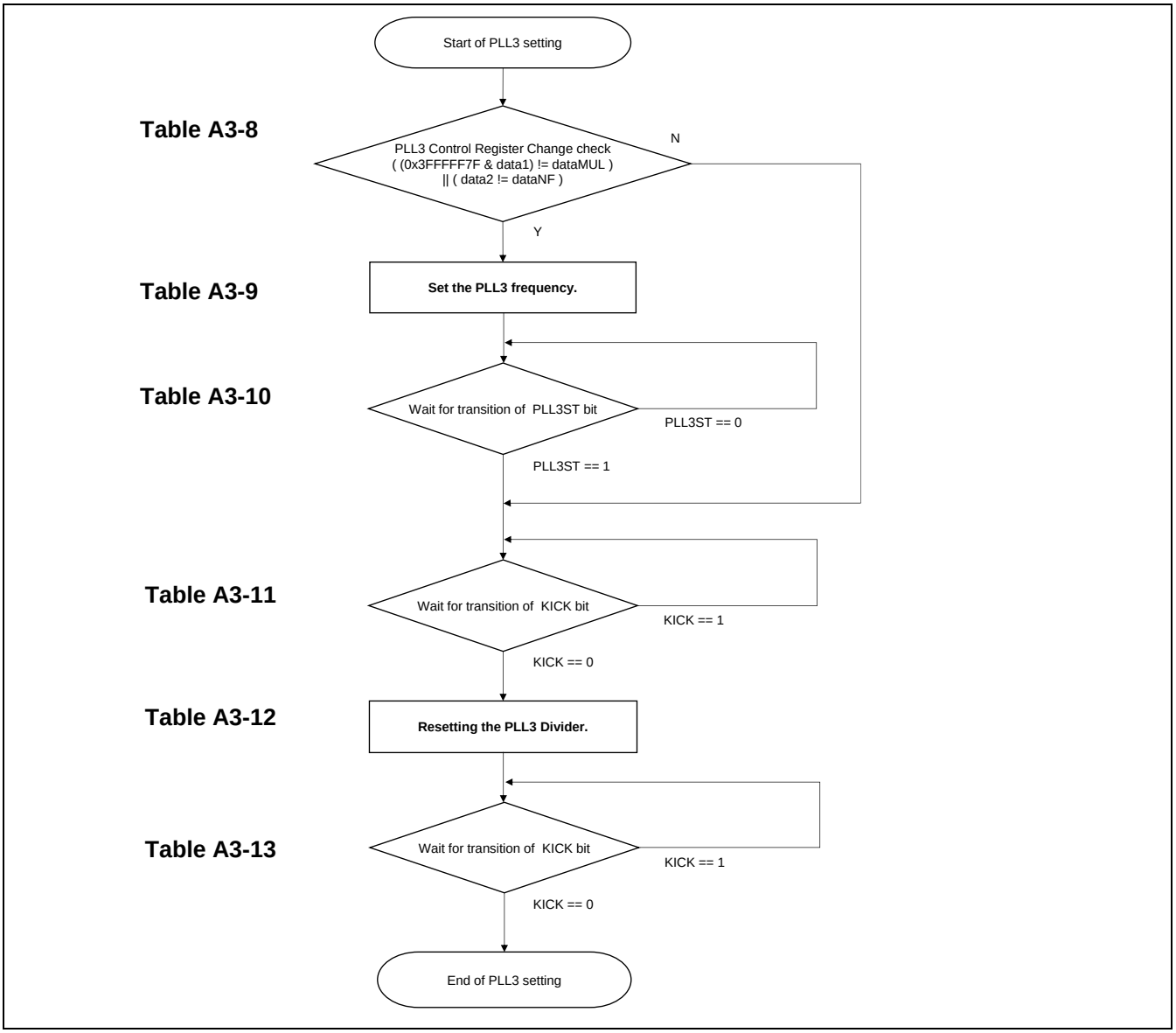

Figure A3-2 Flow of PLL3 Setting

Table A3-8 PLL3 Control Register Change check

Op.	Register Name	Bit	Bit Name	Data	Description
R	CPG_PLL3CR0	—	—	data1	
R	CPG_PLL3CR1	—	—	data2	

Table A3-9 Setting the PLL3 Frequency

Op.	Register Name	Bit	Bit Name	Data	Description
W	CPG_CPGWPR	—	—	~(dataMUL)	
W	CPG_PLL3CR0	—	—	dataMUL	
W	CPG_CPGWPR	—	—	~(dataNF)	
W	CPG_PLL3CR1	—	—	dataNF	
R	CPG_PLL3CR0	—	—	dataL	
W	CPG_CPGWPR	—	—	~(dataL | 0x80000000)	
W	CPG_PLL3CR0	—	—	dataL | 0x80000000	

Table A3-10 Get the PLL Enable Control

Op.	Register Name	Bit	Bit Name	Data	Description
R	CPG_PLLECR	—	—	dataL	

Table A3-11 Get the PLL Enable Control

Op.	Register Name	Bit	Bit Name	Data	Description
R	CPG_FRQCRD0	—	—	dataL	Wait for the PLL3 frequency setting to complete.

Table A3-12 Resetting the PLL3 Divider

Op.	Register Name	Bit	Bit Name	Data	Description
R	CPG_FRQCRD0	—	—	dataL	Divider setting for PLL3
W	CPG_CPGWPR	—	—	~(dataDIV | (0xFFFFFFF0 & dataL))	
W	CPG_FRQCRD0	—	—	dataDIV | (0xFFFFFFF0 & dataL)	
R	CPG_FRQCRD0	—	—	dataL	
W	CPG_CPGWPR	—	—	~(dataL | 0x80000000)	
W	CPG_FRQCRD0	—	—	dataL | 0x80000000	

Table A3-13 Get the PLL Enable Control

Op.	Register Name	Bit	Bit Name	Data	Description
R	CPG_FRQCRD0	—	—	dataL	Wait for the PLL3 frequency setting to complete.

A4. Periodic Training Separate Mode Setting

In this appendix, the "Periodic training separate mode" is described. If you want to enable this mode, the following flow must be performed after QoS settings. For details of this settings, see QoS documentation. Figure A4-1 shows the flow of Periodic Training Separate Mode Setting.

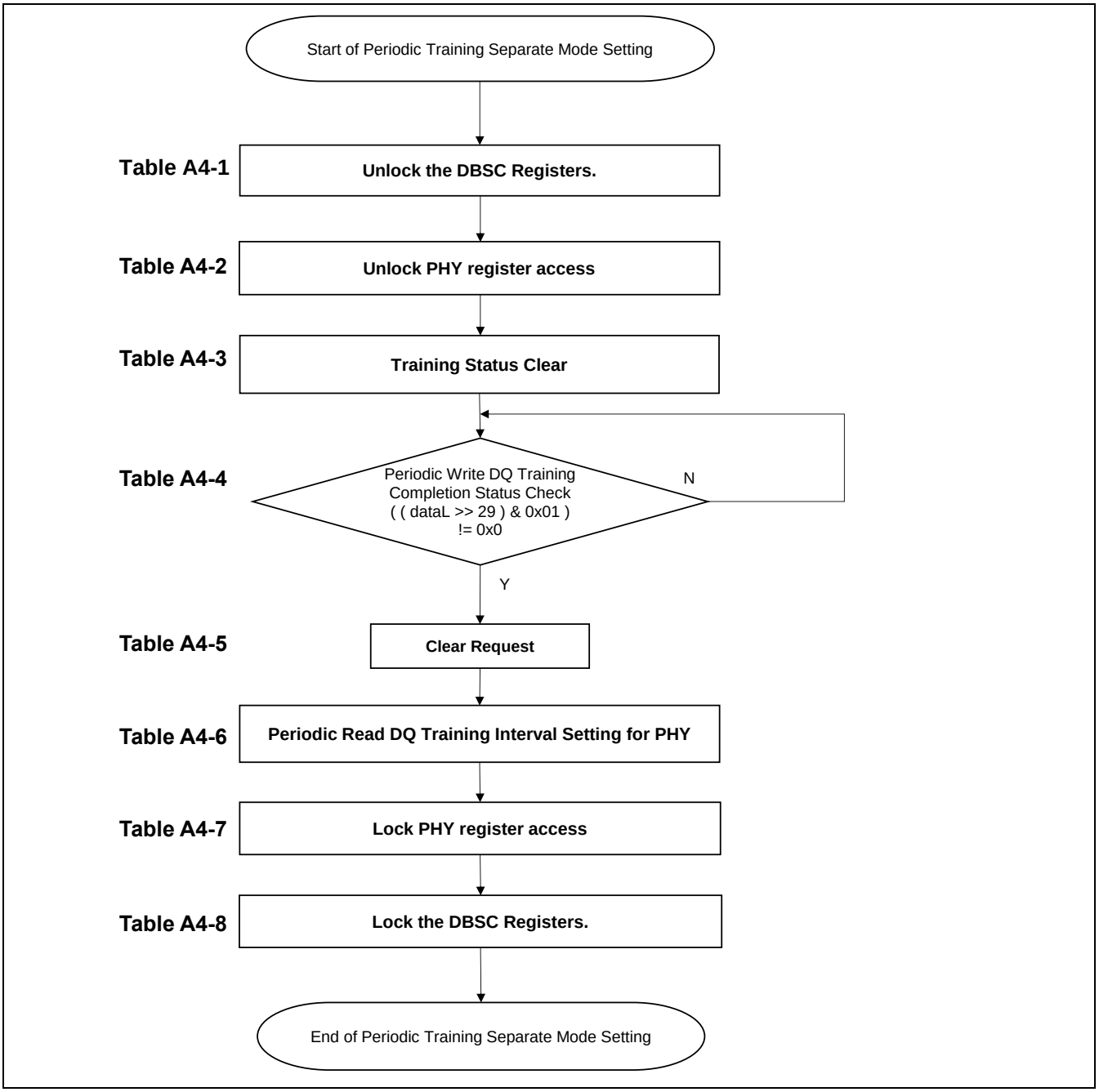

Figure A4-1 Flow of Periodic Training Separate Mode Setting

Table A4-1 Unlocking the DBSC Register

Op.	Register Name	Bit	Bit Name	Data	Description
W	DBSC_DBSYSCNT0	[15:0]	REGLOCK	0x00001234	Unlocks the DBSC registers against access. See Reference [3].
W	DBSC_DBSYSCNT0A	[15:0]	REGLOCK	0x00001234	Unlocks the DBSC registers against access. See Reference [3].

Table A4-2 Unlocking Access to the PHY Registers

Op.	Register Name	Bit	Bit Name	Data	Description
W	DBSC_DBPDLK{m_1}	[31:0]	PLOCK{m_1}	0x0000A55A	Unlock access to the PHY registers.

Table A4-3 Training Status Clear

Op.	Bit Name	Data	Description
W	PI_INT_ACK_0	0xFFFFFFFF	
W	PI_INT_ACK_1	0x01	

Table A4-4 Get PI_INT_STATUS

Op.	Bit Name	Data	Description
R	PI_INT_STATUS	dataL	

Table A4-5 Clear Request

Op.	Bit Name	Data	Description
W	PI_INT_ACK_0	0x1 << 0x29	

Table A4-6 Periodic Read DQ Training Interval Setting for PHY

Op.	Bit Name	Data	Description
R	PI_LONG_COUNT_MASK	count	
W	PI_RDLVL_INTERVAL	((PERIODIC_TRAINING_INTERVAL – 3000) * (ddr_mbps / ddr_mbpsdiv / 8) / (1024 – count * 32))	PERIODIC_TRAINING_INTERVAL = 20000 For details of this settings, see QoS documentation. The following parameters are explained in section 3.4: ddr_mbpsdiv, ddr_mbps.

Table A4-7 Locking the PHY Registers

Op.	Register Name	Bit	Bit Name	Data	Description
W	DBSC_DBPDLK{m_1}	[31:0]	PLOCK{m_1}	0x00000000	Locks the PHY registers against access.

Table A4-8 Locking the DBSC Register

Op.	Register Name	Bit	Bit Name	Data	Description
W	DBSC_DBSYSCNT0	[15:0]	REGLOCK	0x00000000	Locks the DBSC registers against access. See Reference [3].
W	DBSC_DBSYSCNT0A	[15:0]	REGLOCK	0x00000000	Locks the DBSC registers against access. See Reference [3].

References

1. JEDEC STANDARD LPDDR4 [JESD209-4C]. *JEDEC*
2. JEDEC STANDARD Addendum No.1 to JESD209-4 [JESD209-4-1A]. *JEDEC*
3. R-Car V4M Series User's Manual: Hardware [Rev.0.80]. *RENESAS*
4. R-Car V4M Modifying the LPDDR4X SDRAM Initialize Code [Rev.1.00]. *RENESAS*

Revision History

		Description	
Rev.	**Date**	**Page**	**Summary**
0.01	Nov. 2023	—	First edition issued.
0.10	Feb. 2024	—	Fixed incorrect / missing characters.
		—	Fixed the flowchart. A table number corresponding to processing has been added.
		9	The support code in Table 1-2 has been updated from 0.01 to 0.10.
		16	Correction of Figure 4-4.
		38	Correction of Table 4-9.
		40	Correction of Table 4-10.
		42	Correction of Table 4-11.
		—	Delete Table 4-13, Table 4-14 in Application Note Rev.0.01.
		46,48	Added Table 4-13, Table 4-14.
		52	Correction of Figure 4-5.
		—	Delete Table 4-27, Table 4-28, Table 4-29 in Application Note Rev.0.01.
		53,54, 55,56	Added Table 4-27, Table 4-28, Table 4-29, Table 4-30.
		81	Correction of Table 4-77. The following bits have been removed: PI_SEQ_ARRAY_65
		83	Correction of Table 4-84. Before: **Op.** **Bit Name** **Data** **Description** W PI_SEQ_ARRAY_29 0x11910048 W PI_SEQ_ARRAY_64 0x18061100 W PI_SEQ_ARRAY_65 0x19A10D06 W PI_FREQ_MAP 0x07 After: **Op.** **Bit Name** **Data** **Description** W PI_SEQ_ARRAY_29 0x11910048 W PI_SEQ_ARRAY_64 0x19A10D06 W PI_FREQ_MAP 0x07

Rev.	Date	Description Page	Summary
0.10	Feb. 2024	98	Correction of Table 5-3. Fixed the initial value of the PHY register. Before: V4M Bit Name / Address offset / n [hex] / Bit / Initial value [hex] PI_TSDO_F1 / DDR_PI_OFS / E5 / [31:24] / 0B PI_TDELAY_RDWR_2_BUS_IDLE_F1 / DDR_PI_OFS / E8 / [7:0] / 3A PI_WRLAT_F1 / DDR_PI_OFS / ED / [22:16] / 08 PI_WCK_ACTIVE_WR_F1 / DDR_PI_OFS / EF / [6:0] / 0D PI_WCK_ACTIVE_RD_F1 / DDR_PI_OFS / EF / [14:8] / 11 PI_CASLAT_F1 / DDR_PI_OFS / EF / [30:24] / 0C PI_TRFC_F1 / DDR_PI_OFS / F4 / [9:0] / 0CB PI_TREF_F1 / DDR_PI_OFS / F5 / [19:0] / 0081C PI_TDFI_WRLVL_WW_F1 / DDR_PI_OFS / FA / [17:8] / 019 PI_WRLVL_WCKOFF_F1 / DDR_PI_OFS / FA / [31:24] / 0B PI_RDLAT_ADJ_F1 / DDR_PI_OFS / 105 / [24:16] / 008 PI_WRLAT_ADJ_F1 / DDR_PI_OFS / 106 / [30:24] / 04 PI_TDFI_CALVL_CC_F1 / DDR_PI_OFS / 109 / [9:0] / 039 PI_TDFI_CALVL_CAPTURE_F1 / DDR_PI_OFS / 109 / [25:16] / 011 PI_TMRZ_F1 / DDR_PI_OFS / 10C / [20:16] / 01 After: V4M Bit Name / Address offset / n [hex] / Bit / Initial value [hex] PI_TSDO_F1 / DDR_PI_OFS / E5 / [31:24] / 10 PI_TDELAY_RDWR_2_BUS_IDLE_F1 / DDR_PI_OFS / E8 / [7:0] / 40 PI_WRLAT_F1 / DDR_PI_OFS / ED / [22:16] / 0C PI_WCK_ACTIVE_WR_F1 / DDR_PI_OFS / EF / [6:0] / 11 PI_WCK_ACTIVE_RD_F1 / DDR_PI_OFS / EF / [14:8] / 15 PI_CASLAT_F1 / DDR_PI_OFS / EF / [30:24] / 10 PI_TRFC_F1 / DDR_PI_OFS / F4 / [9:0] / 130 PI_TREF_F1 / DDR_PI_OFS / F5 / [19:0] / 00C2E PI_TDFI_WRLVL_WW_F1 / DDR_PI_OFS / FA / [17:8] / 01B PI_WRLVL_WCKOFF_F1 / DDR_PI_OFS / FA / [31:24] / 0F PI_RDLAT_ADJ_F1 / DDR_PI_OFS / 105 / [24:16] / 00A PI_WRLAT_ADJ_F1 / DDR_PI_OFS / 106 / [30:24] / 08 PI_TDFI_CALVL_CC_F1 / DDR_PI_OFS / 109 / [9:0] / 03B PI_TDFI_CALVL_CAPTURE_F1 / DDR_PI_OFS / 109 / [25:16] / 013 PI_TMRZ_F1 / DDR_PI_OFS / 10C / [20:16] / 02

Rev.	Date	Description Page	Summary
0.10	Feb. 2024	98	Correction of Table 5-3. Fixed the initial value of the PHY register. Before: V4M Bit Name / Address offset / n [hex] / Bit / Initial value [hex] PI_TCAENT_F1 / DDR_PI_OFS / 10D / [13:0] / 0086 PI_TVREF_SHORT_F1 / DDR_PI_OFS / 111 / [25:16] / 087 PI_TVREF_LONG_F1 / DDR_PI_OFS / 112 / [9:0] / 087 PI_TVRCG_ENABLE_F1 / DDR_PI_OFS / 112 / [25:16] / 06C PI_TVRCG_DISABLE_F1 / DDR_PI_OFS / 113 / [9:0] / 037 PI_TXP_F1 / DDR_PI_OFS / 119 / [20:16] / 07 PI_TMRWCKEL_F1 / DDR_PI_OFS / 119 / [31:24] / 0A PI_TCKEHDQS_F1 / DDR_PI_OFS / 121 / [21:16] / 14 PI_TFC_F1 / DDR_PI_OFS / 122 / [9:0] / 086 PI_TDFI_WDQLVL_WR_F1 / DDR_PI_OFS / 128 / [17:8] / 025 PI_TDFI_WDQLVL_RW_F1 / DDR_PI_OFS / 129 / [9:0] / 02B PI_WDQLVL_RDLAT_ADJ_F1 / DDR_PI_OFS / 12B / [8:0] / 006 PI_WDQLVL_WRLAT_ADJ_F1 / DDR_PI_OFS / 12B / [24:16] / 004 PI_TRP_F1 / DDR_PI_OFS / 137 / [7:0] / 0C PI_TRCD_F1 / DDR_PI_OFS / 137 / [15:8] / 0A After: V4M Bit Name / Address offset / n [hex] / Bit / Initial value [hex] PI_TCAENT_F1 / DDR_PI_OFS / 10D / [13:0] / 00C8 PI_TVREF_SHORT_F1 / DDR_PI_OFS / 111 / [25:16] / 0C9 PI_TVREF_LONG_F1 / DDR_PI_OFS / 112 / [9:0] / 0C9 PI_TVRCG_ENABLE_F1 / DDR_PI_OFS / 112 / [25:16] / 0A1 PI_TVRCG_DISABLE_F1 / DDR_PI_OFS / 113 / [9:0] / 051 PI_TXP_F1 / DDR_PI_OFS / 119 / [20:16] / 09 PI_TMRWCKEL_F1 / DDR_PI_OFS / 119 / [31:24] / 0D PI_TCKEHDQS_F1 / DDR_PI_OFS / 121 / [21:16] / 16 PI_TFC_F1 / DDR_PI_OFS / 122 / [9:0] / 0C8 PI_TDFI_WDQLVL_WR_F1 / DDR_PI_OFS / 128 / [17:8] / 029 PI_TDFI_WDQLVL_RW_F1 / DDR_PI_OFS / 129 / [9:0] / 02D PI_WDQLVL_RDLAT_ADJ_F1 / DDR_PI_OFS / 12B / [8:0] / 008 PI_WDQLVL_WRLAT_ADJ_F1 / DDR_PI_OFS / 12B / [24:16] / 008 PI_TRP_F1 / DDR_PI_OFS / 137 / [7:0] / 11 PI_TRCD_F1 / DDR_PI_OFS / 137 / [15:8] / 0F

Rev.	Date	Description Page	Summary
0.10	Feb. 2024	98	Correction of Table 5-3. Fixed the initial value of the PHY register. Before: V4M Bit Name / Address offset / n [hex] / Bit / Initial value [hex] PI_TWR_F1 / DDR_PI_OFS / 138 / [31:24] / 0B PI_TRAS_MAX_F1 / DDR_PI_OFS / 139 / [15:0] / 41D0 PI_TRAS_MIN_F1 / DDR_PI_OFS / 139 / [24:16] / 017 PI_TDQSCK_MAX_F1 / DDR_PI_OFS / 13A / [3:0] / 2 PI_TSR_F1 / DDR_PI_OFS / 13A / [23:16] / 08 PI_TMRD_F1 / DDR_PI_OFS / 13A / [31:24] / 0A PI_TDFI_CTRLUPD_MAX_F1 / DDR_PI_OFS / 142 / [20:0] / 001038 PI_TDFI_CTRLUPD_INTERVAL_F1 / DDR_PI_OFS / 143 / [31:0] / 0000A230 PI_TXSR_F1 / DDR_PI_OFS / 146 / [31:16] / 00CF PI_TINIT_F1 / DDR_PI_OFS / 14E / [23:0] / 01A0AB PI_TINIT5_F1 / DDR_PI_OFS / 152 / [23:0] / 00042B PI_TXSNR_F1 / DDR_PI_OFS / 153 / [15:0] / 00CF PI_TZQCAL_F1 / DDR_PI_OFS / 15C / [27:16] / 216 PI_TZQLAT_F1 / DDR_PI_OFS / 15D / [6:0] / 10 PI_ZQRESET_F1 / DDR_PI_OFS / 160 / [11:0] / 01B After: V4M Bit Name / Address offset / n [hex] / Bit / Initial value [hex] PI_TWR_F1 / DDR_PI_OFS / 138 / [31:24] / 10 PI_TRAS_MAX_F1 / DDR_PI_OFS / 139 / [15:0] / 62B8 PI_TRAS_MIN_F1 / DDR_PI_OFS / 139 / [24:16] / 022 PI_TDQSCK_MAX_F1 / DDR_PI_OFS / 13A / [3:0] / 3 PI_TSR_F1 / DDR_PI_OFS / 13A / [23:16] / 0C PI_TMRD_F1 / DDR_PI_OFS / 13A / [31:24] / 0C PI_TDFI_CTRLUPD_MAX_F1 / DDR_PI_OFS / 142 / [20:0] / 00185C PI_TDFI_CTRLUPD_INTERVAL_F1 / DDR_PI_OFS / 143 / [31:0] / 0000F398 PI_TXSR_F1 / DDR_PI_OFS / 146 / [31:16] / 0136 PI_TINIT_F1 / DDR_PI_OFS / 14E / [23:0] / 027100 PI_TINIT5_F1 / DDR_PI_OFS / 152 / [23:0] / 000640 PI_TXSNR_F1 / DDR_PI_OFS / 153 / [15:0] / 0136 PI_TZQCAL_F1 / DDR_PI_OFS / 15C / [27:16] / 320 PI_TZQLAT_F1 / DDR_PI_OFS / 15D / [6:0] / 18 PI_ZQRESET_F1 / DDR_PI_OFS / 160 / [11:0] / 028

Rev.	Date	Description Page	Summary
0.10	Feb. 2024	98	Correction of Table 5-3. Fixed the initial value of the PHY register. Before: V4M Bit Name / Address offset / n [hex] / Bit / Initial value [hex] PI_TWCK2DQ7H_F1 / DDR_PI_OFS / 163 / [12:8] / 05 PI_TDQ7HWCK_F1 / DDR_PI_OFS / 163 / [20:16] / 03 PI_TDQ7LWCK_F1 / DDR_PI_OFS / 163 / [28:24] / 06 PI_TDQ72DQ_F1 / DDR_PI_OFS / 164 / [9:0] / 086 PI_TCBTRTW_F1 / DDR_PI_OFS / 164 / [21:16] / 0B PI_MC_TRFC_F1 / DDR_PI_OFS / 168 / [25:16] / 0CD PI_SEQ_ARRAY_55 / DDR_PI_OFS / 1E3 / [28:0] / 18061140 PI_SEQ_ARRAY_56 / DDR_PI_OFS / 1E4 / [28:0] / 18861101 PI_SEQ_ARRAY_64 / DDR_PI_OFS / 1EC / [28:0] / 18061100 PI_SEQ_ARRAY_65 / DDR_PI_OFS / 1ED / [28:0] / 19A10D06 PI_SEQ_ARRAY_66 / DDR_PI_OFS / 1EE / [28:0] / 18051800 PI_SEQ_ARRAY_67 / DDR_PI_OFS / 1EF / [28:0] / 101B0001 PI_SEQ_ARRAY_68 / DDR_PI_OFS / 1F0 / [28:0] / 181B0100 PI_SEQ_ARRAY_69 / DDR_PI_OFS / 1F1 / [28:0] / 181B0200 PI_SEQ_ARRAY_70 / DDR_PI_OFS / 1F2 / [28:0] / 181B0300 After: V4M Bit Name / Address offset / n [hex] / Bit / Initial value [hex] PI_TWCK2DQ7H_F1 / DDR_PI_OFS / 163 / [12:8] / 06 PI_TDQ7HWCK_F1 / DDR_PI_OFS / 163 / [20:16] / 04 PI_TDQ7LWCK_F1 / DDR_PI_OFS / 163 / [28:24] / 07 PI_TDQ72DQ_F1 / DDR_PI_OFS / 164 / [9:0] / 0C8 PI_TCBTRTW_F1 / DDR_PI_OFS / 164 / [21:16] / 10 PI_MC_TRFC_F1 / DDR_PI_OFS / 168 / [25:16] / 132 PI_SEQ_ARRAY_55 / DDR_PI_OFS / 1E3 / [28:0] / 18861101 PI_SEQ_ARRAY_56 / DDR_PI_OFS / 1E4 / [28:0] / 181F0000 PI_SEQ_ARRAY_64 / DDR_PI_OFS / 1EC / [28:0] / 19A10D06 PI_SEQ_ARRAY_65 / DDR_PI_OFS / 1ED / [28:0] / 18051800 PI_SEQ_ARRAY_66 / DDR_PI_OFS / 1EE / [28:0] / 101B0001 PI_SEQ_ARRAY_67 / DDR_PI_OFS / 1EF / [28:0] / 181B0100 PI_SEQ_ARRAY_68 / DDR_PI_OFS / 1F0 / [28:0] / 181B0200 PI_SEQ_ARRAY_69 / DDR_PI_OFS / 1F1 / [28:0] / 181B0300 PI_SEQ_ARRAY_70 / DDR_PI_OFS / 1F2 / [28:0] / 181B0400

Rev.	Date	Description Page	Summary
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Before:

		V4M		
Bit Name	Address offset	n [hex]	Bit	Initial value [hex]
PI_WP_GAP_1_F1	DDR_PI_OFS	41B	[14:0]	001C
PI_WR_GAP_S_1_F1	DDR_PI_OFS	41E	[14:0]	001A
PI_WR_GAP_L_1_F1	DDR_PI_OFS	41F	[30:16]	001A
PI_RW_GAP_1_F1	DDR_PI_OFS	421	[14:0]	0011
PI_WP_GAP_2_F1	DDR_PI_OFS	428	[30:16]	001C
PI_WR_GAP_S_2_F1	DDR_PI_OFS	42B	[30:16]	001A
PI_WR_GAP_L_2_F1	DDR_PI_OFS	42D	[14:0]	001A
PI_RW_GAP_2_F1	DDR_PI_OFS	42E	[30:16]	0011
PI_WP_GAP_3_F1	DDR_PI_OFS	436	[14:0]	001C
PI_WR_GAP_S_3_F1	DDR_PI_OFS	439	[14:0]	001A
PI_WR_GAP_L_3_F1	DDR_PI_OFS	43A	[30:16]	001A
PI_RW_GAP_3_F1	DDR_PI_OFS	43C	[14:0]	0011
PI_DARRAY3_0_CS0_F1	DDR_PI_OFS	4A7	[7:0]	14
PI_DARRAY3_1_CS0_F1	DDR_PI_OFS	4A7	[15:8]	49
PI_DARRAY3_0_CS1_F1	DDR_PI_OFS	4C5	[7:0]	14
PI_DARRAY3_1_CS1_F1	DDR_PI_OFS	4C5	[15:8]	49

After:

		V4M		
Bit Name	Address offset	n [hex]	Bit	Initial value [hex]
PI_WP_GAP_1_F1	DDR_PI_OFS	41B	[14:0]	0025
PI_WR_GAP_S_1_F1	DDR_PI_OFS	41E	[14:0]	001E
PI_WR_GAP_L_1_F1	DDR_PI_OFS	41F	[30:16]	001E
PI_RW_GAP_1_F1	DDR_PI_OFS	421	[14:0]	0012
PI_WP_GAP_2_F1	DDR_PI_OFS	428	[30:16]	0025
PI_WR_GAP_S_2_F1	DDR_PI_OFS	42B	[30:16]	001E
PI_WR_GAP_L_2_F1	DDR_PI_OFS	42D	[14:0]	001E
PI_RW_GAP_2_F1	DDR_PI_OFS	42E	[30:16]	0012
PI_WP_GAP_3_F1	DDR_PI_OFS	436	[14:0]	0025
PI_WR_GAP_S_3_F1	DDR_PI_OFS	439	[14:0]	001E
PI_WR_GAP_L_3_F1	DDR_PI_OFS	43A	[30:16]	001E
PI_RW_GAP_3_F1	DDR_PI_OFS	43C	[14:0]	0012
PI_DARRAY3_0_CS0_F1	DDR_PI_OFS	4A7	[7:0]	24
PI_DARRAY3_1_CS0_F1	DDR_PI_OFS	4A7	[15:8]	52
PI_DARRAY3_0_CS1_F1	DDR_PI_OFS	4C5	[7:0]	24
PI_DARRAY3_1_CS1_F1	DDR_PI_OFS	4C5	[15:8]	52

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0.10	Feb. 2024	166	Correction of Table 5-4. Fixed the initial value of the PHY register.

Before:

Register Name	Address Offset (_OFS)	n [hex] (_OFS + n)	V4M
DDR_PI_229	DDR_PI_OFS	E5	0x0B02DF4D
DDR_PI_232	DDR_PI_OFS	E8	0x0000003A
DDR_PI_237	DDR_PI_OFS	ED	0x00080600
DDR_PI_239	DDR_PI_OFS	EF	0x0C00110D
DDR_PI_244	DDR_PI_OFS	F4	0x000000CB
DDR_PI_245	DDR_PI_OFS	F5	0x0000081C
DDR_PI_250	DDR_PI_OFS	FA	0x0B001901
DDR_PI_261	DDR_PI_OFS	105	0x00080004
DDR_PI_262	DDR_PI_OFS	106	0x04020019
DDR_PI_265	DDR_PI_OFS	109	0x00110039
DDR_PI_268	DDR_PI_OFS	10C	0x0001000E
DDR_PI_269	DDR_PI_OFS	10D	0x00040086
DDR_PI_273	DDR_PI_OFS	111	0x00870100
DDR_PI_274	DDR_PI_OFS	112	0x006C0087
DDR_PI_275	DDR_PI_OFS	113	0x01000037
DDR_PI_281	DDR_PI_OFS	119	0x0A07070D

After:

Register Name	Address Offset (_OFS)	n [hex] (_OFS + n)	V4M
DDR_PI_229	DDR_PI_OFS	E5	0x1002DF4D
DDR_PI_232	DDR_PI_OFS	E8	0x00000040
DDR_PI_237	DDR_PI_OFS	ED	0x000C0600
DDR_PI_239	DDR_PI_OFS	EF	0x10001511
DDR_PI_244	DDR_PI_OFS	F4	0x00000130
DDR_PI_245	DDR_PI_OFS	F5	0x00000C2E
DDR_PI_250	DDR_PI_OFS	FA	0x0F001B01
DDR_PI_261	DDR_PI_OFS	105	0x000A0004
DDR_PI_262	DDR_PI_OFS	106	0x08020019
DDR_PI_265	DDR_PI_OFS	109	0x0013003B
DDR_PI_268	DDR_PI_OFS	10C	0x0002000E
DDR_PI_269	DDR_PI_OFS	10D	0x000400C8
DDR_PI_273	DDR_PI_OFS	111	0x00C90100
DDR_PI_274	DDR_PI_OFS	112	0x00A100C9
DDR_PI_275	DDR_PI_OFS	113	0x01000051
DDR_PI_281	DDR_PI_OFS	119	0x0D09070D

Rev.	Date	Description Page	Summary
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Before:

Register Name	Address Offset (_OFS)	n [hex] (_OFS + n)	V4M
DDR_PI_289	DDR_PI_OFS	121	0x0014000E
DDR_PI_290	DDR_PI_OFS	122	0x00240086
DDR_PI_296	DDR_PI_OFS	128	0x00002500
DDR_PI_297	DDR_PI_OFS	129	0x220E002B
DDR_PI_299	DDR_PI_OFS	12B	0x00040006
DDR_PI_311	DDR_PI_OFS	137	0x09000A0C
DDR_PI_312	DDR_PI_OFS	138	0x0B090009
DDR_PI_313	DDR_PI_OFS	139	0x001741D0
DDR_PI_314	DDR_PI_OFS	13A	0x0A082002
DDR_PI_322	DDR_PI_OFS	142	0x00001038
DDR_PI_323	DDR_PI_OFS	143	0x0000A230
DDR_PI_326	DDR_PI_OFS	146	0x00CF0016
DDR_PI_334	DDR_PI_OFS	14E	0x0001A0AB
DDR_PI_338	DDR_PI_OFS	152	0x0000042B
DDR_PI_339	DDR_PI_OFS	153	0x000000CF
DDR_PI_348	DDR_PI_OFS	15C	0x02160040

After:

Register Name	Address Offset (_OFS)	n [hex] (_OFS + n)	V4M
DDR_PI_289	DDR_PI_OFS	121	0x0016000E
DDR_PI_290	DDR_PI_OFS	122	0x002400C8
DDR_PI_296	DDR_PI_OFS	128	0x00002900
DDR_PI_297	DDR_PI_OFS	129	0x220E002D
DDR_PI_299	DDR_PI_OFS	12B	0x00080008
DDR_PI_311	DDR_PI_OFS	137	0x09000F11
DDR_PI_312	DDR_PI_OFS	138	0x10090009
DDR_PI_313	DDR_PI_OFS	139	0x002262B8
DDR_PI_314	DDR_PI_OFS	13A	0x0C0C2003
DDR_PI_322	DDR_PI_OFS	142	0x0000185C
DDR_PI_323	DDR_PI_OFS	143	0x0000F398
DDR_PI_326	DDR_PI_OFS	146	0x01360016
DDR_PI_334	DDR_PI_OFS	14E	0x00027100
DDR_PI_338	DDR_PI_OFS	152	0x00000640
DDR_PI_339	DDR_PI_OFS	153	0x00000136
DDR_PI_348	DDR_PI_OFS	15C	0x03200040

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Before:

Register Name	Address Offset (_OFS)	n [hex] (_OFS + n)	V4M
DDR_PI_349	DDR_PI_OFS	15D	0x00010010
DDR_PI_352	DDR_PI_OFS	160	0x006B001B
DDR_PI_355	DDR_PI_OFS	163	0x06030503
DDR_PI_356	DDR_PI_OFS	164	0x0D0B0086
DDR_PI_360	DDR_PI_OFS	168	0x00CD0017
DDR_PI_483	DDR_PI_OFS	1E3	0x18061140
DDR_PI_484	DDR_PI_OFS	1E4	0x18861101
DDR_PI_492	DDR_PI_OFS	1EC	0x18061100
DDR_PI_493	DDR_PI_OFS	1ED	0x19A10D06
DDR_PI_494	DDR_PI_OFS	1EE	0x18051800
DDR_PI_495	DDR_PI_OFS	1EF	0x101B0001
DDR_PI_496	DDR_PI_OFS	1F0	0x181B0100
DDR_PI_497	DDR_PI_OFS	1F1	0x181B0200
DDR_PI_498	DDR_PI_OFS	1F2	0x181B0300
DDR_PI_499	DDR_PI_OFS	1F3	0x181B0400
DDR_PI_500	DDR_PI_OFS	1F4	0x1C440316

After:

Register Name	Address Offset (_OFS)	n [hex] (_OFS + n)	V4M
DDR_PI_349	DDR_PI_OFS	15D	0x00010018
DDR_PI_352	DDR_PI_OFS	160	0x006B0028
DDR_PI_355	DDR_PI_OFS	163	0x07040603
DDR_PI_356	DDR_PI_OFS	164	0x0D1000C8
DDR_PI_360	DDR_PI_OFS	168	0x01320017
DDR_PI_483	DDR_PI_OFS	1E3	0x18861101
DDR_PI_484	DDR_PI_OFS	1E4	0x181F0000
DDR_PI_492	DDR_PI_OFS	1EC	0x19A10D06
DDR_PI_493	DDR_PI_OFS	1ED	0x18051800
DDR_PI_494	DDR_PI_OFS	1EE	0x101B0001
DDR_PI_495	DDR_PI_OFS	1EF	0x181B0100
DDR_PI_496	DDR_PI_OFS	1F0	0x181B0200
DDR_PI_497	DDR_PI_OFS	1F1	0x181B0300
DDR_PI_498	DDR_PI_OFS	1F2	0x181B0400
DDR_PI_499	DDR_PI_OFS	1F3	0x1C440316
DDR_PI_500	DDR_PI_OFS	1F4	0x100D0000

Rev.	Date	Description Page	Summary
0.10	Feb. 2024	166	Correction of Table 5-4. Fixed the initial value of the PHY register.

Before:

Register Name	Address Offset (_OFS)	n [hex] (_OFS + n)	V4M
DDR_PI_501	DDR_PI_OFS	1F5	0x100D0000
DDR_PI_502	DDR_PI_OFS	1F6	0x101C0000
DDR_PI_978	DDR_PI_OFS	3D2	0x00000086
DDR_PI_981	DDR_PI_OFS	3D5	0x00000002
DDR_PI_984	DDR_PI_OFS	3D8	0x00000007
DDR_PI_987	DDR_PI_OFS	3DB	0x0000000B
DDR_PI_1002	DDR_PI_OFS	3EA	0x00000037
DDR_PI_1005	DDR_PI_OFS	3ED	0x0000006C
DDR_PI_1023	DDR_PI_OFS	3FF	0x00000087
DDR_PI_1037	DDR_PI_OFS	40D	0x001C0011
DDR_PI_1040	DDR_PI_OFS	410	0x001A0016
DDR_PI_1042	DDR_PI_OFS	412	0x0032001A
DDR_PI_1043	DDR_PI_OFS	413	0x0011000E
DDR_PI_1051	DDR_PI_OFS	41B	0x0043001C
DDR_PI_1054	DDR_PI_OFS	41E	0x0032001A
DDR_PI_1055	DDR_PI_OFS	41F	0x001A0016

After:

Register Name	Address Offset (_OFS)	n [hex] (_OFS + n)	V4M
DDR_PI_501	DDR_PI_OFS	1F5	0x101C0000
DDR_PI_502	DDR_PI_OFS	1F6	0x181F0000
DDR_PI_978	DDR_PI_OFS	3D2	0x000000C8
DDR_PI_981	DDR_PI_OFS	3D5	0x00000003
DDR_PI_984	DDR_PI_OFS	3D8	0x00000009
DDR_PI_987	DDR_PI_OFS	3DB	0x00000010
DDR_PI_1002	DDR_PI_OFS	3EA	0x00000051
DDR_PI_1005	DDR_PI_OFS	3ED	0x000000A1
DDR_PI_1023	DDR_PI_OFS	3FF	0x000000C9
DDR_PI_1037	DDR_PI_OFS	40D	0x00250011
DDR_PI_1040	DDR_PI_OFS	410	0x001E0016
DDR_PI_1042	DDR_PI_OFS	412	0x0032001E
DDR_PI_1043	DDR_PI_OFS	413	0x0012000E
DDR_PI_1051	DDR_PI_OFS	41B	0x00430025
DDR_PI_1054	DDR_PI_OFS	41E	0x0032001E
DDR_PI_1055	DDR_PI_OFS	41F	0x001E0016

Rev.	Date	Description Page	Summary
0.10	Feb. 2024	166	Correction of Table 5-4. Fixed the initial value of the PHY register. Before: Register Name / Address Offset (_OFS) / n [hex] (_OFS + n) / V4M DDR_PI_1057 / DDR_PI_OFS / 421 / 0x00290011 DDR_PI_1064 / DDR_PI_OFS / 428 / 0x001C0011 DDR_PI_1067 / DDR_PI_OFS / 42B / 0x001A0016 DDR_PI_1069 / DDR_PI_OFS / 42D / 0x0032001A DDR_PI_1070 / DDR_PI_OFS / 42E / 0x0011000E DDR_PI_1078 / DDR_PI_OFS / 436 / 0x0043001C DDR_PI_1081 / DDR_PI_OFS / 439 / 0x0032001A DDR_PI_1082 / DDR_PI_OFS / 43A / 0x001A0016 DDR_PI_1084 / DDR_PI_OFS / 43C / 0x00290011 DDR_PI_1191 / DDR_PI_OFS / 4A7 / 0x00F14914 DDR_PI_1221 / DDR_PI_OFS / 4C5 / 0x00F14914 After: Register Name / Address Offset (_OFS) / n [hex] (_OFS + n) / V4M DDR_PI_1057 / DDR_PI_OFS / 421 / 0x00290012 DDR_PI_1064 / DDR_PI_OFS / 428 / 0x00250011 DDR_PI_1067 / DDR_PI_OFS / 42B / 0x001E0016 DDR_PI_1069 / DDR_PI_OFS / 42D / 0x0032001E DDR_PI_1070 / DDR_PI_OFS / 42E / 0x0012000E DDR_PI_1078 / DDR_PI_OFS / 436 / 0x00430025 DDR_PI_1081 / DDR_PI_OFS / 439 / 0x0032001E DDR_PI_1082 / DDR_PI_OFS / 43A / 0x001E0016 DDR_PI_1084 / DDR_PI_OFS / 43C / 0x00290012 DDR_PI_1191 / DDR_PI_OFS / 4A7 / 0x00F15224 DDR_PI_1221 / DDR_PI_OFS / 4C5 / 0x00F15224
		216	Correction of Figure A3-1.
		221	Added Reference [4].

Rev.	Date	Description Page	Summary
0.20	May. 2024	—	Fixed incorrect / missing characters.
		—	Fixed the flowchart. A table number corresponding to processing has been added.
		9	The support code in Table 1-2 has been updated from 0.10 to 0.20.
		99	Correction of Table 5-3. Fixed the initial value of the PHY register. Before: V4M Bit Name / Address offset / n [hex] / Bit / Initial value [hex] PHY_DQ_OE_TIMING / DDR_PHY_SLICE_OFS / 55 / [23:16] / 41 After: V4M Bit Name / Address offset / n [hex] / Bit / Initial value [hex] PHY_DQ_OE_TIMING / DDR_PHY_SLICE_OFS / 55 / [23:16] / 51
		167	Correction of Table 5-4. Fixed the initial value of the PHY register. Before: Register Name / Address Offset (_OFS) / n [hex] (_OFS + n) / V4M DDR_PHY_SLICE_085 / DDR_PHY_SLICE_OFS / 55 / 0x90410503 After: Register Name / Address Offset (_OFS) / n [hex] (_OFS + n) / V4M DDR_PHY_SLICE_085 / DDR_PHY_SLICE_OFS / 55 / 0x90510503
		222	Reference [4] has been updated from Rev.0.01 to Rev.0.10.

Rev.	Date	Description Page	Summary
0.40	May. 2024	—	Fixed incorrect / missing characters.
		—	Fixed the flowchart. A table number corresponding to processing has been added.
		9	The support code in Table 1-2 has been updated from 0.20 to 0.40.
		21	Section 3.4 was fixed.
		32	Correction of Figure 4-4.
		53	Correction of Figure 4-5.
		60	Correction of Table 4-38. Before: **Op.** / **Bit Name** / **Data** / **Description** W / PHY_ADR_CALVL_SWIZZLE 0 / ((~(0xF0000000 & (0xF << (swap_num * 4)))) & bdcfg_ca_swap) | ((0x0000000F & (bdcfg_ca_swap >> 24)) << (swap_num * 4)) | 0x70000000) / The parameters are explained in Appendix A1.1. W / PHY_ADR_ADDR_SEL / ((~(0xF0000000 & (0xF << (swap_num * 4)))) & 0x06543210) | (0x6 << (swap_num * 4))) / | After: **Op.** / **Bit Name** / **Data** / **Description** W / PHY_ADR_CALVL_SWIZZLE 0 / (((~(0xF0000000 & (0xF << (swap_num * 4)))) & bdcfg_ca_swap) | ((0x0000000F & (bdcfg_ca_swap >> 24)) << (swap_num * 4)) | 0x70000000) / The parameters are explained in Appendix A1.1. W / PHY_ADR_ADDR_SEL / (((~(0xF0000000 & (0xF << (swap_num * 4)))) & 0x06543210) | (0x6 << (swap_num * 4))) / |
		66	Correction of Figure 4-8.
		67	Section 4.2.5.1 was fixed.
		68	Correction of Figure 4-9.
		69	Correction of Figure 4-10.
		74	Added Table 4-63, Table 4-67, Table 4-68, Table 4-69.
		84	Section 4.2.7 was fixed.
		84	Added Figure 4-15.
		86	Correction of Figure 4-16.

Rev.	Date	Description Page	Summary
0.40	May. 2024	99	Correction of Table 5-3. Fixed the initial value of the PHY register. Before: V4M Bit Name / Address offset / n [hex] / Bit / Initial value [hex] PHY_PLL_DESKEWCALIN_0 / DDR_PHY_ADR_G_OFS / 18 / [11:0] / 000 PHY_LP4_BOOT_PLL_DESKEWCALIN_0 / DDR_PHY_ADR_G_OFS / 18 / [27:16] / 000 PHY_PLL_DESKEWCALIN_1 / DDR_PHY_ADR_G_OFS / 1B / [11:0] / 000 PHY_LP4_BOOT_PLL_DESKEWCALIN_1 / DDR_PHY_ADR_G_OFS / 1B / [27:16] / 000 PHY_PLL_DESKEWCALIN_2 / DDR_PHY_ADR_G_OFS / 1E / [11:0] / 000 PHY_LP4_BOOT_PLL_DESKEWCALIN_2 / DDR_PHY_ADR_G_OFS / 1E / [27:16] / 000 After: V4M Bit Name / Address offset / n [hex] / Bit / Initial value [hex] PHY_PLL_DESKEWCALIN_0 / DDR_PHY_ADR_G_OFS / 18 / [11:0] / 001 PHY_LP4_BOOT_PLL_DESKEWCALIN_0 / DDR_PHY_ADR_G_OFS / 18 / [27:16] / 001 PHY_PLL_DESKEWCALIN_1 / DDR_PHY_ADR_G_OFS / 1B / [11:0] / 001 PHY_LP4_BOOT_PLL_DESKEWCALIN_1 / DDR_PHY_ADR_G_OFS / 1B / [27:16] / 001 PHY_PLL_DESKEWCALIN_2 / DDR_PHY_ADR_G_OFS / 1E / [11:0] / 001 PHY_LP4_BOOT_PLL_DESKEWCALIN_2 / DDR_PHY_ADR_G_OFS / 1E / [27:16] / 001
		167	Correction of Table 5-4. Fixed the initial value of the PHY register. Before: Register Name / Address Offset (_OFS) / n [hex] (_OFS + n) / V4M DDR_PHY_ADR_G_024 / DDR_PHY_ADR_G_OFS / 18 / 0x00000000 DDR_PHY_ADR_G_027 / DDR_PHY_ADR_G_OFS / 1B / 0x00000000 DDR_PHY_ADR_G_030 / DDR_PHY_ADR_G_OFS / 1E / 0x00000000 After: Register Name / Address Offset (_OFS) / n [hex] (_OFS + n) / V4M DDR_PHY_ADR_G_024 / DDR_PHY_ADR_G_OFS / 18 / 0x00010001 DDR_PHY_ADR_G_027 / DDR_PHY_ADR_G_OFS / 1B / 0x00010001 DDR_PHY_ADR_G_030 / DDR_PHY_ADR_G_OFS / 1E / 0x00010001
		222	Reference [4] has been updated from Rev.0.10 to Rev.0.40.

Rev.	Date	Description Page	Summary
0.50	Jul. 2024	—	Fixed incorrect / missing characters.
		—	Fixed the flowchart. A table number corresponding to processing has been added.
		9	Ver.2.0 has been added to the target products in Table 1-1.
		9	The support code in Table 1-2 has been updated from 0.40 to 0.50.
		16	Section 2 was fixed.
		19	The value of Ver.2.0 has been added to Table 3-1. Ver.2.0: 0x10
		53	Correction of Figure 4-5.
		57, 56, 57	Correction of Table 4-28, Table 4-29, Table 4-30. The following bit have been removed: PHY_DATA_DC_CAL_CLK_SEL, PHY_CLK_DC_CAL_CLK_SEL, PHY_CAL_CLK_SELECT_0
		57	Added Table 4-31, Table 4-32.
		60	Correction of Table 4-40.

Before:

Op.	Bit Name	Data	Description
W	PHY_ADR_CALVL_SWIZZLE0	(((~(0xF0000000 & (0xF << (swap_num * 4)))) & bdcfg_ca_swap) | ((0x0000000F & (bdcfg_ca_swap >> 24)) << (swap_num * 4)) | 0x70000000))	The parameters are explained in Appendix A1.1.
W	PHY_ADR_ADDR_SEL	(((~(0xF0000000 & (0xF << (swap_num * 4)))) & 0x06543210) | (0x6 << (swap_num * 4)))	

After:

Op.	Bit Name	Data	Description
W	PHY_ADR_CALVL_SWIZZLE0	(((~(0xF0000000 | (0xF << (swap_num * 4)))) & bdcfg_ca_swap) | ((0x0000000F & (bdcfg_ca_swap >> 24)) << (swap_num * 4)) | 0x70000000)	The parameters are explained in Appendix A1.1.
W	PHY_ADR_ADDR_SEL	(((~(0xF0000000 | (0xF << (swap_num * 4)))) & 0x06543210) | (0x6 << (swap_num * 4)))	

Rev.	Date	Description Page	Summary
0.50	Jul. 2024	89	Correction of Table 4-100.

Before:

Op.	Bit Name	Data	Description
W	PI_RDLVL_GATE_EN_F1	0x03	
W	PI_RDLVL_EN_F1	0x01	
W	PI_WDQLVL_EN_F1	0x01	
W	PI_RDLVL_GATE_EN_F2	0x03	
W	PI_RDLVL_EN_F2	0x03	
W	PI_WDQLVL_EN_F2	0x03	

After:

Op.	Bit Name	Data	Description
W	PI_RDLVL_GATE_EN_F1	0x03	
W	PI_RDLVL_EN_F1	0x01	
W	PI_WDQLVL_EN_F1	0x03	
W	PI_RDLVL_GATE_EN_F2	0x03	
W	PI_RDLVL_EN_F2	0x03	
W	PI_WDQLVL_EN_F2	0x03	

	211	Section A2 was fixed.
	211	Correction of Figure A2-1.
	222	Reference [3] has been updated from Rev.0.51 to Rev.0.70.
	222	Reference [4] has been updated from Rev.0.40 to Rev.0.50.

		Description	
Rev.	**Date**	**Page**	**Summary**
0.80	Sep. 2024	—	Fixed incorrect / missing characters.
		—	Fixed the flowchart. A table number corresponding to processing has been added.
		1	Added target device description. ・R-Car V4M-7 ・R-Car V4M-5 ・R-Car V4M-3 ・R-Car V4M-2
		9	The support code in Table 1-2 has been updated from 0.50 to 0.80.
		23	Added Table 3-4, Table 3-5, Table 3-6.
		69	Correction of Figure 4-10.
		205	Added Table 5-8.
		222	Reference [4] has been updated from Rev.0.50 to Rev.0.80.

Rev.	Date	Description Page	Summary
0.90	Nov. 2024	—	Fixed incorrect / missing characters.
		—	Fixed the flowchart. A table number corresponding to processing has been added.
		9	The support code in Table 1-2 has been updated from 0.80 to 0.90.
		99	Correction of Table 5-3. Before: V4M Bit Name / Address offset / n [hex] / Bit / Initial value [hex] PHY_IE_MODE / DDR_PHY_SLICE_OFS / 5A / [17:16] / 0 After: V4M Bit Name / Address offset / n [hex] / Bit / Initial value [hex] PHY_IE_MODE / DDR_PHY_SLICE_OFS / 5A / [17:16] / 1
		167	Correction of Table 5-4. Before: Register Name / Address Offset (_OFS) / n [hex] (_OFS + n) / V4M DDR_PHY_SLICE_090 / DDR_PHY_SLICE_OFS / 5A / 0x010000C0 After: Register Name / Address Offset (_OFS) / n [hex] (_OFS + n) / V4M DDR_PHY_SLICE_090 / DDR_PHY_SLICE_OFS / 5A / 0x010100C0
		222	Reference [3] has been updated from Rev.0.70 to Rev.0.71.
		222	Reference [4] has been updated from Rev.0.80 to Rev.0.90.

Rev.	Date	Description Page	Summary
1.00	Jan. 2025	—	Fixed incorrect / missing characters.
		—	Fixed the flowchart. A table number corresponding to processing has been added.
		9	The support code in Table 1-2 has been updated from 0.90 to 1.00.
		22	Correcting name in Table 3-3.
		23	Correcting name in Table 3-4, Table 3-5, Table 3-6.
		205	Correction of Table 5-8. Before: Register Name / Abbreviation / R/W / Value after Reset / Address / Bit Name / Bit OTP_MEM Monitor Register 60 / OTPMONITOR60 / R / --- / 0xE61B F1F0 / ID_REG / [7:0] After: Register Name / Abbreviation / R/W / Value after Reset / Address / Bit Name / Bit OTP_MEM Monitor Register 17 / OTPMONITOR17 / R / --- / 0xE61B F144 / ID_REG / [7:0]
		222	Reference [3] has been updated from Rev.0.71 to Rev.0.80.
		222	Reference [4] has been updated from Rev.0.90 to Rev.1.00.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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