Design Guide

R-Car V4M
FCBGA 19.0sq

PCB design guide for LPDDR4X

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R-Car V4M / LPDDR4X

DDR PCB Design Guide

Introduction

This guideline provides a brief explanation of a PCB design which satisfy verification items in the following document:

[Ref] R-Car V4M FCBGA 19p0sq PCB verification guide for LPDDR4X

The verification items of signal line and IO PDN in the [Ref] must be checked even if you copy the layout.

Target Device

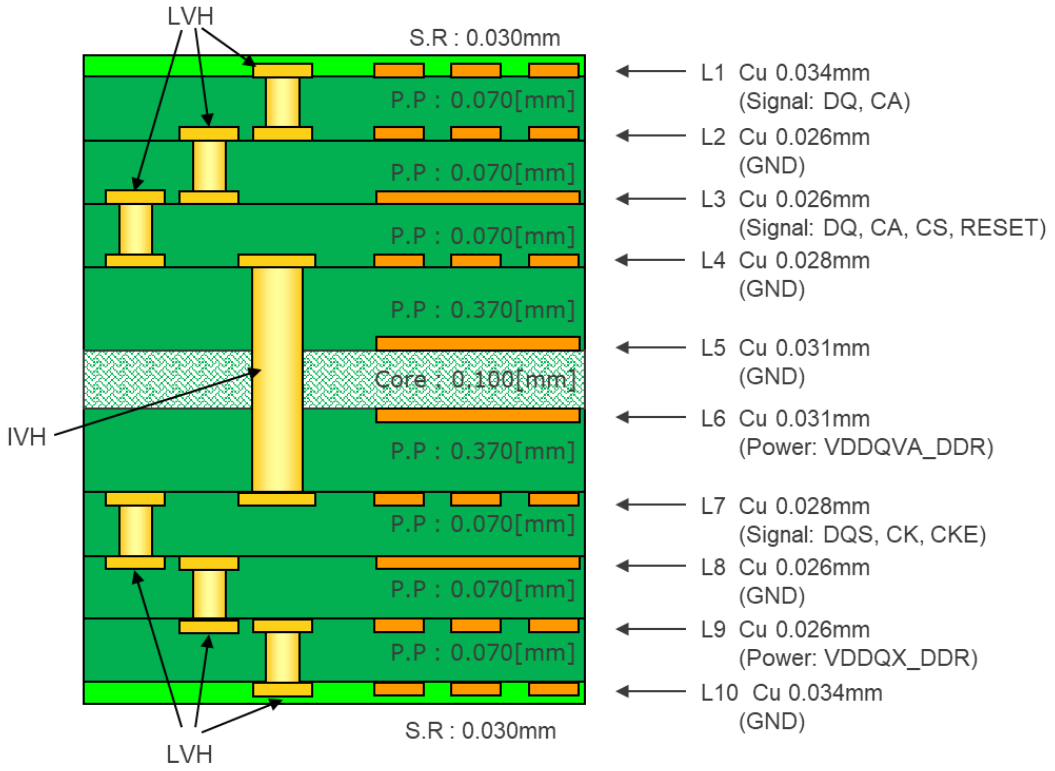
LPDDR4X of R-Car V4M (FCBGA 19sq)
/ 10-Layer Build-Up (3-4-3) Board
/ 1 pcs of x32 DRAM Structure
/ N01

Contents

1. Basic information

1.1 PCB structure

This guideline is written assuming the following layer structure.
The signal, ground and power layer assignment is as follows.
Signal names represent layers where these signal traces are mainly routed.



10-Layer Build-Up(3-4-3)
Base Material : FR-4
[Dielectric constant : Relative permittivity / Loss tangent]
Solder Resist (SR 0.030mm): 3.7/0.017 (in case of 1GHz)
Prepreg (PP 0.070mm): 4.1/0.013 (in case of 1GHz)
Prepreg (PP 0.370mm): 4.6/0.010 (in case of 1GHz)
Core (PP 0.100mm): 4.6/0.010 (in case of 1GHz)

Figure 1-1. PCB layer structure

1.2 Design rule

This guideline was written assuming the following design rule.

◆ Through-hole specifications

1. Build-Up section (LVH: L1-L2-L3-L4 Layer, L7-L8-L9-L10 Layer)
   VIA diameter: 0.1mm (laser-processed)
   Land diameter: 0.275mm
2. Through-via holes (IVH: L4-L7 Layer)
   VIA diameter: 0.2mm (drilled)
   Land diameter (surface layer): SOC side 0.5mm / DRAM side 0.5mm
   Land diameter (internal layer): SOC side 0.5mm / DRAM side 0.5mm
   Internal layer clearance diameter: SOC side 0.7mm / DRAM side 0.7mm

◆ Line width / Space (Min.)

Single-ended: 0.100mm / 0.100mm
Differential: 0.100mm / pair gap 0.100mm / GND guard gap 0.100mm

◆ BGA ball land diameter (PAD dimension)

SOC: 0.34mm (Resist opening diameter: 0.44mm)
DRAM: 0.32mm (Resist opening diameter: 0.42mm)

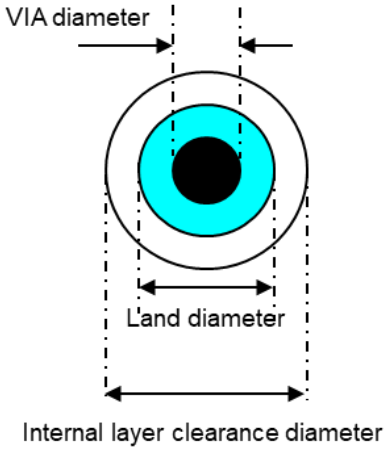


Figure 1-2. Definition on design rule

2. IO setting and PCB configuration

2.1 IO setting for LPDDR4X

Drivability and ODT setting during WRITE and READ operation are set as the following table.
SOC IBIS models are also listed. Proper DRAM model must be selected based on materials provided by DRAM vender.

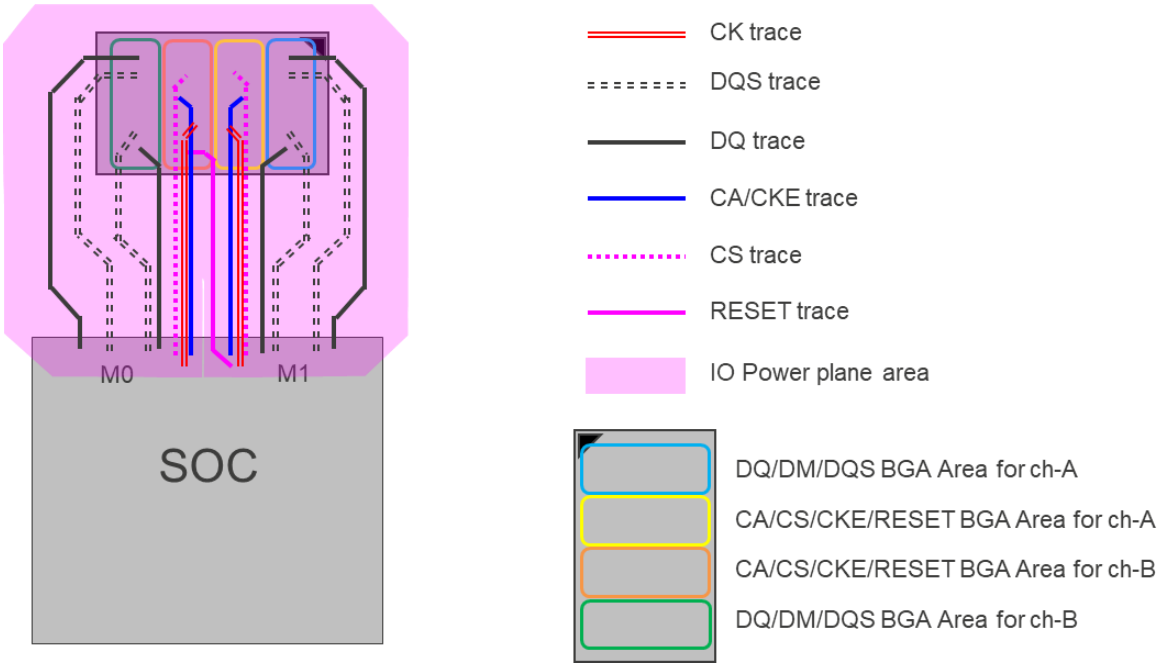
Table 2-1. IO setting for LPDDR4X

DDR IF signals	Operation	SOC			DRAM		Number of connected DRAM(s)	Series resistor	Termination resistor
		Drivability	ODT	IBIS model selection	Drivability	ODT			
CK/ CK#	Write	PU : 34ohm PD : 34ohm	OFF	lpddr4x_ocd_34p_34n_diff / lpddr4x_ocd_34p_34n_diff	OFF	60ohm	1	-	-
DQS/ DQS#	Write	PU : 34ohm PD : 34ohm	OFF	lpddr4x_ocd_34p_34n_diff / lpddr4x_ocd_34p_34n_diff	OFF	60ohm	1	-	-
	Read	OFF	40ohm	lpddr4x_odt_40_diff / lpddr4x_odt_40_diff	VOH=0.5*VDDQ SOC ODT=RZQ/6 PDDS=RZQ/6	OFF			
DQ, DM	Write	PU : 34ohm PD : 34ohm	OFF	lpddr4x_ocd_34p_34n	OFF	60ohm	1	-	-
	Read	OFF	40ohm	lpddr4x_odt_40	VOH=0.5*VDDQ SOC ODT=RZQ/6 PDDS=RZQ/6	OFF			
CA	Write	PU : 40ohm PD : 40ohm	OFF	lpddr4x_ocd_40p_40n	OFF	60ohm	1	-	-
CS	Write	PU : 40ohm PD : 40ohm	OFF	lpddr4x_ocd_40p_40n	OFF	60ohm	1	-	-
CKE	Write	PU : 640ohm *1) PD : 240ohm	OFF	lpddr4x_cke_240p_240n	-	-	1	-	-
RESET	Write	PU : 50ohm PD : 50ohm	OFF	lpddr4x_ocd_50p_50n	-	-	1	-	-
ODT	-	No signal	No signal	-	-	-	1	-	Please contact DRAM vendor.

*1) The model name is “lpddr4x_cke_240p_240n”, but only the drivability on PU side is about 640ohm.

2.2 PCB configuration

This guideline is written assuming the following placement of parts on L1.
Topology of signal trace and IO power plane configuration are depicted in the figure.



Notes: 1. Detailed topology of each signal is described in succeeding pages.
2. IO power plane is placed to cover all signal traces of DDR and DRAM device as the above figure.

Figure 2-1. PCB configuration

3. Topology of signal trace

3.1 CK topology

The trace topology is the following figure. The CK and CK# is a differential pair.
L1, L2, L3, L4, and L7 show trace layer and 'a0' to 'i0#' show trace element name.

Trace width *)

e0/e0#: 0.200mm

Trace space *)

'e0' - 'e0#': 0.150mm, 'e0/e0#' - 'GND shield': 0.100mm

Trace length(delay))

Each trace element is equal as much as possible:
a0=a0#, b0=b0#, c0=c0#, d0=d0#, e0=e0#, f0=f0#, g0=g0#, h0=h0#, i0=i0#
Trace lengths except the main trace are shortened as much as possible.

GND shield)

GND shield trace is applied to the differential pair.
These GND shield traces are connected to GND plane at start/end and some middle points by vias.

* Main trace on L7 (e0, e0#). Differential impedances of the pairs are described in the figure.
* Fine value of trace width and trace space are rounded.

The following skew need to be managed:

Intra-pair skew between the true and complement signal of differential pair.

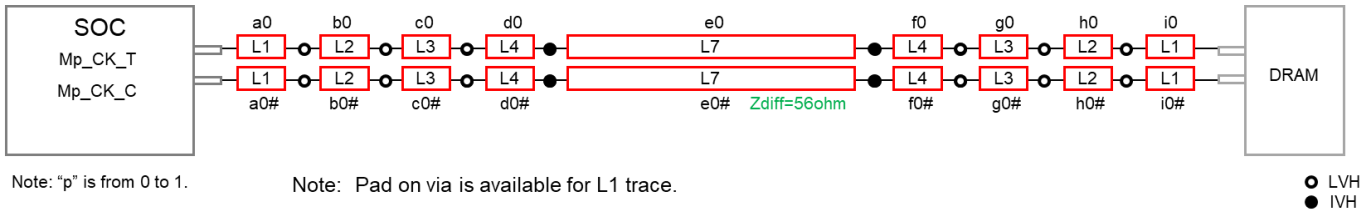


Figure 3-1. CK topology

3.2 DQS topology

The trace topology is the following figure. The DQS and DQS# is a differential pair.
L1, L2, L3, L4, and L7 show trace layer and 'a0' to 'i0#' show trace element name.

Trace width *)

e0/e0#: 0.200mm

Trace space *)

'e0' - 'e0#': 0.150mm, 'e0/e0#' - 'GND shield': 0.100mm

Trace length(delay))

Each trace element is equal as much as possible:
a0=a0#, b0=b0#, c0=c0#, d0=d0#, e0=e0#, f0=f0#, g0=g0#, h0=h0#, i0=i0#
Trace lengths except the main trace are shortened as much as possible.

GND shield)

GND shield trace is applied to the differential pair.
These GND shield traces are connected to GND plane at start/end and some middle points by vias.

* Main trace on L7 (e0, e0#). Differential impedances of the pairs are described in the figure.
* Fine value of trace width and trace space are rounded.

The following skew need to be managed:

Intra-pair skew between the true and complement signal of differential pair.
Difference between DQS and CK.
Sum of CK and DQS (flight-time).

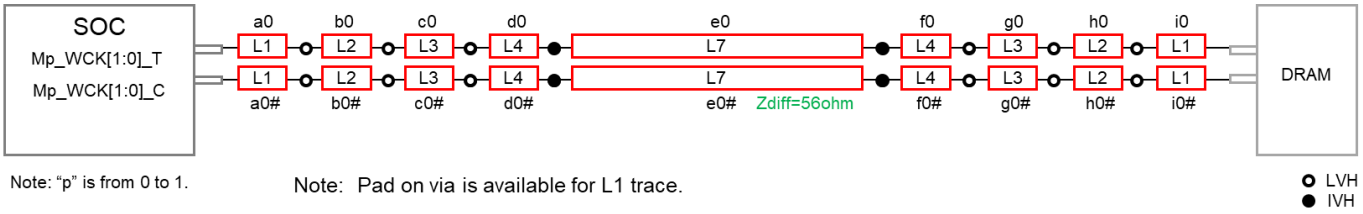


Figure 3-2. DQS topology

3.3 DQ topology

The trace topology is the following figure.
L1, L2, and L3 show trace layer and 'a0' to 'e1' show trace element name.

Trace width *)

a0: 0.200mm, c1: 0.100mm

Trace length(delay))

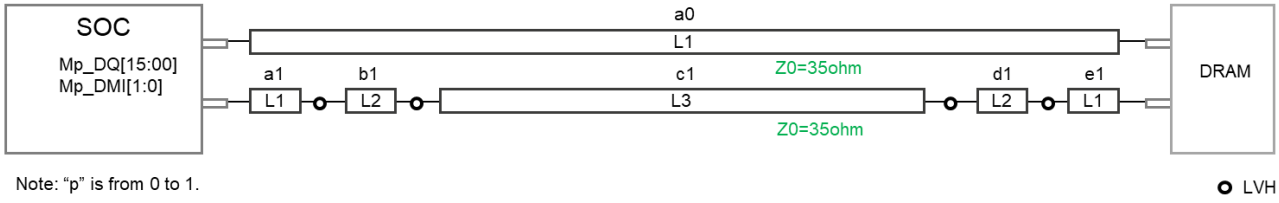
Trace lengths except the main trace are shortened as much as possible.

* Main trace on L1 (a0) and L3 (c1). Characteristic impedances of these traces are described in the figure.
* Fine value of trace width and trace space are rounded.

The following skew need to be managed:

Difference between DQ/DM and DQS in same byte lane.

Difference among DQ/DM in same byte lane.



Note: Pad on via is available for L1 trace.

Note: In order to consider the impedance matching, the trace width is slightly changed in one trace. Please refer to the PCB layout for details.

Figure 3-3. DQ topology

3.4 CA topology

The trace topology is the following figure.
L1, L2, and L3 show trace layer and ‘a0’ to ‘e1’ show trace element name.

Trace width *)

a0: 0.200mm, c1: 0.100mm

Trace length(delay))

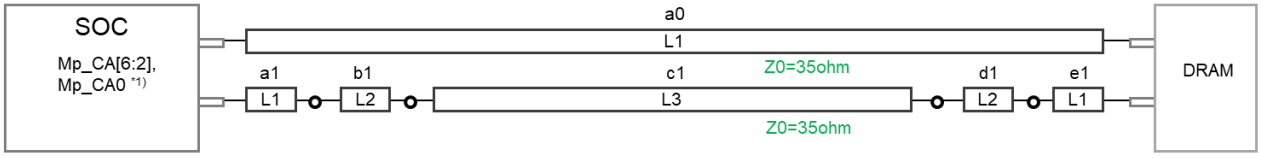
Trace lengths except the main trace are shortened as much as possible.

* Main trace on L1 (a0) and L3 (c1). Characteristic impedances of these traces are described in the figure.
* Fine value of trace width and trace space are rounded.

The following skew need to be managed:

Difference between CA and CK.

Difference among CAs.



Note: “p” is from 0 to 1.

*1) Mp_CA1 cannot be used for LPDDR4X. Please use Mp_CA6 instead of Mp_CA1.

o LVH

Note: Pad on via is available for L1 trace.

Note: In order to consider the impedance matching, the trace width is slightly changed in one trace. Please refer to the PCB layout for details.

Figure 3-4. CA topology

3.5 CS topology

The trace topology is the following figure.
L1, L2, and L3 show trace layer and ‘a0’ to ‘e0’ show trace element name.

Trace width *)

c0: 0.100mm

Trace length(delay))

Trace lengths except the main trace are shortened as much as possible.

* Main trace on L3 (c0). Characteristic impedances of these traces are described in the figure.
* Fine value of trace width and trace space are rounded.

The following skew need to be managed **:

Difference between CS and CK.

** CS-CS, CA-CS skew are automatically satisfied if CA-CK, CS-CK skew are satisfied.

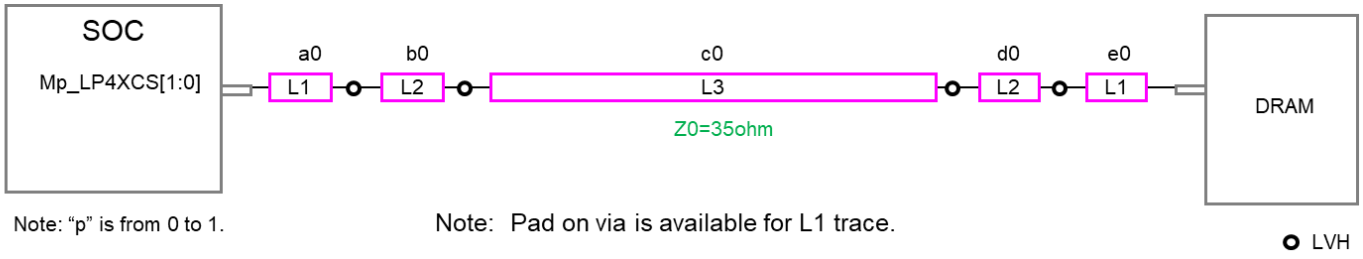


Figure 3-5. CS topology

3.6 CKE topology

The trace topology is the following figure.
L1, L2, L3, L4, and L7 show trace layer and ‘a0’ to ‘i0’ show trace element name.

Trace width *)

e0: 0.100mm

Trace length(delay))

Trace lengths except the main trace are shortened as much as possible.

* Main trace on L7 (e0). Characteristic impedances of these traces are described in the figure.
* Fine value of trace width and trace space are rounded.

The following skew need to be managed:

Difference between CKE and CK is not restricted tightly.

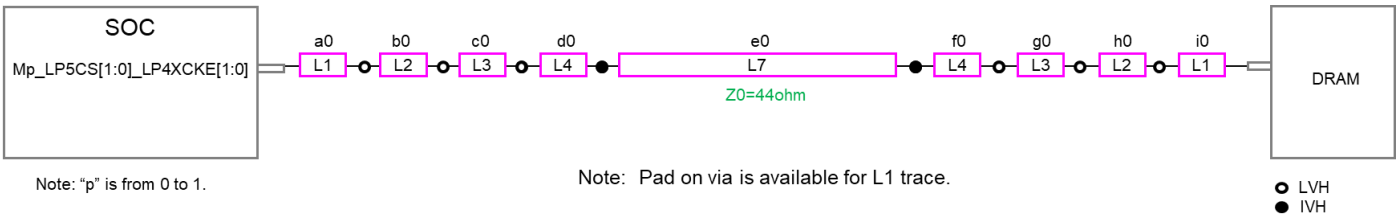


Figure 3-6. CKE topology

3.7 RESET topology

The trace topology is the following figure.
L1, L2, and L3 show trace layer and ‘a0’ to ‘e0’ show trace element name.

Trace width *)

c0: 0.100mm

Trace length(delay))

Trace lengths except the main trace are shortened as much as possible.

* Main trace on L3 (c0). Characteristic impedances of these traces are described in the figure.
* Fine value of trace width and trace space are rounded.

The skew between RESET and the other signals does not need to be managed tightly.

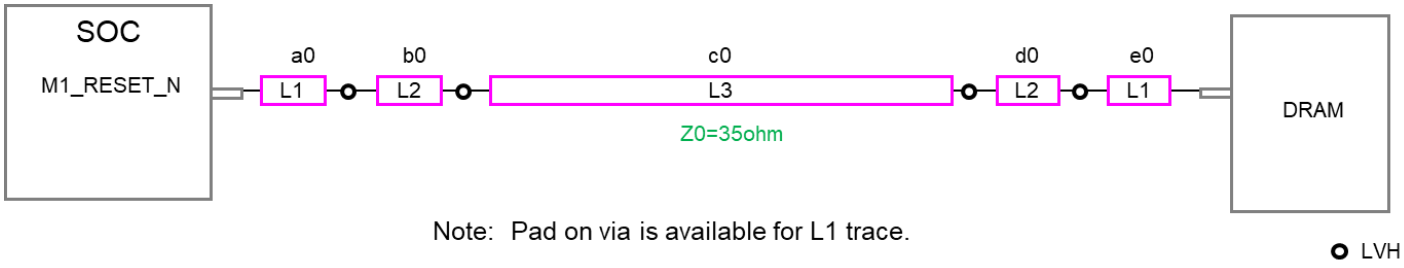


Figure 3-7. RESET topology

4. Configuration of IO Power Delivery Network (PDN)

4.1 VDDQVA_DDR and VDDQX_DDR configuration

The VDDQVA_DDR and VDDQX_DDR configuration to satisfy the target impedance is shown in following figure and table.

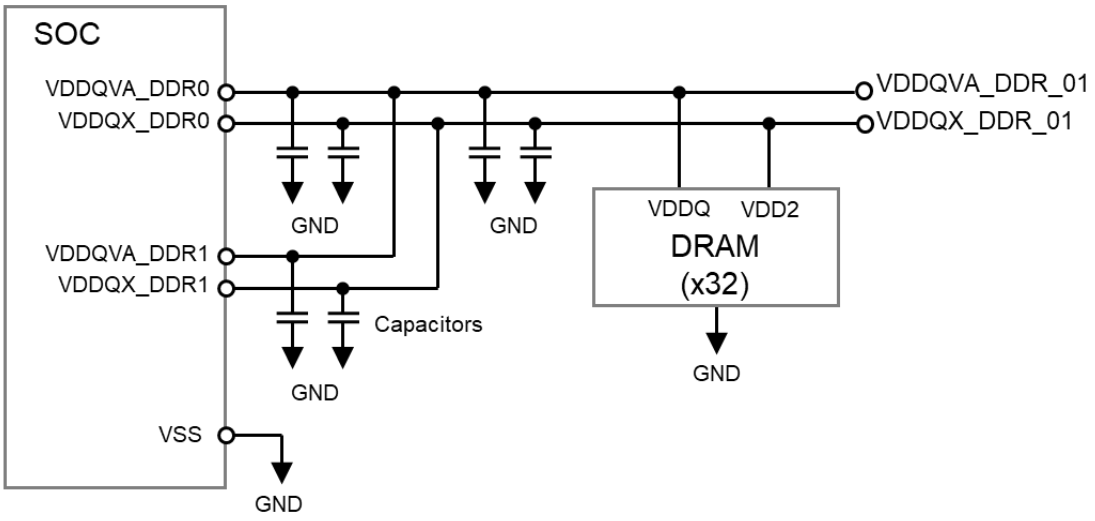


Figure 4-1. VDDQVA_DDR and VDDQX_DDR configuration

Table 4-1. Capacitor selection for VDDQVA_DDR

Value	Pics.
	VDDQVA_DDR
1uF	6
0.1uF	13
0.01uF	2
2200pF	1
1000pF	1
470pF	2
330pF	2
220pF	6
100pF	6
68pF	1

Table 4-2. Capacitor selection for VDDQX_DDR

Value	Pics.
	VDDQX_DDR
22uF	1
1uF	7
0.1uF	13
330pF	2
220pF	1
100pF	7

Revision History

Rev.	Date	Description	
		Page	Summary
0.90	2023/12/27	-	Newly issued as preliminary version.
1.00	2024/09/30	-	Upgrade to revision 1.00.

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1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
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