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User's Guide

Printed Circuit Board Design Guidelines for Serial Interface with R-Car V4M

User's Guide: Hardware

RENESAS
SoCs for Automotive

PCI Express
CSI/DSI

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R-Car V4M

Design Guideline

Introduction

This user's guide describes design guidelines for Serial Interface PCBs of R-Car V4M.

Target Device

R-Car V4M PCI Express (PCI Express Gen4.0)

R-Car V4M DSI/CSI

Contents

1. Preface

This document describes the design guidelines for PCB of serial interface with R-Car V4M.

1.1 PCI Express General Information

For general information on electric and transfer path characteristics, and on connector specifications required in designing printed circuit boards including PCI Express connections, refer to the specifications issued by the standards certification bodies listed in Table 1-1.

Table 1-1 Standard Applicable to PCI Express

Standards Certification Body	Title of specification
PCI-SIG	PCI Express® Base Specification Revision 4.0
	PCI Express Card Electromechanical Specification Revision 4.0

1.2 DSI General Information

For general information on electric and transfer path characteristics, and on connector specifications required in designing printed circuit boards connections, refer to the specifications issued by the standards certification bodies listed in Table 1-2.

Table 1-2 Standard Applicable to DSI

Standards Certification Body	Title of specification
MIPI Alliance	MIPI Alliance Specification for D-PHY Version 1.2
	MIPI Alliance Test Program, D-PHY Physical Layer Conformance Test Suite Version v1.2 rel11

1.3 CSI General Information

For general information on electric and transfer path characteristics, and on connector specifications required in designing printed circuit boards including MIPI connections, refer to the specifications(for the maximum supported bit rate) issued by the standards listed in Table 1-3.

Table 1-3 Standard Applicable to CSI

Standards	Title of specification
mipi alliance Errata 01 for MIPI D-PHY℠ Specification v2.1	Chapter 8 Interconnect and Lane Configuration
	Chapter 8.6.1 Differential Characteristics
	Chapter 8.6.2 Common-mode Characteristics
	Chapter 8.6.3 Intra-Lane Cross-Coupling
	Chapter 8.6.4 Mode-Conversion Limits
	Chapter 8.6.5 Inter-Lane Cross-Coupling
	Chapter 8.6.6 Inter-Lane Static Skew (or, Chapter 10.2.4 is met)
	Chapter 10.2.1.1/10.2.1.2 Data-Clock Timing Specifications If the target datarate is ≥ 0.08 Gbps and ≤ 1.5Gbps, the specification related to Channel Skew needs to be verified. Simulation bench of the document shown in Table 3-3 can be used in the verification for Channel Skew. In the same time, please check if VDIR_RX ≥ 70mV.
	Chapter 10.2.4 Receiver Eye Diagram Specification TEYE_RX >= 0.8UI (*1) VDIF_RX ≧ 40mV *1 TEYE_RX is replaced to 0.8UI from 0.5UI. 0.8UI is the value that does not include TX jitter and only takes PCB jitter into account. Please refer to the [Procedure] in the chapter 3.1 of the document shown in Table 3-3.

2. Pins information of Serial Interface

2.1 Signal pins

The list of R-Car V4M serial interface signal pins is shown in Table 2-1.

Table 2-1. Signal pins of R-Car V4M Serial Interface

Module	Pin Name	Pin Function	Voltage Range
PCI Express ch0	PCIE0_CLK_P	PCI Express ch0 REFCLK pin (pos)	0-VDD
	PCIE0_CLK_M	PCI Express ch0 REFCLK pin (neg)	0-VDD
	PCIE0_TX0_P	PCI Express ch0 lane0 Tx (pos)	0-VDD
	PCIE0_TX0_M	PCI Express ch0 lane0 Tx (neg)	0-VDD
	PCIE0_RX0_P	PCI Express ch0 lane0 Rx (pos)	0-VDD
	PCIE0_RX0_M	PCI Express ch0 lane0 Rx (neg)	0-VDD
	PCIE0_TX1_P	PCI Express ch0 lane1 Tx (pos)	0-VDD
	PCIE0_TX1_M	PCI Express ch0 lane1 Tx (neg)	0-VDD
	PCIE0_RX1_P	PCI Express ch0 lane1 Rx (pos)	0-VDD
	PCIE0_RX1_M	PCI Express ch0 lane1 Rx (neg)	0-VDD
	PCIE0_RESREF	Pin for connecting the external reference resistor of PCI Express ch0	0-VDD
DSI0	DSI0_CLKP	DSI0 MIPI transmitter positive output (clock)	(Note1)
	DSI0_CLKN	DSI0 MIPI transmitter negative output (clock)	(Note1)
	DSI0_DATAP0	DSI0 MIPI transmitter positive output (ch0)	(Note1)
	DSI0_DATAN0	DSI0 MIPI transmitter negative output (ch0)	(Note1)
	DSI0_DATAP1	DSI0 MIPI transmitter positive output (ch1)	(Note1)
	DSI0_DATAN1	DSI0 MIPI transmitter negative output (ch1)	(Note1)
	DSI0_DATAP2	DSI0 MIPI transmitter positive output (ch2)	(Note1)
	DSI0_DATAN2	DSI0 MIPI transmitter negative output (ch2)	(Note1)
	DSI0_DATAP3	DSI0 MIPI transmitter positive output (ch3)	(Note1)
	DSI0_DATAN3	DSI0 MIPI transmitter negative output (ch3)	(Note1)
	DSI0_REXT	DSI0 external resistor pin	0-VDD18

CSI0 MIPI receiver	CSI0_DATAP0	Positive input (data lane0 for DPHY)	(Note1)
	CSI0_DATAN0	Negative input (data lane0 for DPHY)	(Note1)
	CSI0_DATAP1	Positive input (data lane1 for DPHY)	(Note1)
	CSI0_DATAN1	Negative input (data lane1 for DPHY)	(Note1)
	CSI0_CLKP	Positive input (clock lane for DPHY)	(Note1)
	CSI0_CLKN	Negative input (clock lane for DPHY)	(Note1)
	CSI0_DATAP2	Positive input (data lane2 for DPHY)	(Note1)
	CSI0_DATAN2	Negative input (data lane2 for DPHY)	(Note1)
	CSI0_DATAP3	Positive input (data lane3 for DPHY)	(Note1)
	CSI0_DATAN3	Negative input (data lane3 for DPHY)	(Note1)
	CSI0_REXT	CSI0 external resistor pin	0-VDD18
CSI1 MIPI receiver	CSI1_DATAP0	Positive input (data lane0 for DPHY)	(Note1)
	CSI1_DATAN0	Negative input (data lane0 for DPHY)	(Note1)
	CSI1_DATAP1	Positive input (data lane1 for DPHY)	(Note1)
	CSI1_DATAN1	Negative input (data lane1 for DPHY)	(Note1)
	CSI1_CLKP	Positive input (clock lane for DPHY)	(Note1)
	CSI1_CLKN	Negative input (clock lane for DPHY)	(Note1)
	CSI1_DATAP2	Positive input (data lane2 for DPHY)	(Note1)
	CSI1_DATAN2	Negative input (data lane2 for DPHY)	(Note1)
	CSI1_DATAP3	Positive input (data lane3 for DPHY)	(Note1)
	CSI1_DATAN3	Negative input (data lane3 for DPHY)	(Note1)
	CSI1_REXT	CSI1 external resistor pin	0-VDD18

Note

1. Voltage Range is based on MIPI specification.

2.2 Power supply pins

The list of R-Car V4M serial interface power supply pins is shown in Table 2-2.

Table 2-2. Power supply pins of R-Car V4M Serial Interface

Module	Pin Name	Pin Function
PCI Express ch0	VDD_PCIE0	Analog supply for PCI Express ch0
	VDD18_PCIE0	High Voltage IO supply for PCI Express ch0
DSI0	VDD_DSI0	Analog supply for MIPI DPHY DSI0
	VDD_DSI0PLL	Analog Low Voltage for MIPI DPHY DSI0's PLL
	VDD18_DSI	Analog high voltage supply for MIPI DPHY
CSI0 MIPI Receiver	VDD_CSI0	Analog supply for MIPI CDPHY
	VDD18_CSI0	Analog high voltage supply for MIPI CDPHY
CSI1 MIPI Receiver	VDD_CSI1	Analog supply for MIPI CDPHY
	VDD18_CSI1	Analog high voltage supply for MIPI CDPHY

2.3 Pin assignment of Serial Interface

2.3.1 R-Car V4M Pin assignment of Serial Interface

The diagram for pin assignment of R-Car V4M serial interface modules is shown in Figure 2-1. In the diagram, only the area around the pins of serial interface is cut out and described.

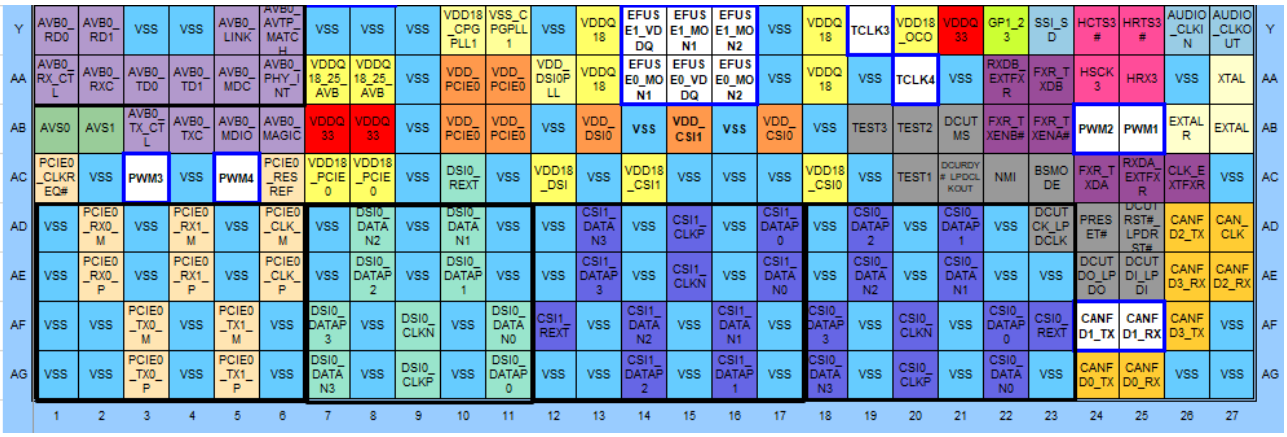

Figure 2-1 Diagram for pin assignment of R-Car V4M Serial Interface (PKG TOP View)

3. Signal line design guidelines

3.1 Signal Integrity Analysis

Each of the RX and TX differential routes must be designed and simulated to ensure signal integrity quality for serial interface.

3.1.1 IBIS-AMI Models for Signal Integrity Analysis for PCI Express modules

IBIS Algorithmic Modeling Interface (IBIS-AMI) model of the PCI Express modules is provided for signal integrity analysis. The following application note in Table 3-1 details the provided IBIS-AMI model.

Table 3-1. SerDes Interface IBIS-AMI Model Application Note for PCI Express modules

Type	Document Name
Application Note (PCIe)	*R-CarV4M SerDes Interface IBIS-AMI Model Application Note*

3.1.2 IBIS Models for Signal Integrity Analysis for DSI modules

IBIS model of the DSI module is provided for signal integrity analysis. The following IBIS model file is included these models.

Table 3-2. SerDes Interface IBIS Model File for DSI module

Type	File Name
IBIS model file	*r8a779h0.ibs*

3.1.3 S-Parameter Models for Signal Integrity Analysis for CSI modules

S-parameter models of the CSI modules are provided for signal integrity analysis. The following application note in Table 3-3 details the provided S-parameter model.

Table 3-3. SerDes Interface S-parameter Model File for CSI modules

Type	Document Name
Application Note (CSI)	*r01an6768ej0100-r-carv4m-mipi-dphy-rx-spara-model.docx*

4. Power line design guidelines

4.1 Power Integrity Analysis

The power distribution network (PDN) for each of the serial interface module supplies must be designed and simulated to ensure power integrity requirements.

4.2 Power Supply Connections

For each power supply, the bypass capacitors and filter isolation as shown in Figure 4-1 must be considered. Please see the target characteristics shown in chapter 4.3.

[Note] To obtain good ESD performance, please make a common ground between R-Car package and PCB.

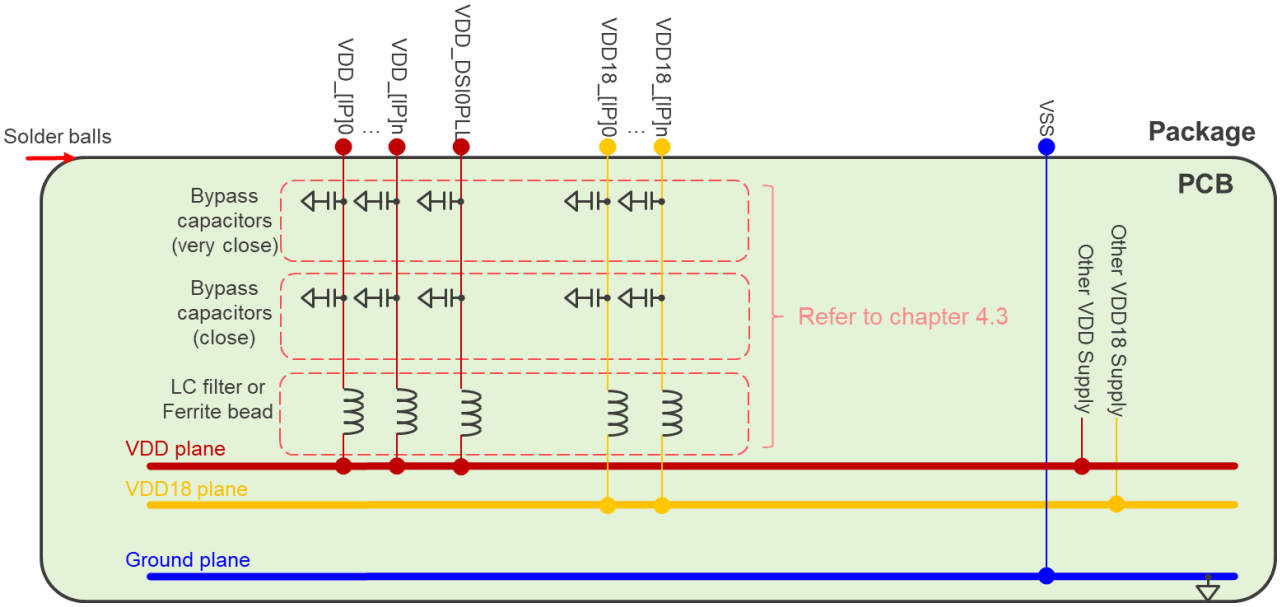

Figure 4-1 Power Supply Connections

4.3 Power integrity requirement

4.3.1 Target inductance and impedance requirement

The target inductance and impedance are shown in Table 4-1.

The inductance and impedance can be obtained by calculating loop inductance and impedance from the VDD ball of the package to the VSS balls of the package taken as an ideal GND in the way shown in Figure 4-2. Bypass Capacitor Models should include the ESL and the ESR.

Please check that the impedance on PCB is less than the target impedance curve. Target inductance is just a guide for an initial estimate.

[Note] This target contains only a self-impedance component. Therefore, please place ground shield between the power supply lines to minimize mutual impedance as a factor in transmitting noise from power supply line of other IPs.

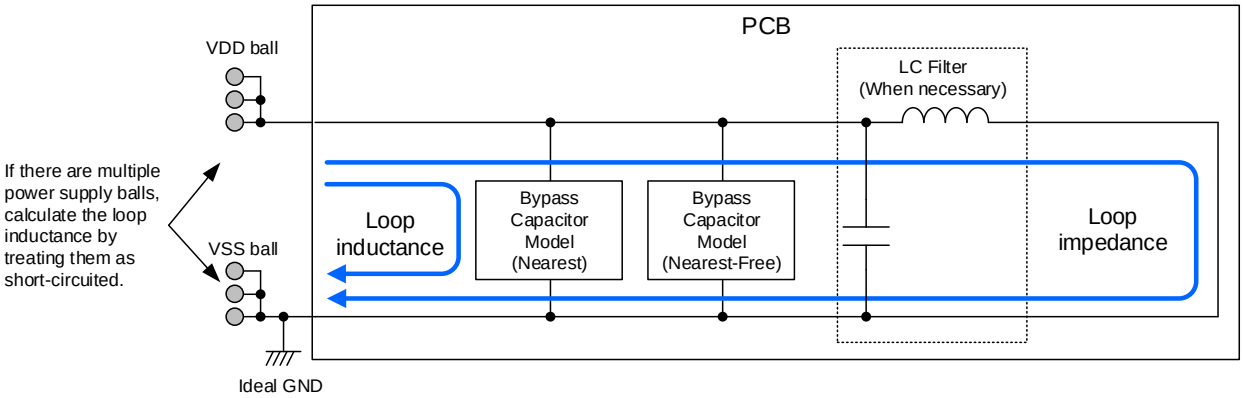

Figure 4-2 Concept of loop inductance and impedance

Table 4-1. R-Car V4M Target inductance and recommended bypass capacitors

Module	Pin Name	Target inductance	Target Impedance curve
PCI Express ch0	VDD_PCIE0	1.66nH	Figure 4-3
	VDD18_PCIE0	6.00nH	Figure 4-3
DSI0	VDD_DSI0	3.46nH	Figure 4-4
	VDD_DSI0PLL	2.69nH	Figure 4-4
	VDD18_DSI	6.00nH	Figure 4-4
CSI0,1 MIPI Receiver	VDD_CSI0	3.67nH	Figure 4-5
	VDD_CSI1	3.67nH	Figure 4-5
	VDD18_CSI0	6.00nH	Figure 4-5
	VDD18_CSI1	6.00nH	Figure 4-5

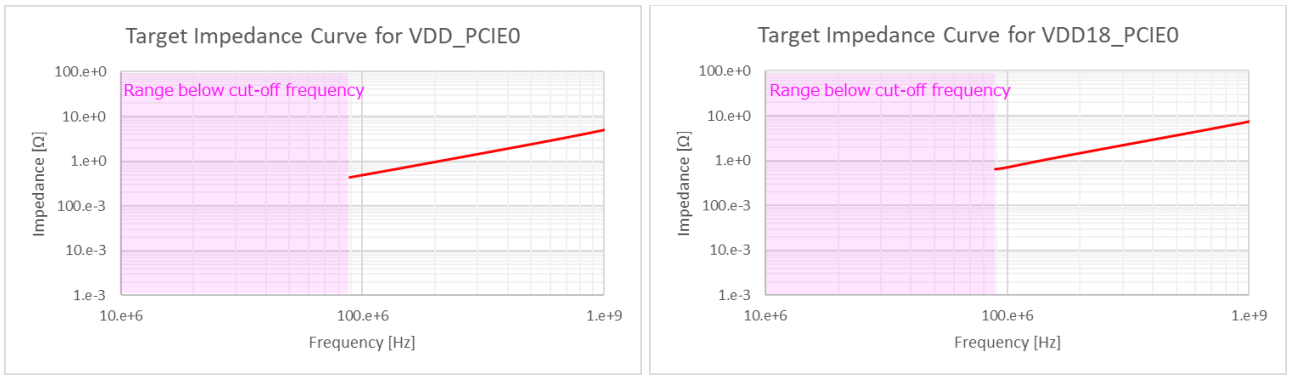

Figure 4-3 R-Car V4M PCI Express ch0 Target impedance curve

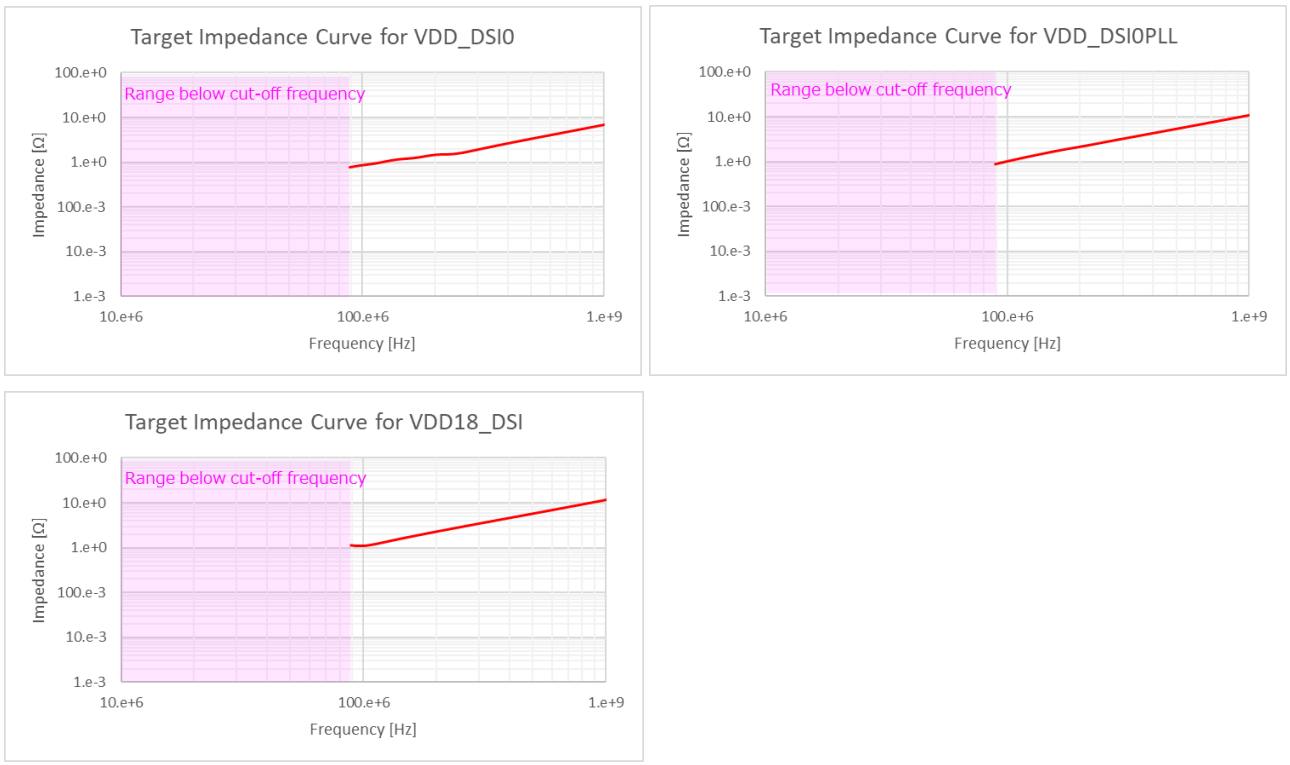

Figure 4-4 R-Car V4M DSI0 Target impedance curve

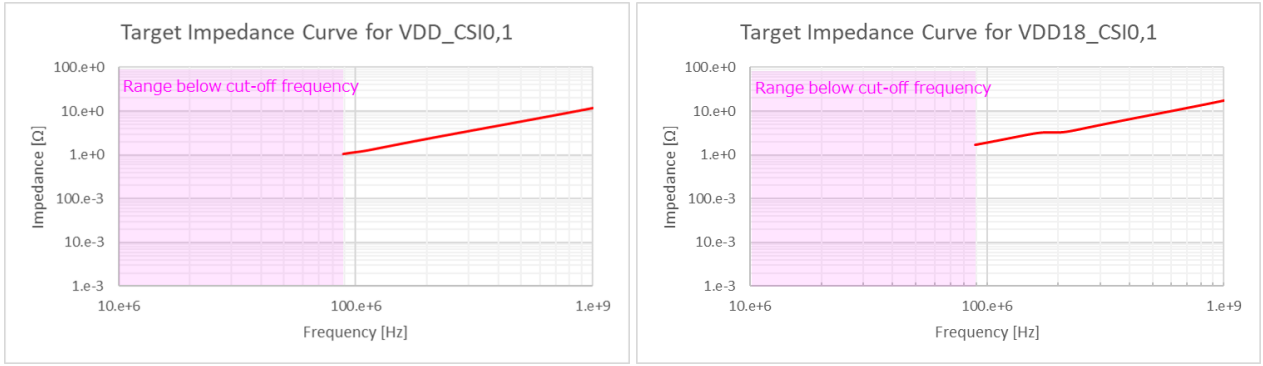

Figure 4-5 R-Car V4M CSI0, CSI1 Target impedance curve

4.3.2 Target filter requirement

The target filter curve list is shown in Table 4-2.

If the noise source on the PCB has a high-frequency component, noise attenuation by a filter is required. This is because the higher the noise frequency, the more it affects the timing of the high-speed signal.

[Testbench]

The requirement must be verified for each power supply.

Figure 4-6 testbench for verification

Table 4-2. R-Car X5H Target filter curve list

Module	Pin Name	IR-Drop	Target cut-off frequency	Limit amplitude of noise source on PCB
PCI Express ch0	VDD_PCIE0	(See Note 1)	90MHz	+/- 0.06V
	VDD18_PCIE0	(See Note 1)	90MHz	+/- 0.1V
DSI0	VDD_DSI0	(See Note 1)	90MHz	+/- 0.06V
	VDD_DSI0PLL	(See Note 1)	90MHz	+/- 0.06V
	VDD18_DSI	(See Note 1)	90MHz	+/- 0.1V
CSI0,1 MIPI Receiver	VDD_CSI0	(See Note 1)	90MHz	+/- 0.06V
	VDD_CSI1	(See Note 1)	90MHz	+/- 0.06V
	VDD18_CSI0	(See Note 1)	90MHz	+/- 0.1V
	VDD18_CSI1	(See Note 1)	90MHz	+/- 0.1V

[Note]

1. Please make sure IR-drop is within the DC range of the product power supply. Especially, when RC-filter is adopted, the influence of IR-drop is greater.

2. The noise attenuation by filter is necessary to satisfy the requirement for ripple noise inside the chip. However, the noise amplitude of noise source on the PCB is depends on the board design.

In addition, If the noise of power sources such as PMIC don't have the high frequency component (>100MHz) with amplitude of DC range, it is possible to ignore the gain curve for >100MHz.

5. Reference clock guideline

Serial interface modules require a high-quality reference clock supply.

5.1 Supply of reference clock for Serial Interface modules

The REFCLK pins of the serial interface modules must be supplied with a reference clock. They are supported a differential reference clock source. The REFCLK pins are shown in Table 5-1.

Table 5-1. REFCLK pins of Serial Interface modules

Number	Pin Name	Pin Function
<1>	PCIE0_CLK_P	PCI Express ch0 REFCLK pin (pos)
<2>	PCIE0_CLK_M	PCI Express ch0 REFCLK pin (neg)

Supply of reference clock for serial interface modules is shown in Figure 5-1.

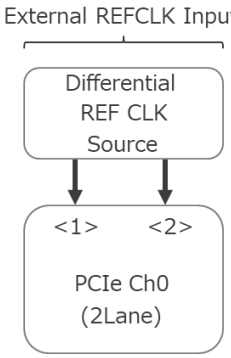

Figure 5-1 Supply of reference clock for Serial Interface modules

5.2 Reference clock specification

5.2.1 PCI Express reference clock requirement

The reference clock must meet requirements in the PCI Express Base Specification 4.0. The requirements are such as signal swing, jitter, edge rate, and so on.

PCI Express® Base Specification Revision 4.0 Version 1.0

8.6 Refclk Specifications

However, PCI Express modules have stricter restrictions than the PCI Express specifications in the items shown in Table 5-2. The reference REFCLK Waveform are shown in Figure 5-2.

Table 5-2. Restrictions of PCI Express modules

Symbol	Parameter	Min	Max	Unit
VMAX / VMIN	Absolute Max / Min input voltage	0	VDD max	V

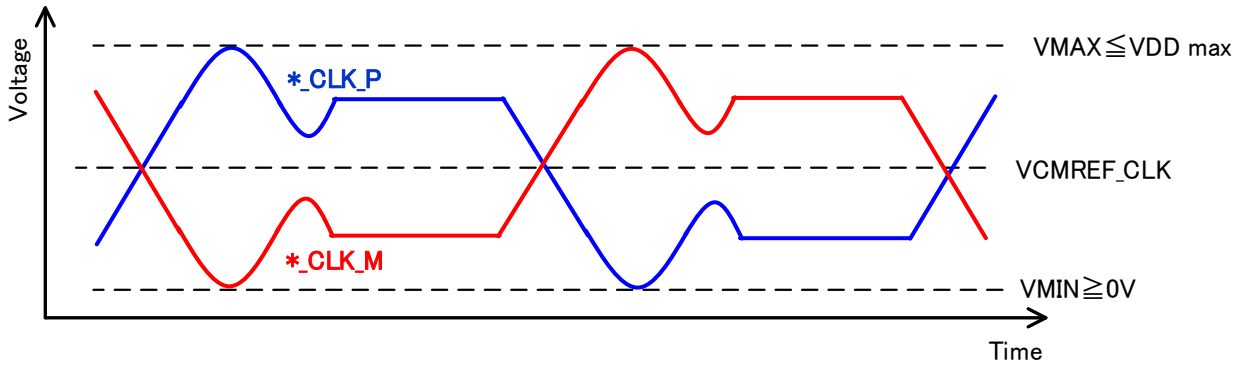

Figure 5-2 Restrictions of PCI Express modules

The reference clock and reference clock line must be designed and simulated to ensure signal integrity quality. Signal integrity verification for reference clock can be performed with the test configuration shown in Figure 5-3.

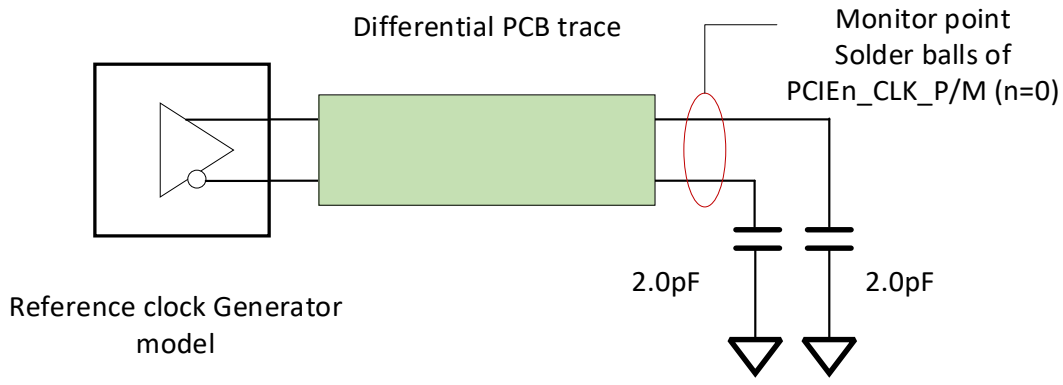

Figure 5-3 Test configuration of SI verification for reference clock

5.2.2 CSI/DSI reference clock requirement

CSI and DSI modules do not have external reference clock pins. The reference clock of the modules is supplied from inside chip.

5.3 Reference clock input structure

The REFCLK pins of serial interface modules are not on-chip terminated. Depending on the type of reference clock source, on-board termination may be required.

For example, for current drive such as HCSL, on-board termination is required. On the other hand, when using a push-pull voltage drive such as Low Power HCSL, this terminal is unnecessary.

Since the requirements for termination depend on the REFCLK source used, it is necessary to according to the specifications of the REFCLK source used. An example of On-Board termination is shown in Figure 5-4.

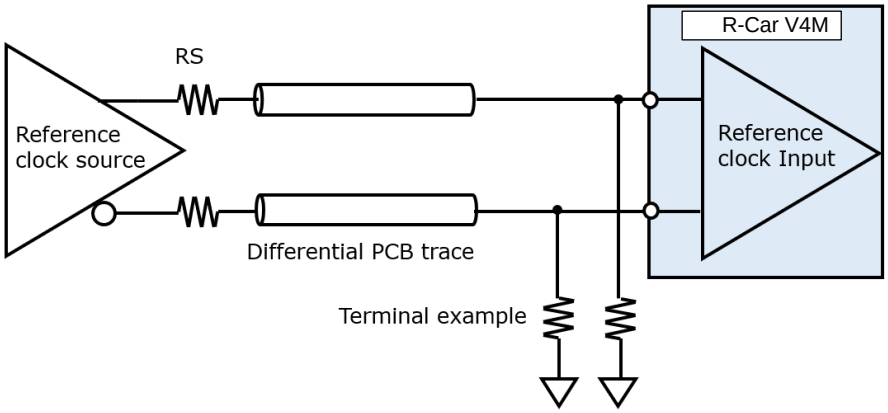

Figure 5-4 Reference clock source termination

6. External reference resistors guideline

Serial interface modules need to use external precision resistors when calibrating themselves. The RESREF pins of the serial interface modules must be connected to an external reference resistor.

6.1 External reference resistor specification

An external reference resistors specification is shown in Table 6-1.

Table 6-1 External reference resistors specification

Pin Name	Resistance	External Resistor Maximum Current
PCIE0_RESREF	200 Ω ±1%, ±100 ppm/degC	2mA (Note1)
DSI0_REXT	200 Ω ±1%, ±100 ppm/degC	(Note2)
CSI0_REXT	200 Ω ±1%, ±100 ppm/degC	(Note2)
CSI1_REXT	200 Ω ±1%, ±100 ppm/degC	(Note2)

Note

1. Current flows in the external resistor during calibration. This is not a DC current, and no current flows in the external resistor during not calibration.
2. The resistor is only used on the calibration procedures during the PHY Start-up. Leakage from inactive circuits is less than 10uA.

6.2 Constraints on parasitic components

Parasitic components for external resistance wirings are shown in Figure 6-1.

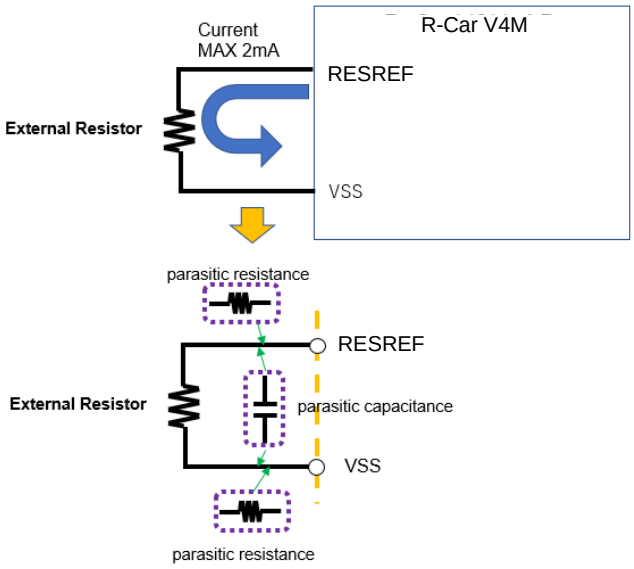

Figure 6-1 Parasitic components for external resistance wiring

There is a constraint on the parasitic component for external resistance wirings. The constraints on parasitic components is shown in Table 6-2.

Table 6-2 Constraints on parasitic components

Pin Name	Item	Maximum value
PCIE0_RESREF	parasitic capacitance	7.2pF
	parasitic resistance	1Ω
DSI0_REXT	parasitic capacitance	8pF
	parasitic resistance	0.8Ω
CSI0_REXT	parasitic capacitance	6.4pF
	parasitic resistance	0.35Ω
CSI1_REXT	parasitic capacitance	6.4pF
	parasitic resistance	0.35Ω

If the parasitic component is not satisfied, correct calibration can’t be performed.

7. Configuration when each Serial Interface modules is unused

If the serial interface module is unused, the following configuration can be used for the power supply and signal pins. In this configuration, the serial interface modules must always be disabled.

7.1 Signal pins

The TX, RX, and RESREF pins of the unused serial interface modules can be left floating except for DPHY. CLK pins of the unused serial interface modules should be connected to Ground. The list of R-Car V4M serial interface signal pins is shown in Table 7-1.

Table 7-1 Signal pins of the unused Serial Interface modules

IP	Terminals	Condition
PCI Express	PCIE0_CLK_P	Connect to Ground
	PCIE0_CLK_M	Connect to Ground
	PCIE0_TX0_P	Leave floating.
	PCIE0_TX0_M	Leave floating.
	PCIE0_RX0_P	Leave floating.
	PCIE0_RX0_M	Leave floating.
	PCIE0_TX1_P	Leave floating.
	PCIE0_TX1_M	Leave floating.
	PCIE0_RX1_P	Leave floating.
	PCIE0_RX1_M	Leave floating.
	PCIE0_RESREF	Leave floating.
DSI0	DSI0_CLKP	Connect to Ground
	DSI0_CLKN	Connect to Ground
	DSI0_DATAP0	Leave floating.
	DSI0_DATAN0	Leave floating.
	DSI0_DATAP1	Leave floating.
	DSI0_DATAN1	Leave floating.
	DSI0_DATAP2	Leave floating.
	DSI0_DATAN2	Leave floating.
	DSI0_DATAP3	Leave floating.
	DSI0_DATAN3	Leave floating.
	DSI0_REXT	Connect to Ground
CSI0 MIPI Receiver	CSI0_DATAP0	Connect to Ground
	CSI0_DATAN0	Connect to Ground
	CSI0_DATAP1	Connect to Ground
	CSI0_DATAN1	Connect to Ground
	CSI0_CLKP	Connect to Ground
	CSI0_CLKN	Connect to Ground
	CSI0_DATAP2	Connect to Ground
	CSI0_DATAN2	Connect to Ground
	CSI0_DATAP3	Connect to Ground
	CSI0_DATAN3	Connect to Ground
	CSI0_REXT	Connect to Ground
CSI1 MIPI Receiver	CSI1_DATAP0	Connect to Ground
	CSI1_DATAN0	Connect to Ground
	CSI1_DATAP1	Connect to Ground
	CSI1_DATAN1	Connect to Ground
	CSI1_CLKP	Connect to Ground
	CSI1_CLKN	Connect to Ground
	CSI1_DATAP2	Connect to Ground
	CSI1_DATAN2	Connect to Ground
	CSI1_DATAP3	Connect to Ground
	CSI1_DATAN3	Connect to Ground
	CSI1_REXT	Connect to Ground

7.2 Power supply pins

It is necessary to connect a power supply to the power supply pins of serial interface modules which is unused. The serial interface modules must be supplied with power even in the disable.
It is not necessary to mount the capacitors and ferrite beads of serial interface modules which is unused. The capacitors and ferrite beads for power supply are to ensure the power supply quality for normal operation of the serial interface modules. Not required if the serial interface modules are always disabled. The list of R-Car V4M serial interface power supply pins is shown in Table 7-2.

Table 7-2 Power Supply pins of the unused Serial Interface modules

IP	Terminals	Condition
PCI Express ch0	VSS	Connect to Ground
	VDD_PCIE0	Connect to VDD system power supply
	VDDQ18_PCIE0	Connect to VDD18 power supply
DSI0	VDD_DSI0	Connect to VDD system power supply
	VDD_DSI0PLL	Connect to VDD system power supply
	VDD18_DSI	Connect to VDD18 power supply
CSI0 MIPI Receiver	VDD_CSI0	Connect to VDD system power supply
	VDD18_CSI0	Connect to VDD18 power supply
CSI1 MIPI Receiver	VDD_CSI1	Connect to VDD system power supply
	VDD18_CSI1	Connect to VDD18 power supply

For example, when only the PCIE0 module are used and the DSI, CSI modules are unused, the configuration shown in Figure 7-1 is possible.

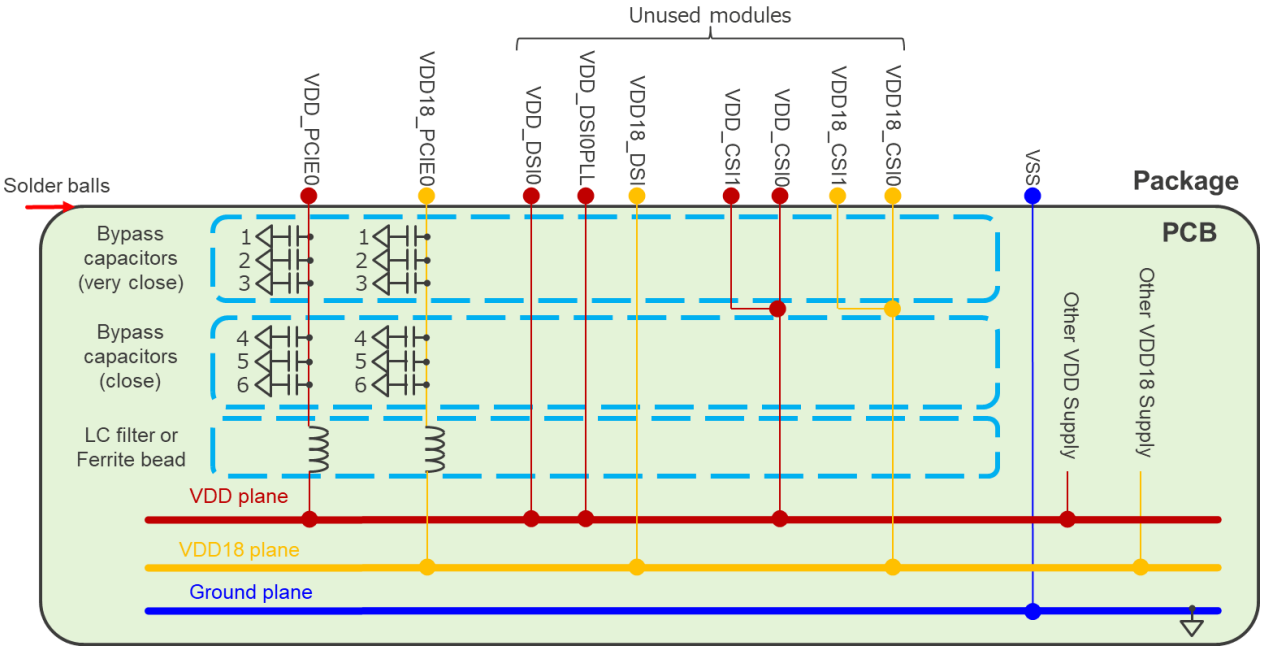

Figure 7-1 Configuration example for unused module

Revision History

Rev.	Date	Description	
		Page	Summary
0.5	2022/09/30	–	Preliminary edition
0.9	2023/01/31	–	■Revision and Date update ■Chapter 1, Table 1-3 (Removed “T.B.D.”) ■Chapter 3, Table 3-1, 3-2, 3-3 (Removed “In preparation”) ■Chapter 4, Figure 4-5, 4-6, 4-7 (Added Impedance curve)
1.0	2025/03/17	–	■Chapter 4, Figure 4-5, 4-6, 4-7 (Relaxation of pole components on the high frequency of Impedance curve.) ■Chapter 4, Table 4-1 (modified due to the above relaxation) ■Chapter 6, Table 6-2 (Removed “T.B.D.”)

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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