R-Car V4M

SerDes Interface IBIS-AMI Model

Introduction

This application note describes how to use the Interface IBIS-AMI models for signal integrity verification of R-Car V4M.

Target Device

PCIe-Express

Contents

1. Preface

1.1 Purpose

Provided models are for signal integrity verification of R-Car V4M FCBGA. The target macros are PCI-Express Gen4.

1.2 Simulation Environment

Recommended Simulator: ADVANCED DESIGN SYSTEM* (ADS) 2017.01 Copyright © Keysight Technologies 1985- 2017.

(*)This simulator has been checked for operation.

This simulation environment supports only Linux 64-bit.

1.3 Disclaimer

These SerDes interface models are provided "AS IS" with no warranty and Renesas Electronics is not responsible for any problems this model may cause to the users. These models are subject to change without any notice.

Renesas Electronics does not support user's PCB board design.

2. Provided Model Files

2.1 Package Model

The provided Package models are shown in Table 2-1.

Table 2-1 Provided Package Model Files

Macro	File Name	File Descriptions
PCI-Express	RCV4M_FCBGA25sq_PCIe_CH0.s16p	The spara file of Package Model for PCIe Ch0.

2.2 TX Interface Model

2.2.1 PCI-Express

There are two types of TX interface models, one for 16GT/s and the other for 2.5GT/s, 5.0GT/s and 8.0GT/s. The provided TX interface models are shown in Table 2-2.

Table 2-2 Provided TX Interface Model Files for PCI-Express

Macro	File Name	File Descriptions
PCI-Express	pcie4_tx_2p5_5_8G_ami.ibs	The IBIS file of PCIe TX for 2.5GT/s, 5.0GT/s and 8.0G T/s.
	pcie4_tx_16G_ami.ibs	The IBIS file of PCIe TX for 16GT/s.
	pcie4_tx_2p5_5_8G_AMI.ami	The ami file of PCIe TX for 2.5GT/s, 5.0GT/s and 8.0G T/s.
	pcie4_tx_16G_AMI.ami	The ami file of PCIe TX for 16GT/s.
	pcie4_tx_AMI_x64.dll	The AMI executables for Windows 64-bit platform.
	pcie4_tx_AMI_x64.so	The AMI executables for Linux 64-bit platform.
	pcie4_tx_fast.s4p	TX on-die spara file
	pcie4_tx_typ.s4p	TX on-die spara file
	pcie4_tx_slow.s4p	TX on-die spara file

2.3 RX Interface Model

2.3.1 PCI-Express

There is one type of RX interface models for 2.5GT/s, 5.0GT/s, 8.0GT/s and 16.0GT/s. The provided RX interface models are shown in Table 2-3.

Table 2-3 Provided RX Interface Model Files for PCI-Express

Macro	File Name	File Descriptions
PCI-Express	pcie4_rx_ami.ibs	The IBIS file of PCIe RX.
	pcie4_rx_AMI.ami	The ami file of PCIe RX.
	pcie4_rx_AMI.dll	The AMI executables for Windows 32-bit platform.
	pcie4_rx_AMI_x64.dll	The AMI executables for Windows 64-bit platform.
	pcie4_rx_AMI_x64.so	The AMI executables for Linux 64-bit platform.

2.4 Sample Test Bench

The provided sample test bench Files are shown in Table 2-4.

Table 2-4 Provided Sample Test Bench Files

Macro	File Name	File Descriptions
PCI-Express	pcie_testbench.7zads	An example PCIe IBIS-AMI TX to RX channel simulation for 16GT/s, 8.0GT/s, 5.0GT/s and 2.5GT/s is included

3. Details of Interface Model

3.1 PCI-Express

3.1.1 Configurable Parameters

Parameters of the user configurable PCIe model are shown in Table 3-1.

Table 3-1 Parameters of the user configurable for PCIe

Parameter	Value	Description
Xtx_process	slow=5, typical=1, fast=4 (Default 1)	TX process corner
Xvptx	min= VDD_PCIEn (min), typical= VDD_PCIEn (typ), max= VDD_PCIEn (max)	xvptx controls the VDD_PCIEn(n=0 to 1) supply voltage
XTx_main	2.5GT/s, 5.0GT/s: See Table 3-2 8.0GT/s, 16GT/s: See Table 3-3	2.5GT/s, 5.0GT/s: These control De-Emphasis settings 8.0GT/s, 16GT/s: These control Preset settings
XTx_post		
XTx_pre		
Tstonefile	“pcie4_tx_fast.s4p” “pcie4_tx_typ.s4p” (Default) “pcie4_tx_slow.s4p”	TX on-die spara file

Table 3-2 De-Emphasis settings for PCIe 2.5GT/s, 5.0GT/s

Swing	De-Emphasis	XTx_main	XTx_post	XTx_pre
Full Swing	2.5GT/s 3.5dB	20	16	0
Full Swing	5.0GT/s 3.5dB	20	16	0
Full Swing	5.0GT/s 6.0dB	18	24	0
Reduced Swing	2.5GT/s 3.5dB	10	8	0
Reduced Swing	5.0GT/s 3.5dB	10	8	0
Reduced Swing	5.0GT/s 6.0dB	9	12	0

Table 3-3 Preset setting for PCIe 8.0GT/s, 16GT/s

Swing	Preset	XTx_main	XTx_post	XTx_pre
Full Swing	P0	18	24	0
Full Swing	P1	20	16	0
Full Swing	P2	19	20	0
Full Swing	P3	21	12	0
Full Swing	P4	24	0	0
Full Swing	P5	22	0	8
Full Swing	P6	21	0	12
Full Swing	P7	17	18	10
Full Swing	P8	18	12	12
Full Swing	P9	20	0	16
Full Swing	P10	16	32	0
Reduced Swing	P1	10	8	0
Reduced Swing	P3	10	8	0
Reduced Swing	P4	12	0	0
Reduced Swing	P5	11	0	4
Reduced Swing	P6	10	0	8
Reduced Swing	P9	10	0	8

3.1.2 TX model Usage for 16GT/s

PCIe4 Tx model for 16GT/s is defined for channel simulation use through one *.ibs file: pcie4_tx_16G_ami.ibs. The PCIe4 Tx AMI model for 16GT/s supports PCIe4 rate at 16GT/s. The Tx intrinsic jitter budgets are defined in pcie4_tx_16G_AMI.ami files in the Reserved_Parameters section. A sample test pattern is provided in example IBIS-AMI model simulation (LFSR7). User can set any data pattern as stimulus for TX. The PCIe4 for 16GT/s Tx AMI models, including the AMI executables (*x64.so in Linux 64-bit) shall be used with both statistical analysis and time domain analysis enabled for most accurate analysis. This IBIS-AMI model internally references the TX on-die spara file. TX on-die spara file can be specified by Tstonefile parameter.

3.1.3 TX model Usage for 2.5GT/s, 5.0GT/s and 8.0GT/s

PCIe4 Tx model for 2.5GT/s, 5.0GT/s and 8.0GT/s is defined for channel simulation use through one *.ibs file: pcie4_tx_2p5_5_8G_ami.ibs. The PCIe4 Tx AMI model for 2.5GT/s, 5.0GT/s and 8.0GT/s supports PCIe4 rate at 2.5GT/s, 5.0GT/s and 8.0GT/s. The Tx intrinsic jitter budgets are defined in pcie4_rx_2p5_5_8G_AMI.ami files in the Reserved_Parameters section. A sample test pattern is provided in example IBIS-AMI model simulation (LFSR7). User can set any data pattern as stimulus for TX. The PCIe4 for 2.5GT/s, 5.0GT/s and 8.0GT/s Tx AMI models, including the AMI executables (*x64.so in Linux 64-bit) shall be used with both statistical analysis and time domain analysis enabled for most accurate analysis. This IBIS-AMI model internally references the TX on-die spara file. TX on-die spara file can be specified by Tstonefile parameter.

3.1.4 RX model Usage

PCIe4 Rx model is defined for channel simulation use through one *.ibs file: pcie4_rx_ami.ibs. The PCIe4 Rx AMI model supports PCIe4 rate at 2.5GT/s, 5.0GT/s and 8.0GT/s, 16GT/s. This RX model is for expressing only the ideal RX input load of 50 ohms. The output waveform of the RX model is the same as the input waveform. The PCIe4 Rx AMI models, including the AMI executables (*x64.so in Linux 64-bit) shall be used with both statistical analysis and time domain analysis enabled for most accurate analysis.

3.1.5 Sample Bench Usage for 16GT/s

The following figure shows a sample PCIe IBIS-AMI TX to RX link simulation setup with blocking capacitance and ideal channel model in place. The sample bench can be modified and simulated according to the user's board environment. These setups are available in the pcie4_16G_testbench contained in the pcie_testbench.7zads.

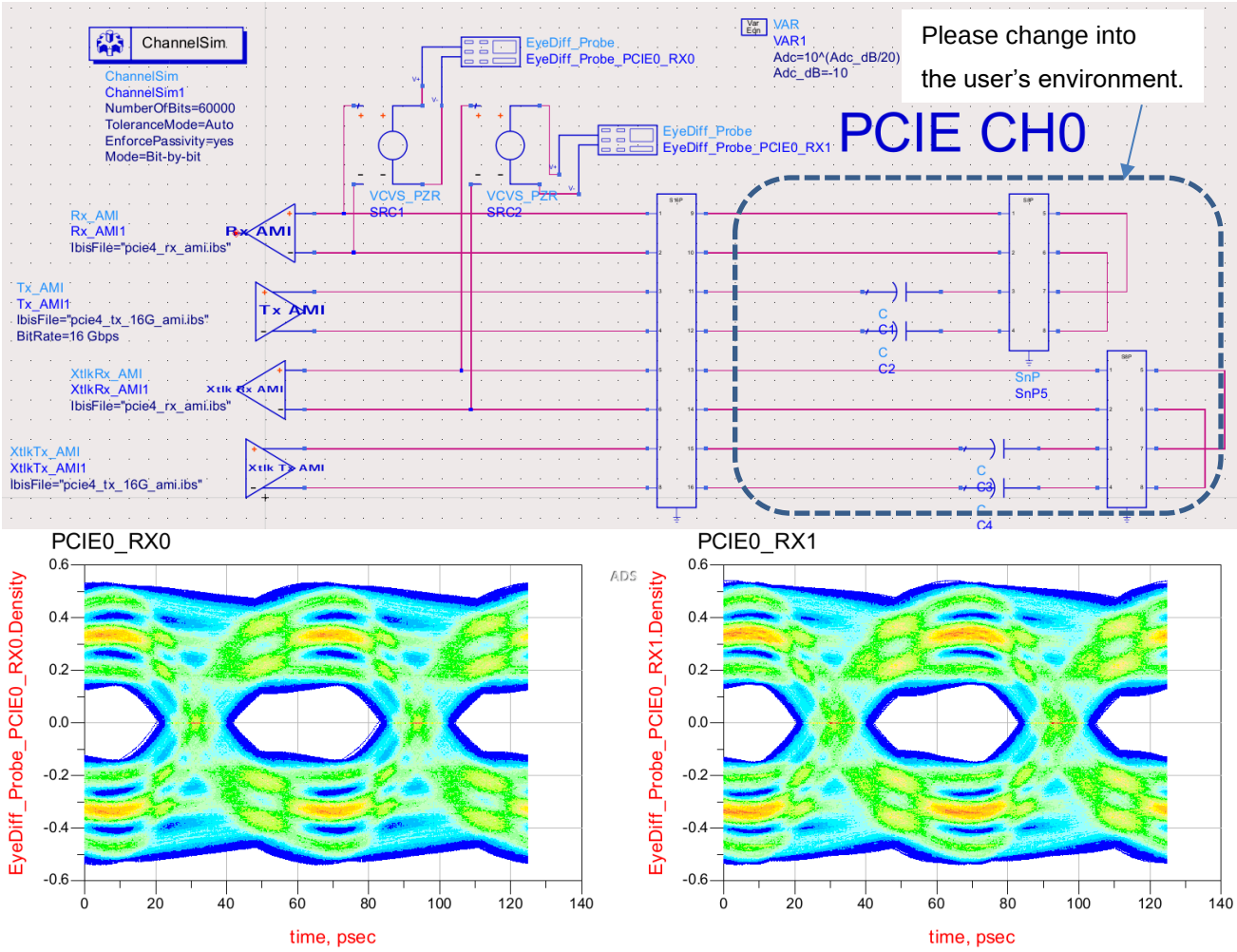

Figure 3-1 ADS Sample Bench for PCIe IBIS-AMI TX to RX Link Simulation for 16GT/s

3.1.6 Sample Bench Usage for 8.0GT/s

The following figure shows a sample PCIe IBIS-AMI TX to RX link simulation setup with blocking capacitance and ideal channel model in place. The sample bench can be modified and simulated according to the user's board environment. These setups are available in the pcie4_8G_testbench contained in the pcie_testbench.7zads.

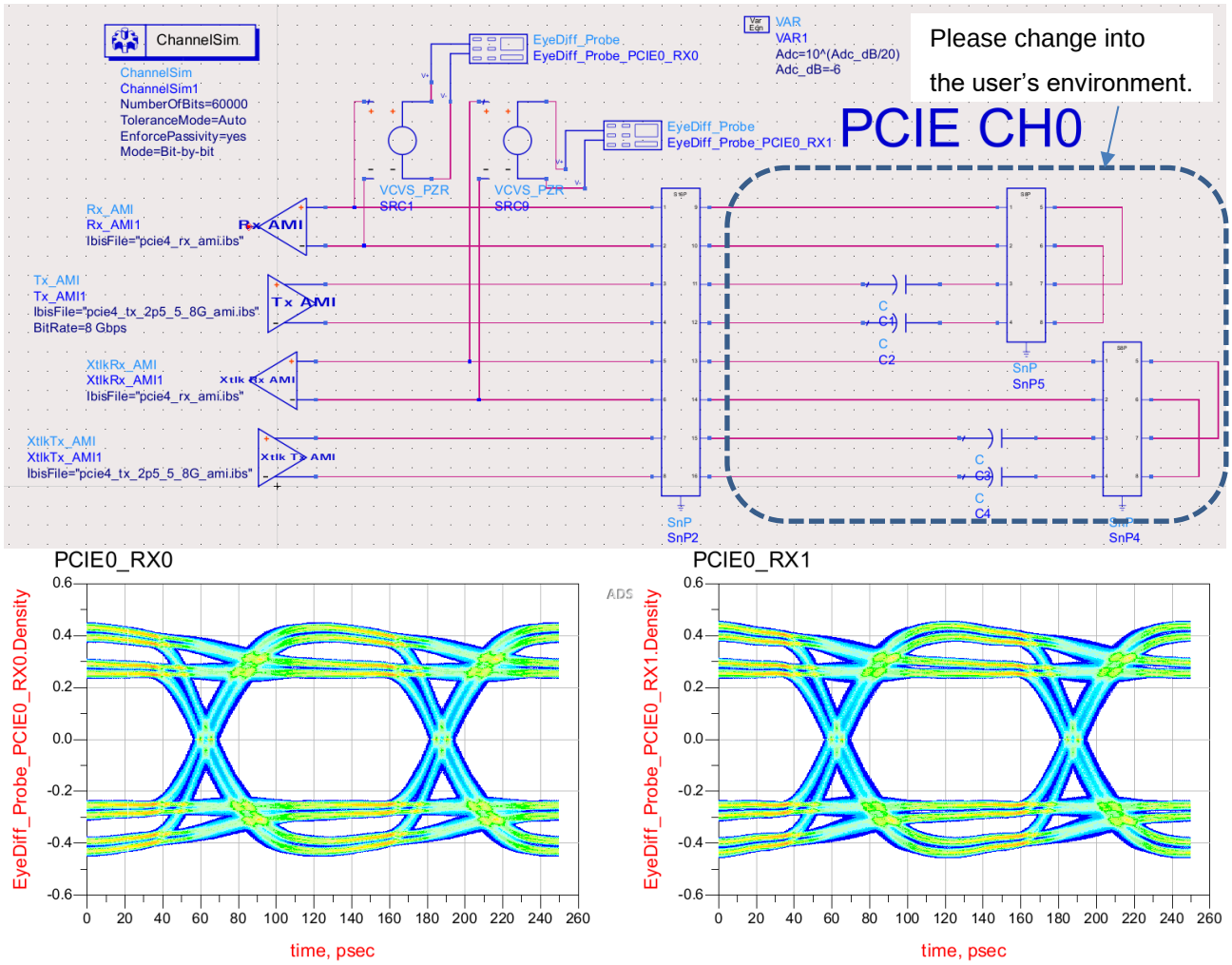

Figure 3-2 ADS Sample Bench for PCIe4 IBIS-AMI TX to RX Link Simulation for 8.0GT/s

3.1.7 Sample Bench Usage for 5.0GT/s

The following figure shows a sample PCIe IBIS-AMI TX to RX link simulation setup with blocking capacitance and ideal channel model in place. The sample bench can be modified and simulated according to the user's board environment. These setups are available in the pcie4_5G_testbench contained in the pcie_testbench.7zads.

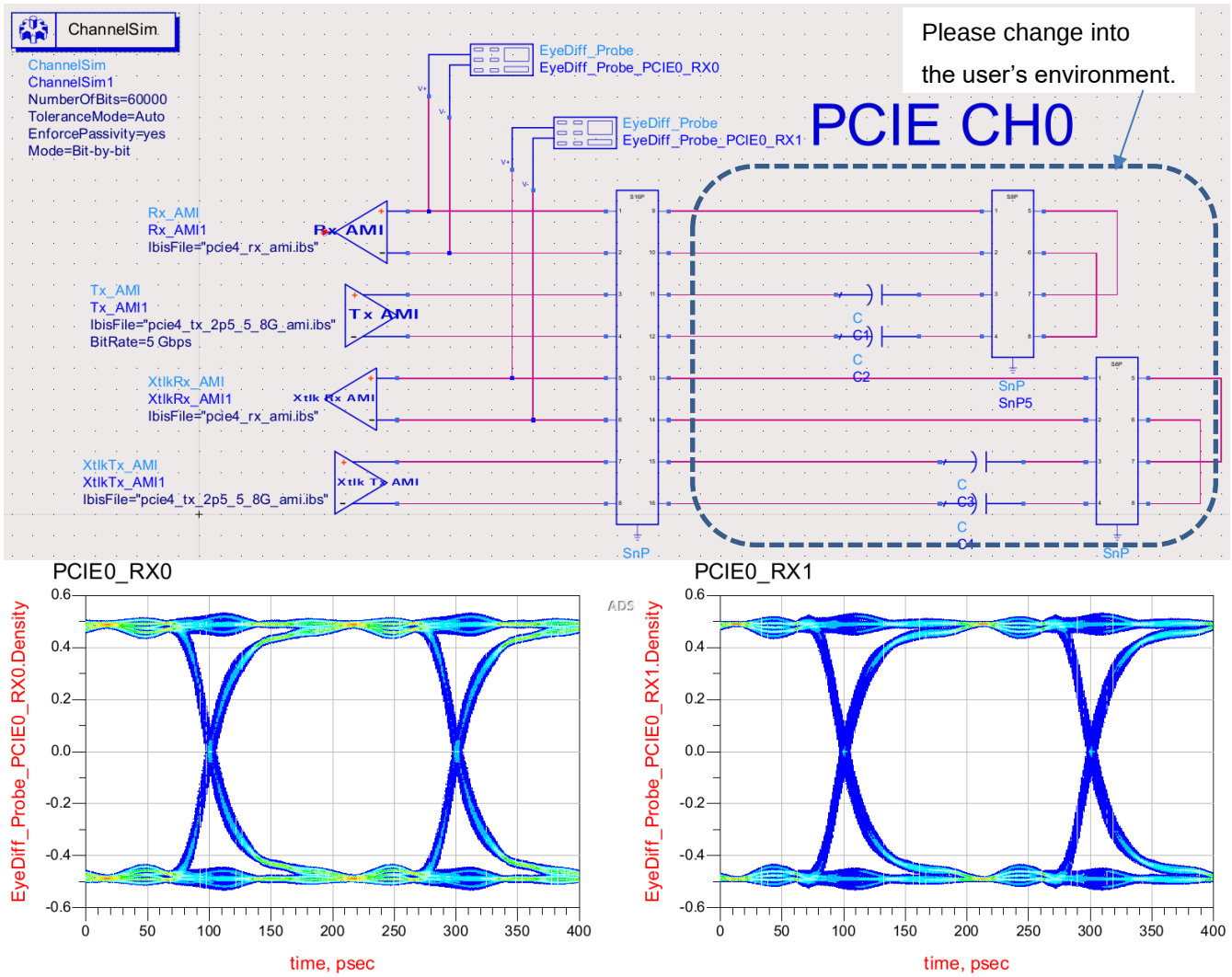

Figure 3-3 ADS Sample Bench for PCIe4 IBIS-AMI TX to RX Link Simulation for 5.0GT/s

3.1.8 Sample Bench Usage for 2.5GT/s

The following figure shows a sample PCIe IBIS-AMI TX to RX link simulation setup with blocking capacitance and ideal channel model in place. The sample bench can be modified and simulated according to the user's board environment. These setups are available in the pcie4_2p5G_testbench contained in the pcie_testbench.7zads.

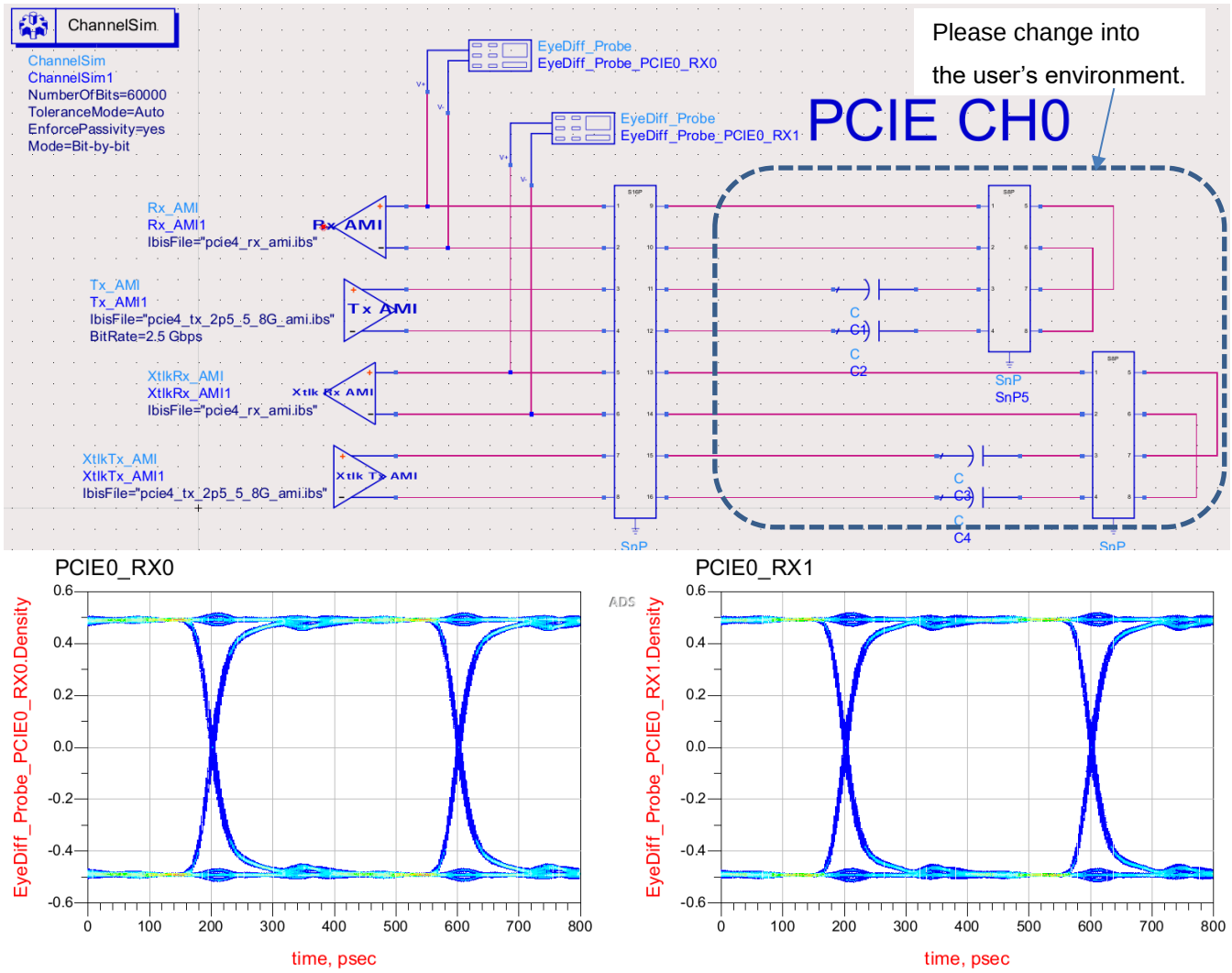

Figure 3-4 ADS Sample Bench for PCIe4 IBIS-AMI TX to RX Link Simulation for 2.5GT/s

Revision History

Rev.	Date	Description	
		Page	Summary
0.9	Jan/31/2023	-	First edition
1.0	Mar/17/2025	-	No change (revision change only)

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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