R-Car V4M

MIPI DPHY RX S-parameter Model

Introduction

This application note describes how to use the S-parameter models for signal integrity verification of R-Car V4M.

Target Device

MIPI DPHY RX

Contents

1. Preface

1.1 Purpose

Provided models are for signal integrity verification of R-Car V4M FCBGA. The target macros are MIPI DPHY RX.

1.2 Simulation Environment

Recommended Simulator: Synopsys HSPICE 2017.03-2. (This version has been checked for operation)

1.3 Disclaimer

These models are provided "AS IS" with no warranty and Renesas Electronics is not responsible for any problems this model may cause to the users. These models are subject to change without any notice.

Renesas Electronics does not support user’s PCB board design.

2. Provided Files

The provided files are shown in Table 2-1.

Table 2-1 Provided Files

File Type	No.	File Name	Descriptions
S-parameter model (Touchstone)	1	rcarv4m_mipi_dphyrx_fast.s40p	For dphy fast condition *1
	2	rcarv4m_mipi_dphyrx_slow.s40p	For dphy slow condition *1
	3	rcarv4m_mipi_dphyrx_ideal.s40p	For dphy ideal condition *2

*1 It needs to be confirmed that the target is satisfied for both fast and slow models.

*2 This model is only used when measuring the Teye_tx shown in chapter 3.

Since this is a simple tool with only limited functions, a trigger signal different from the normal one may be output when an unexpected waveform that does not satisfy the MIPI specification is input.

Please check if the trigger signal has no strange waveform such as trigger missing, glitch or others.

2.1 No.1/No.2/No.3：S-parameter for dphy (CSI0 and CSI1)

Figure 2-1 shows ports of S-parameter (File No. 1, 2 and 3) shown in Table 2-1.

For CSI0, ports 1 to 10 are on the BGA side and ports 21 to 30 are on PHY side.

For CSI1, ports 11 to 20 are on the BGA side and ports 31 to 40 are on PHY side.

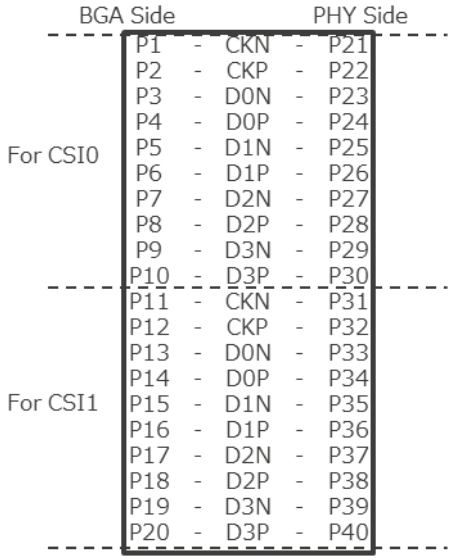

Figure 2-1 Ports of S-parameter model for dphy

3. Simulation bench and Result confirmation procedure

3.1 dphy

Figure 3-1 shows the connection on simulation bench to check eye diagram for Teye_pcb_tx.

Figure 3-2 shows the connection on simulation bench to check eye diagram for Teye_tx.

The TX model (refer to [Note 3-b]) and PCB model must be prepared by user side.

[Procedure]

1. probe the following signals;

   The data differential signals between D*P_PHY*(positive signal) and D*N_PHY*(negative signal).

   The clock differential signal between CKP_PHY*(positive signal) and CKN_PHY*(negative signal).

2. display the eye diagram for the following signals;

   The all csi0/1 data differential signals. (The red in Figure 3-1/Figure 3-2) (refer to [Note 2] below)

   The csi0/1 clock signal is used as the trigger signal. (Rise and Fall Edge) (The blue in Figure 3-1/Figure 3-2)

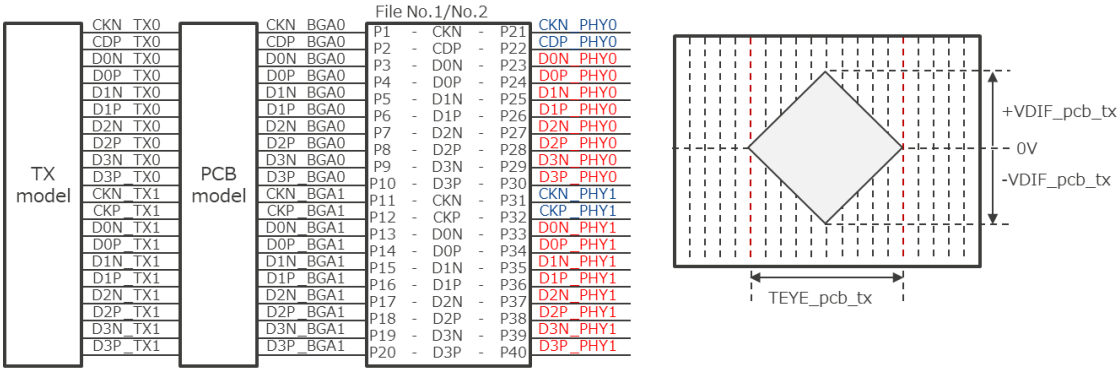

Figure 3-1 dphy simulation bench to check eye diagram for Teye_pcb_tx

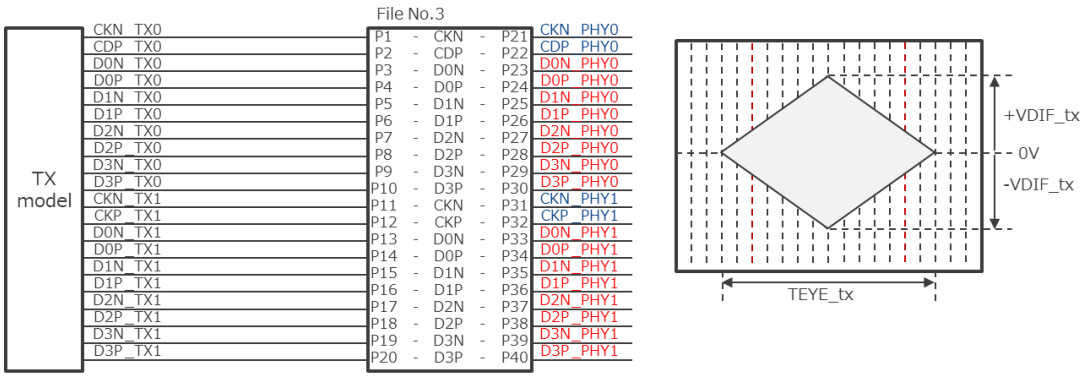

Figure 3-2 dphy simulation bench to check eye diagram for Teye_tx

3. measure TEYE_pcb_tx and |VDIF_pcb_tx| for the waveform of each data signal on the eye diagram.
   measure /TEYE_tx for the waveform of each data signal on the eye diagram. (refer to [Note 1] below)

4. calculate TEYE_pcb = TEYE_pcb_tx + (1UI – TEYE_tx)

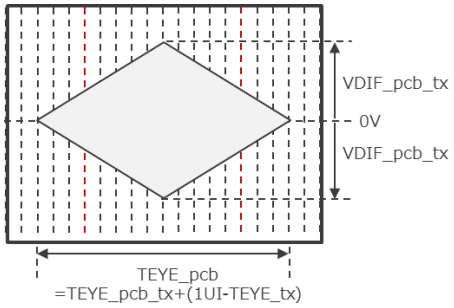

Figure 3-3 dphy Teye_pcb image

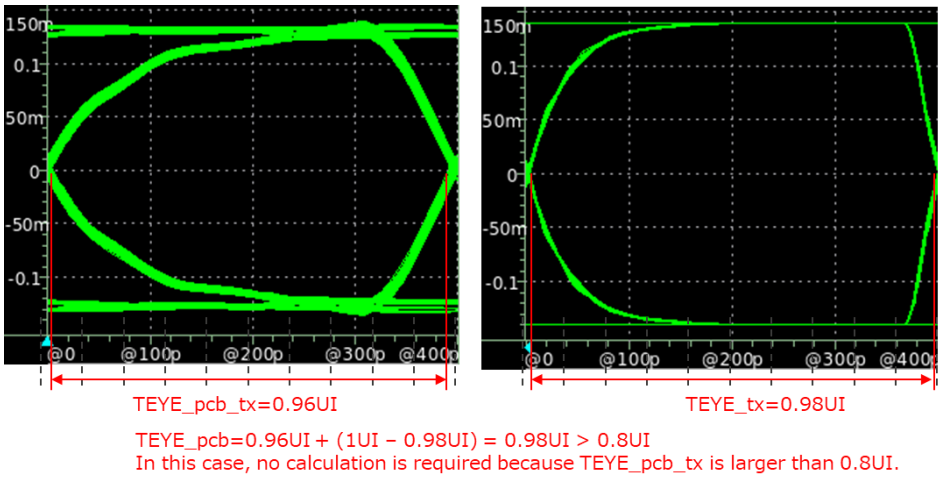

Figure 3-4 dphy Teye_pcb calculation example

5. check if |VDIF_pcb_tx| ≥ VDIF_RX(40mV) and TEYE_pcb ≥ TEYE_RX(0.8UI),
   TEYE_RX is replaced to 0.8UI from 0.5UI shown in MIPI specification.
   0.8UI is the value that does not include TX jitter and only takes PCB jitter into account.

[Note]

1. If TEYE_pcb_tx is larger than TEYE_RX(0.8UI), TEYE_tx does not need to be measured.
2. Since the S-parameter model (File No.1 and No.2) has input termination characteristics inside the PHY, it is unnecessary to connect the additional termination.
3. If the eye diagram specification TEYE_RX are not met,
   a. Please check if the wiring length difference between clock and data signals is small enough and if PCB characteristics meets MIPI D-PHY Specification; 8.6 Interconnect Specification.
   b. TXEQ1/EQ2 should be used. Please refer to MIPI D-PHY Specification; 10.4 Operating Modes: Data rate and Channel Support Guidance.

Revision History

Rev.	Date	Description	
		Page	Summary
0.9	Jan/31/2023	-	First edition
1.0	Mar/17/2025	-	No change (revision change only)

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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(Rev.5.0-1 October 2020)

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